Personal System/2
Model 50
Technical Reference

Third Edition (October 1990)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer of express or implied warranties in certain transactions, therefore, this statement may not apply to you.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Requests for technical information about IBM products should be made to your IBM Authorized Dealer or your IBM Marketing Representative.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

© Copyright International Business Machines Corporation 1989, 1990. All rights reserved.

Note to U.S. Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Special Notices

References in this publication to IBM products, programs, or services do not imply that IBM intends to make these available in all countries in which IBM operates. Any reference to an IBM product, program or service is not intended to state or imply that only IBM's product, program, or service may be used. Any functionally equivalent product, program, or service that does not infringe any of IBM's intellectual property rights or other legally protectible rights may be used instead of the IBM product, program, or service. Evaluation and verification of operation in conjunction with other products, programs, or services, except those expressly designated by IBM, are the user's responsibility.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

The following terms, denoted by an asterisk (*) in this publication, are trademarks of the IBM Corporation in the United States and/or other countries:

IBM
Micro Channel
Personal Computer AT
Personal System/2
PS/2

The following terms, denoted by a double asterisk (**) in this publication, are trademarks of other companies as follows:

Hitachi	Hitachi Corporation
Intel	Intel Corporation
Motorola	Motorola, Incorporated

Preface

This technical reference contains hardware and software interface information specific to the IBM Personal System/2 Model 50 computer. It is intended for those who develop hardware and software products for these systems. Users should understand computer architecture and programming concepts.

This publication consists of the following sections:

Section 1, "System Overview," describes the system, features and specifications.

Section 2, "Programmable Option Select," describes registers used for configuration.

Section 3, "System Board," describes the system specific hardware implementations.

This technical reference should be used with the following publications:

IBM Personal System/2 Hardware Interface Technical Reference — Architectures

IBM Personal System/2 Hardware Interface Technical Reference — Common Interfaces

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference

These publications contain additional information on many of the subjects discussed in this technical reference.

Warning: The term "Reserved" describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

© Copyright IBM Corp. 1989, 1990

Contents

Section 1. System Overview 1-1
Description 1-3
System Board Features 1-3
System Board Block Diagram 1-5
System Board I/O Address Map 1-6
Specifications 1-7
| Power Supply 1-11
| Outputs 1-11
| Output Protection 1-12
| Voltage Sequencing 1-12

Section 2. Programmable Option Select 2-1
Description 2-3
POS Address Map 2-5
Card Selected Feedback 2-6
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-7
System Board POS Register 2 (Hex 0102) 2-8
System Board POS Register 3 (Hex 0103) 2-9
Adapter Enable/Setup Register (Hex 0096) 2-10

Section 3. System Board 3-1
Description 3-3
| Micro Channel Implementation 3-3
| Exception Reporting 3-3
Adapter Identification 3-3
Central Arbiter 3-3
Memory 3-7
Read-Only Memory Subsystem 3-7
Random Access Memory Subsystem 3-7
Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM 3-12
Miscellaneous System Functions 3-24
Nonmaskable Interrupt 3-24
System Control Port B (Hex 0061) 3-24
System Control Port A (Hex 0092) 3-25
Power-On Password 3-27
Type 2 Serial Port Controller 3-28
Hardware Compatibility 3-28

Index X-1

© Copyright IBM Corp. 1989, 1990

Figures

1-1. Model and Submodel Bytes 1-3
1-2. System Board Devices and Features 1-4
1-3. System Board 1-5
1-4. System Board I/O Address Map 1-6
1-5. Performance Specifications — Type 1 System Board . . 1-7
1-6. Performance Specifications — Type 2 System Board . . 1-8
1-7. Physical Specifications 1-9
1-8. Acoustical Readings 1-10
1-9. Component Maximum Current 1-11
1-10. Channel Load Current 1-11
2-1. POS I/O Address Map 2-5
2-2. Card Selected Feedback Register (Hex 0091) 2-6
2-3. System Board Enable/Setup Register (Hex 0094) 2-7
2-4. System Board POS Register 2 (Hex 0102) 2-8
2-5. Parallel Port Select Bits 2-8
2-6. System Board POS Register (Hex 0103) 2-9
2-7. Adapter Enable/Setup Register (Hex 0096) 2-10
3-1. Arbitration Bus Priority Assignments 3-4
3-2. Arbitration Register, Write to Hex 0090 3-5
3-3. Arbitration Register, Read Hex 0090 3-5
3-4. System Memory Map 3-8
3-5. System Board Memory Connector, Type 1 3-9
3-6. System Board Memory Connector, Type 2 3-10
3-7. Presence Detect Encoding 3-11
3-8. RT/CMOS RAM Address Map 3-12
3-9. RT/CMOS Address Register and NMI Mask (Hex 0070) 3-13
3-10. RT/CMOS Data Register (Hex 0071) 3-13
3-11. Real-Time Clock Bytes 3-15
3-12. Status Register A 3-16
3-13. Status Register B 3-16
3-14. Status Register C 3-18
3-15. Status Register D 3-18
3-16. Diagnostic Status Byte 3-19
3-17. Diskette Drive Type Byte 3-20
3-18. Diskette Drive Type Byte (Bits 7 - 4) 3-21
3-19. Diskette Drive Type Byte (Bits 3 - 0) 3-21
3-20. Equipment Byte 3-22
3-21. Equipment Byte (Bits 7, 6) 3-22
3-22. Equipment Byte (Bits 5, 4) 3-22
3-23. System Control Port B (Write) 3-24
3-24. System Control Port B (Read) 3-25
3-25. System Control Port A (Hex 0092) 3-25

© Copyright IBM Corp. 1989, 1990

Section 1. System Overview

Description 1-3
System Board Features 1-3
System Board Block Diagram 1-5
System Board I/O Address Map 1-6
Specifications 1-7
| Power Supply 1-11
| Outputs 1-11
| Output Protection 1-12
| Voltage Sequencing 1-12

© Copyright IBM Corp. 1989, 1990

Notes:

Description

The IBM* Personal System/2* Model 50 computer is a self-contained, desktop system that features the Micro Channel* architecture. This system can support two diskette drives and one internal fixed disk drive and comes with a keyboard.

A system can have either a Type 1 or Type 2 system board. The major differences between the system boards are component layout, the maximum amount of system board memory, and the processor performance. Programs identify the type by reading the model and submodel bytes and BIOS revision code. Interrupt hex 15, function code (AH) = hex C0, returns the model and submodel bytes and BIOS revision code. The following figure shows these bytes and the system board types.

Model Byte	Submodel Byte	Revision Code	System Board
FC	04	00	Type 1
FC	04	03	Type 2

Figure 1-1. Model and Submodel Bytes

System Board Features

The following figure lists the system board devices and features. The Hardware Interface Technical Reference manuals describe devices common to PS/2* products by type number.

* IBM, Personal System/2, PS/2, and Micro Channel are trademarks of the International Business Machines Corporation.

Device	Type	Features
Microprocessor	---	80286 24-bit address and 16-bit data interface
System Timers	1	Channel 0 – System timer Channel 2 – Tone generation for speaker Channel 3 – Watchdog timer
ROM Subsystem	---	128KB (KB = 1024 bytes)
RAM Subsystem	---	Type 1 - 1MB on the system board (MB = 1,048,576 Bytes) Type 2 - 1MB or 2MB on the system board
CMOS RAM Subsystem	---	64-byte CMOS RAM with real-time clock/calendar Battery backup
Video Subsystem	1	Auxiliary connector on the channel Analog output 256KB video memory
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal.
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	1	Supports: - 720KB formatted diskette density - 1.44MB formatted diskette density.
Serial Controller	1, 2*	RS-232C interface Programmable as serial port 1 or 2
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output
Micro Channel	---	Four channel connectors for Type 3 adapters: - 8- or 16-bit device support - One with an auxiliary video extension - One occupied by the fixed disk drive adapter
Math Coprocessor Socket	---	Supports 80287 math coprocessor Same clock speed as the system microprocessor

* The Model 50 does not support the FIFO mode.

Figure 1-2. System Board Devices and Features

System Board Block Diagram

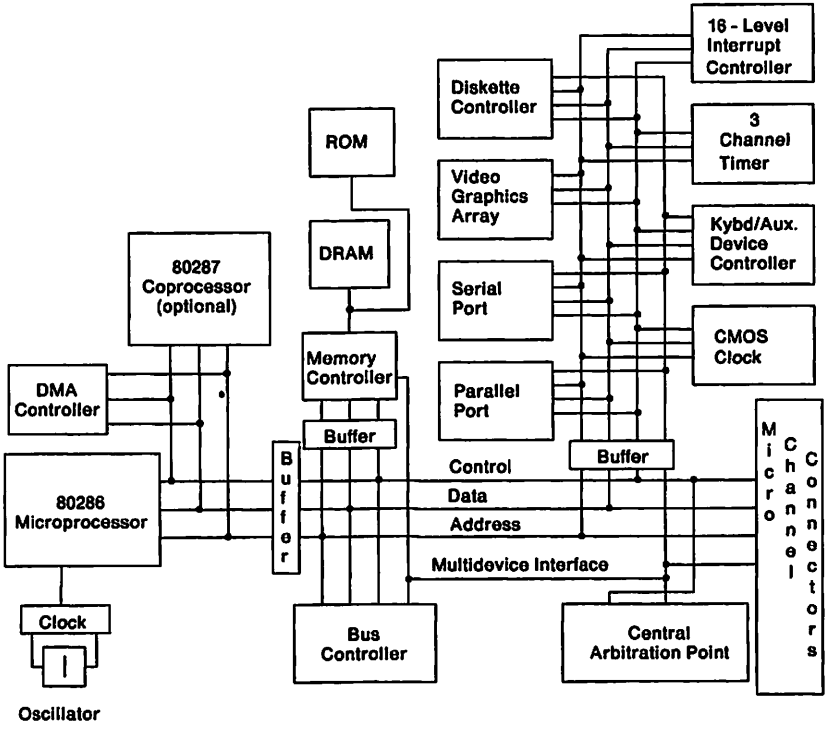


Figure 1-3. System Board

System Board I/O Address Map

Hex Addresses	Device
0000 - 001F	DMA Controller (0 – 3)
0020, 0021	Interrupt Controller (Master)
0040, 0042 - 0044, 0047	System Timers
0060	Keyboard, Auxiliary Device
0061	System Control Port B
0064	Keyboard, Auxiliary Device
0070, 0071	RT/CMOS and NMI Mask
0081 - 0083, 0087	DMA Page Registers (0 – 3)
0089, 008A, 008B, 008F	DMA Page Registers (4 – 7)
0090	Central Arbitration Control Point
0091	Card Selected Feedback Register
0092	System Control Port A
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
00A0 - 00A1	Interrupt Controller (Slave)
00C0 - 00DF	DMA Controller (4 – 7)
00F0 - 00FF	Math Coprocessor
0100 - 0107	Programmable Option Select
01F0 - 01F8	Fixed Disk Drive Controller
0278 - 027B	Parallel Port 3
02F8 - 02FF	Serial Port 2 (RS-232C)
0378 - 037B	Parallel Port 2
03B4, 03B5, 03BA	Video Subsystem
03BC - 03BF	Parallel Port 1
03C0 - 03C5	Video Subsystem
03C6 - 03C9	Video DAC
03CA, 03CC, 03CE, 03CF	Video Subsystem
03D4, 03D5, 03DA	Video Subsystem
03F0 - 03F7	Diskette Drive Controller
03F8 - 03FF	Serial Port 1 (RS-232C)

Figure 1-4. System Board I/O Address Map

Specifications

The following figure describes the Type 1 system board performance.

Device	Number of Waits	Cycle Time (ns)
Microprocessor (10 MHz – 100 ns Clock):		
Access to System Board RAM	1	300
Access to System Board ROM	1	300
Access to Channel:		
Default Transfer Cycle:		
I/O Access	1	300
Memory Access	0	200
Synchronous Extended Transfer Cycle	1	300
Refresh Rate (Typically performed every 15.1 μs)		500 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer: 300 + I/O Access + Memory Access		
Burst Transfers: 300 + (I/O Access + Memory Access)N*		
System Board Memory Access		300
Default Transfer Cycle:		
I/O Access		300
Memory Access		200
Synchronous Extended Transfer Cycle		300

* N is the number of transfers in the burst.

Figure 1-5. Performance Specifications – Type 1 System Board

The following figure describes the Type 2 system board performance. The Type 2 system board supports two speeds of system board memory. Cycle times differ depending upon the speed. See Figure 3-7 on page 3-11.

Device	Number of Waits	Cycle Time (ns)
Microprocessor (10 MHz – 100 ns Clock):		
Access to System Board RAM:		
85-ns Memory	0	200
120-ns Memory	1	300
Access to System Board ROM	1	300
Access to Channel:		
Default Transfer Cycle:		
I/O Access	1	300
Memory Access	0	200
Synchronous Extended Transfer Cycle	1	300
Refresh Rate (Typically performed every 15.1 μs)		500 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer: 300 + I/O Access + Memory Access		
Burst Transfers: 300 + (I/O Access + Memory Access)N*		
System Board Memory Access		
85-ns Memory		200
120-ns Memory		300
Default Transfer Cycle:		
I/O Access		300
Memory Access		200
Synchronous Extended Transfer Cycle		300
* N is the number of transfers in the burst.		

Figure 1-6. Performance Specifications – Type 2 System Board

The following figure describes the physical specifications of the system.

Size:	
Width	360 mm (14.1 in)
Depth	420 mm (16.5 in)
Height	140 mm (5.5 in)
Weight	9.55 kg (21 lb)
Cables:	
Power Cable	1.8 m (6 ft)
Keyboard Cable	1.8 m (6 ft)
Air Temperature:	
System On	15.6 to 32.2°C (60 to 90°F)
System Off	10.0 to 43.0°C (50 to 110°F)
Humidity:	
System On	8% to 80%
System Off	8% to 80%
Maximum Altitude	2133.6 m (7000 ft)
Heat Output	150 Watts(512 BTUs/hour)
Acoustical Readings	(See Figure 1-8 on page 1-10)
Electrical Input:	
Input Voltage (Range is automatically selected; sinewave input is required):	
Low Range	90 (min) – 137 (max) Vac
High Range	180 (min) – 265 (max)Vac
Frequency:	
Low Range	47 (min) – 53 (max) Hz
High Range	57 (min) – 63 (max) Hz
Input in Kilovolt-Ampere (kVA):	
Minimum configuration (as shipped by IBM)	0.11 kVA
Maximum configuration	0.25 kVA
Electromagnetic Compatibility	FCC Class B

Figure 1-7. Physical Specifications

The following figure describes the acoustical readings of the system.

Description	L_{WAd} in bels Operate	Idle	L_{pAm} in dB Operate	Idle	$<L_{pA}>_m$ in dB Operate	Idle
Model 50	5.1	5.1	41	40	38	37

Notes:

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

All measurements made in accordance with ANSI S12.10, and reported in conformance with ISO DIS 9296.

The measurements are preliminary data and subject to change.

Figure 1-8. Acoustical Readings

Power Supply

The power supply requires a sinewave input and converts the ac input voltage to three dc output voltages. The power supply provides power for the following:

- System board
- Channel adapters
- Internal diskette drives
- Internal fixed disk drives
- Auxiliary device
- Keyboard.

The power switch and one light-emitting diode (LED) is on the front of the system unit. The power supply is operating when the LED is lit.

Outputs

The power supply provides separate voltage sources for the system board and the drives. The system-board voltages are +5 Vdc, +12 Vdc, and −12 Vdc. The drive voltages are +5 Vdc and +12 Vdc. The following is a list of the approximate power provided for system components.

System Component	Maximum Current	
	+12 Vdc	+5 Vdc
Auxiliary Device	None	300 mA
Keyboard	None	275 mA

Figure 1-9. Component Maximum Current

The following are the load currents allowed for each Micro Channel connector.

Supply Voltage	Maximum Current
+ 5.0 Vdc	1.6 A
+12.0 Vdc	0.175 A
−12.0 Vdc	0.040 A

Figure 1-10. Channel Load Current

The formulas used to determine the power requirements and the voltage regulation tolerances are in the Micro Channel adapter design information in the *Hardware Interface Technical Reference - Architectures* manual.

Output Protection

A short circuit placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state with no damage to the power supply.

If an overvoltage fault occurs (internal to the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of its nominal value.

If either of these shutdown states is actuated, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least ten seconds.

Voltage Sequencing

At power-on time, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Section 2. Programmable Option Select

Description 2-3
POS Address Map 2-5
Card Selected Feedback 2-6
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-7
System Board POS Register 2 (Hex 0102) 2-8
System Board POS Register 3 (Hex 0103) 2-9
Adapter Enable/Setup Register (Hex 0096) 2-10

© Copyright IBM Corp. 1989, 1990

Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used specifically by the Model 50 system board. For additional POS information, refer to the Hardware Interface Technical Reference Micro Channel architecture information.

Warning:

- IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can cause multiple assignment of the same system resource, improper operation of the feature, loss of data, or possible damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention will occur, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- The channel reset bit (bit 7) in the Adapter Enable/Setup register must be 0 to program the adapters.
- The system board does not support 16-bit I/O operations to 8-bit POS registers. Using 16-bit I/O instructions on 8-bit POS registers will cause erroneous data to be written to or read from the registers. Only 8-bit transfers are supported for setup operations.

Setup functions respond to I/O addresses hex 0100 through 0107 only when their unique setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

System Board Video Subsystem Setup:

- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 0 to place the system board video into the setup mode.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 7 in the System Board Enable/Setup register (hex 0094) must be set to 1 to avoid driving a 'setup' signal to other system board functions.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 1 to allow adapter setup.
- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 1 to avoid driving a 'setup' signal to the Video Subsystem.
- Bit 7 in the System Board Enable/Setup register (hex 0094) must be set to 1 to avoid driving a 'setup' signal to a system board function.

Other System Board Setup:

- Bit 7 in the System Board Enable/Setup register (hex 0094) must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 1 to avoid driving a 'setup' signal to the Video Subsystem.

POS Address Map

The following figure shows the organization of the I/O address space used by POS. The POS registers are 8-bit registers. Bit 0 of POS Register 2 and bits 6 and 7 of POS Register 5 are defined. All other bits in POS Registers 2 through 5 are free-form.

Address (Hex)	Function
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
0100	POS Register 0—Adapter Identification Byte (Low Byte)
0101	POS Register 1—Adapter Identification Byte (High Byte)
0102	POS Register 2—Option Select Data Byte 1 Bit 0 is Card Enable.
0103	POS Register 3—Option Select Data Byte 2
0104	POS Register 4—Option Select Data Byte 3
0105	POS Register 5—Option Select Data Byte 4 Bit 7 is the channel check active indicator. Bit 6 is the channel check status-available indicator.
0106	Reserved
0107	Reserved

Figure 2-1. POS I/O Address Map

Card Selected Feedback

When the adapter is addressed, it responds by setting the '-card selected feedback' signal (-CD SFDBK) to active. -CD SFDBK is derived from the address decode and driven by a totem pole driver. It is latched by the system board and can be read through the Card Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and thereby determine if the video subsystem, system board I/O, or an adapter is addressed and functioning.

Bit	Function
7 - 1	Reserved
0	-Card Selected Feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7 - 1 Reserved.

Bit 0 This bit is set to 1 whenever -CD SFDBK was active on a previous cycle or whenever the system board I/O functions (diskette drive, serial, or parallel interfaces) are accessed by an I/O cycle. Reading this register resets the bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information during setup. The diskette drive controller, serial port, and parallel port are treated as a single device. The video subsystem is also an integrated part of the system board; however, POS treats it as a separate device. The System Board Enable/Setup register is used to place the system board or video subsystem into the setup mode.

System Board Enable/Setup Register (Hex 0094)

This is a read/write register; all bits in this register default to 1 (enabled).

Bit	Function
7	Enable/-Setup System Board Functions
6	Reserved
5	Enable/-Setup Video Subsystem
4 - 0	Reserved

Figure 2-3. System Board Enable/Setup Register (Hex 0094)

Bit 7 When this bit is set to 0, various system board I/O functions are placed in the setup mode. The diskette drive controller, serial port, and parallel port are controlled through System Board POS Register 2 (hex 0102). The memory is controlled through System Board POS Register 3 (hex 0103).

When this bit is set to 1, the system board functions are enabled.

Bit 6 Reserved.

Bit 5 When this bit is set to 0, the video subsystem is placed in the setup mode and controlled through POS Register 2 (hex 0102). When set to 1, and bit 0 in hex 0102 is set to 1, video is enabled.

Bit 0 of POS Register 2 is the video enable bit. When this bit is set to 0, the video subsystem does not respond to commands, addresses, or data. If video is being generated when the video enable bit is set to 0, the output is still generated. For information on BIOS calls to enable or disable the video, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Note: When the video is disabled, access to the video DAC registers is disabled.

Bits 4 - 0 Reserved.

System Board POS Register 2 (Hex 0102)

When the system board is in the setup mode, the diskette drive controller, serial port, and parallel port are controlled by this read/write register. Reading this register returns the current state of these system board functions.

Bit	Function
7	Disable Parallel Port Extended Mode
6, 5	Parallel Port Select
4	Enable Parallel Port
3	Serial Port Select
2	Enable Serial Port
1	Enable Diskette Drive Interface
0	Enable System Board

Figure 2-4. System Board POS Register 2 (Hex 0102)

Bit 7 When set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional interface. When set to 1, this bit disables the bidirectional mode. This bit is set to 0 at power-on, and POST sets it to 1.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Hex Address	Interrupt Level
0 0	Parallel 1	03BC - 03BF	7
0 1	Parallel 2	0378 - 037B	7
1 0	Parallel 3	0278 - 027B	7
1 1	Reserved	----------	-

Figure 2-5. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bit 3 When set to 1, this bit sets the system board serial port as Serial 1 (addresses hex 03F8 through 03FF), which uses interrupt level 4. When set to 0, this bit sets the serial port as Serial 2 (addresses hex 02F8 through 02FF), which uses interrupt level 3.

Bit 2 When this bit and bit 0 are set to 1, the system board serial port is enabled.

Bit 1 When this bit and bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When set to 1, this bit allows bits 4, 2, and 1 to enable and disable their respective devices. When set to 0, this bit disables the diskette drive interface, system board serial port, and system board parallel port, regardless of the state of bits 4, 2, and 1.

System Board POS Register 3 (Hex 0103)

With the system board in setup, this register controls the system board memory.

Bit	Function
7 - 1	Reserved
0	Enable System Board RAM

Figure 2-6. System Board POS Register (Hex 0103)

Bit 7 - 1 Reserved.

Bit 0 When set to 1, this bit enables the system board memory. When set to 0, this bit disables the memory. All system board memory is enabled or disabled by this operation.

Adapter Enable/Setup Register (Hex 0096)

The Adapter Enable/Setup register selects the connector to be configured.

Bit	Symbol
7	Channel Reset
6 - 4	Reserved
3	Card Setup Enable
2 - 0	Channel Select 2 - 0

Figure 2-7. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6 - 4 These bits are reserved.

Bit 3 When set to 1, this bit enables the '-card setup' signal selected by bits 2 through 0.

Bits 2 - 0 These bits are the address bits for the '-card setup' signal Connectors 1 through 4 are addressed as 0 through 3, respectively. When bit 3 is set to 1, these bits select the connector that is put into setup.

Each channel connector has a unique '-card setup' signal (-CD SETUP) associated with it. This signal is used to put the adapters in the setup mode, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Notes:

1. -CD SETUP goes active only when an operation is performed in the I/O address range hex 0100 through 0107.
2. The status of port hex 0096 can be read by software. However, when the port is read, bits 6, 5, and 4 are set to 1.

Section 3. System Board

Description 3-3
Micro Channel Implementation 3-3
Exception Reporting 3-3
Adapter Identification 3-3
Central Arbiter 3-3
Arbitration Bus Priority Assignments 3-4
Central Arbiter Programming 3-5
Memory 3-7
Read-Only Memory Subsystem 3-7
Random Access Memory Subsystem 3-7
System Memory Maps 3-8
System Board Memory Connector 3-9
Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM 3-12
RT/CMOS Address Register and NMI Mask (Hex 0070) . . 3-13
RT/CMOS Data Register (Hex 0071) 3-13
RT/CMOS RAM I/O Operations 3-14
Real-Time Clock Bytes (Hex 000-00D) 3-15
CMOS RAM Configuration 3-19
Miscellaneous System Functions 3-24
Nonmaskable Interrupt 3-24
System Control Port B (Hex 0061) 3-24
System Control Port A (Hex 0092) 3-25
Power-On Password 3-27
Type 2 Serial Port Controller 3-28
Hardware Compatibility 3-28

© Copyright IBM Corp. 1989, 1990

Notes:

Description

This section provides information about the Model 50 implementation of the Micro Channel, memory subsystem, and miscellaneous system ports. Additional information on these topics can be found in the Hardware Interface Technical Reference manuals listed in the preface of this manual.

Micro Channel Implementation

The POST routines and registers used to implement programmable features of the Micro Channel architecture may vary from system to system. This section provides information about the Model 50 implementation of the Micro Channel architecture.

Exception Reporting

Exceptions should be reported using the asynchronous channel check procedure. The synchronous channel check procedure is not supported.

Adapter Identification

When the system is powered on, an adapter can issue an ID of hex 0000 for up to 1 second after channel reset to indicate it is not ready. Any adapter that continues to issue an adapter ID of hex 0000 (not ready) for more than 1 second is considered defective. On the Model 50, if the channel reset was caused by a keyboard sequence or a program routine, this time is reduced to 740 milliseconds.

Central Arbiter

The central arbitration control point gives intelligent subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. This arbiter supports up to 16 arbitrating devices.

Arbitration Bus Priority Assignments

The following figure shows the assignment of arbitration levels. The functions with the lowest arbitration level have the highest priority.

ARB Level	Primary Assignment
-2	Memory Refresh
-1	NMI
0	DMA Channel 0 (Programmable to any arbitration level)
1	DMA Channel 1
2	DMA Channel 2
3	DMA Channel 3
4	DMA Channel 4 (Programmable to any arbitration level)
5	DMA Channel 5
6	DMA Channel 6
7	DMA Channel 7
8-E	Available
F	System Microprocessor

Figure 3-1. Arbitration Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation, and by the previous controlling master. The diskette drive controller should not be held inactive for more than 12 microseconds to prevent overrun.

NMI service is executed at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal (ARB/-GNT)) is in the arbitrate state.

When the central arbitration control point receives a level -1 request (NMI, a system-board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level -1 request, and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following figures.

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Mask
5	Enable Extended Arbitration
4 - 0	Reserved

Figure 3-2. Arbitration Register, Write to Hex 0090

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Masked by NMI
5	Bus Time-out
4	Reserved
3 - 0	Value of Arbitration Bus During Previous Grant State

Figure 3-3. Arbitration Register, Read Hex 0090

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 enables extended arbitration. The minimum arbitration cycle is 300 nanoseconds; this bit extends that minimum cycle to 600 nanoseconds. This bit is set to 0 during a system reset.

Reading this bit as a 1 indicates that a bus time-out has occurred, and resets bit 6 in this register to 0.

Bit 4 This bit is reserved and should be 0.

Bits 3 - 0 These bits are undefined for a write operation and should be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Memory

The Model 50 system uses the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- Real-time Clock and CMOS RAM.

Read-Only Memory Subsystem

The ROM subsystem on the Type 1 system board consists of four 32Kb by 8-bit modules in a 64Kb by 16-bit arrangement (Kb equals 1024 bits). The ROM subsystem on the Type 2 system board consists of two 64Kb by 8-bit modules in a 64Kb by 16-bit arrangement.

ROM is not parity-checked and is assigned addresses at the top of the first and last 1MB of address space (hex 0E0000 and FE0000).

Random Access Memory Subsystem

The RAM subsystem on the system board starts at address hex 000000 of the 16MB address space. It consists of 1MB of RAM modules.

The Type 1 system board uses two, 512KB by 9-bit memory module packages that operate with one wait state. The Type 2 system board supports the following memory module packages:

- 1MB, 120 nanosecond (one wait state)
- 1MB, 85 nanosecond (zero wait state)
- 2MB, 85 nanosecond (zero wait state).

Memory-refresh typically occurs once every 15 microseconds.

The timing of the memory signals on the Type 1 system board is similar to the Hitachi** HB61009BR-15, 150-nanosecond DRAM or equivalent.

** Hitachi is a trademark of the Hitachi Corporation.

The timing of the memory signals on the Type 2 system board with 85-nanosecond memory installed is similar to the Hitachi HM51256CP-8, 85-nanosecond DRAM or equivalent. The timing of the memory signals on the Type 2 system board with 120-nanosecond memory installed is similar to the Hitachi HM51256CP-12, 120-nanosecond DRAM or equivalent.

System Memory Maps

The following figure shows the mapping of the memory locations on the Model 50. A 256-byte portion of this RAM is reserved as a BIOS data area. A 1KB portion of this RAM is reserved as an extended BIOS data area. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for details.

Hex Range	Function
000000 to 09FFFF	640KB System Board RAM *
0A0000 to 0BFFFF	128KB Video RAM
0C0000 to 0DFFFF	128KB I/O Expansion ROM
0E0000 to 0FFFFF	128KB System Board ROM
100000 to 15FFFF	384KB System Board RAM
160000 to FDFFFF	Channel Expansion Memory Addresses
FE0000 to FFFFFF	128KB System Board ROM

* With the system board in the setup mode, the system board memory can be disabled through System Board POS Register 3 (see page 2-9).

Figure 3-4. System Memory Map

System Board Memory Connector

The Type 1 and 2 system boards use different types of memory connectors. The Type 1 system board has two 30-pin connectors and comes with two 512KB memory module packages installed. The Type 2 system board has one 72-pin connector and comes with one 1MB memory module package installed. The following figures show the pin assignments and signal definitions for these connectors.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	5 Vdc	2	I	-Column Address Strobe
3	I/O	Data Bit 1	4	I	Address Bit 1
5	I	Address Bit 2	6	I/O	Data Bit 2
7	I	Address Bit 3	8	I	Address Bit 4
9	N/A	Ground	10	I/O	Data Bit 3
11	I	Address Bit 5	12	I	Address Bit 6
13	I/O	Data Bit 4	14	I	Address Bit 7
15	I	Address Bit 8	16	I/O	Data Bit 5
17	I	Address Bit 9	18	N/A	No Connection
19	I	Row Address Strobe 1	20	I/O	Data Bit 6
21	I	-Write Strobe	22	N/A	Ground
23	I/O	Data Bit 7	24	O	Presence Detect
25	I/O	Data Bit 8	26	O	Presence Detect
27	I	Row Address Strobe	28	N/A	No Connection
29	I/O	Data Bit 9 (Parity)	30	N/A	+5 Vdc

Figure 3-5. System Board Memory Connector, Type 1

Type 2 Memory Connector

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Ground	37	I/O	Parity Data 1
2	I/O	Data 0	38	I/O	Parity Data 3
3	I/O	Data 16	39	N/A	Ground
4	I/O	Data 1	40	O	Column Address Strobe 0
5	I/O	Data 17	41	O	Column Address Strobe 2
6	I/O	Data 2	42	O	Column Address Strobe 3
7	I/O	Data 18	43	O	Column Address Strobe 1
8	I/O	Data 3	44	O	Row Address Strobe 0
9	I/O	Data 19	45	O	Row Address Strobe 1
10	O	+5 Vdc	46	O	Block Select 1
11	O	-Column Address Strobe P	47	O	Write Enable
12	O	Address 0	48	N/A	Reserved
13	O	Address 1	49	I/O	Data 8
14	O	Address 2	50	I/O	Data 24
15	O	Address 3	51	I/O	Data 9
16	O	Address 4	52	I/O	Data 25
17	O	Address 5	53	I/O	Data 10
18	O	Address 6	54	I/O	Data 26
19	N/A	Reserved	55	I/O	Data 11
20	I/O	Data 4	56	I/O	Data 27
21	I/O	Data 20	57	I/O	Data 12
22	I/O	Data 5	58	I/O	Data 28
23	I/O	Data 21	59	O	+5 Vdc
24	I/O	Data 6	60	I/O	Data 29
25	I/O	Data 22	61	I/O	Data 13
26	I/O	Data 7	62	I/O	Data 30
27	I/O	Data 23	63	I/O	Data 14
28	O	Address 7	64	I/O	Data 31
29	O	Block Select 0	65	I/O	Data 15
30	O	+5 Vdc	66	O	Block Select 2
31	O	Address 8	67	I	Presence Detect 0
32	N/A	Reserved	68	I	Presence Detect 1
33	O	Row Address Strobe 3	69	I	Presence Detect 2
34	O	Row Address Strobe 2	70	I	Presence Detect 3
35	I/O	Parity Data 2	71	O	Block Select 3
36	I/O	Parity Data 0	72	N/A	Ground

Figure 3-6. System Board Memory Connector, Type 2

The 'presence detect' signals are used by the system to determine memory card size and memory speed. The pins are either connected to ground (G) or not connected (N). The following table shows those combinations supported by Model 50.

Type of Memory Module Package	Presence Detect Signals			
	0	1	2	3
1 MB Memory at 120 ns	G	N	N	N
1 MB Memory at 85 ns	G	N	N	G
2 MB Memory at 85 ns	N	G	N	G

Figure 3-7. Presence Detect Encoding

Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM

The real-time clock/complementary metal-oxide semiconductor RAM (RT/CMOS) chip contains the real-time clock and 64 bytes of CMOS RAM. The internal clock circuitry uses 14 bytes of this memory, and the rest is allocated to configuration and system status information.

A 6-Vdc lithium battery maintains voltage to the RT/CMOS RAM when the power supply is not in operation.

The system cover can be locked to prevent battery removal and loss of password and configuration information.

The following figure shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000 - 00D	Real-Time Clock Bytes
00E	Diagnostic Status Byte
00F	Shutdown Status Byte
010	Diskette Drive Type Byte
011	First Fixed Disk Drive Type Byte
012	Second Fixed Disk Drive Type Byte
013	Reserved
014	Equipment Byte
015 - 016	Low and High Base Memory Bytes
017 - 018	Low and High Expansion Memory Bytes
019 - 031	Reserved
032 - 033	Configuration CRC Bytes
034	Reserved
035 - 036	Low and High Useable Memory Bytes
037	Date Century Byte
038 - 03F	Reserved

Figure 3-8. RT/CMOS RAM Address Map

RT/CMOS Address Register and NMI Mask (Hex 0070)

This register is used in conjunction with the port at hex 0071 to read and write the RT/CMOS RAM bytes.

Bit	Function
7	NMI Mask
6	Reserved
5 - 0	RT/CMOS RAM Address

Figure 3-9. RT/CMOS Address Register and NMI Mask (Hex 0070)

Warning: The operation following a write to hex 0070 should access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Bit 7 When this bit is set to 1, the NMI is masked off (the NMI is disabled). This bit is set to 1 by a power-on reset and is a write-only bit.

Bit 6 Reserved.

Bits 5 - 0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This port is used in conjunction with the address register at hex 0070 to read and write the RT/CMOS RAM bytes.

Bit	Function
7 - 0	RT/CMOS Data

Figure 3-10. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts should be masked to prevent other interrupt service routines from changing the CMOS address register before data is read or written. After I/O operations, the RT/CMOS and NMI Mask register (hex 0070) should be left pointing to Status Register D (hex 00D).

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

The following steps are required to perform I/O operations to the RT/CMOS RAM addresses:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Write the data to address hex 0071.

Reading RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Read the data from address hex 0071.

Real-Time Clock Bytes (Hex 000-00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following figure.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second Alarm	1
002	Minutes	2
003	Minute Alarm	3
004	Hours	4
005	Hour Alarm	5
006	Day of Week	6
007	Date of Month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-11. Real-Time Clock Bytes

Note: The Setup program initializes status registers A, B, C, and D when the time and date are set. Interrupt hex 1A is the BIOS interface to read and set the time and date and it initializes the register the same way as the Setup program.

Status Register A (Hex 00A)

Bit	Function
7	Update in Progress
6 - 4	22-Stage Divider
3 - 0	Rate Selection Bits

Figure 3-12. Status Register A

Bit 7 When set to 1, this bit indicates the time-update cycle is in progress. When set to 0, it indicates the current date and time can be read.

Bits 6 - 4 These three divider-selection bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768 kHz time-base. This is the only value supported by the system for proper time-keeping.

Bits 3 - 0 These bits allow the selection of a divider output frequency. The system initializes the rate selection bits to a binary 0110, which selects a 1.024 kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Periodic Interrupt Enable
5	Alarm Interrupt Enable
4	Update-Ended Interrupt Enabled
3	Square Wave Enabled
2	Date Mode
1	24-Hour Mode
0	Daylight Savings Enabled

Figure 3-13. Status Register B

Bit 7 When set to 0, this bit updates the cycle, normally by advancing the counts at a rate of one per second. When set to 1, this bit immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This bit is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

Bit 5 When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit indicates if the time-and-date calendar updates use binary or binary-coded-decimal (BCD) formats. When set to 1, this bit indicates a binary format. The system initializes this bit to 0.

Bit 1 This bit establishes if the hours byte is in the 24-hour or 12-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When set to 1, this bit enables the daylight savings time mode. When set to 0, it disables the mode, and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt Request Flag
6	Periodic Interrupt Flag
5	Alarm Interrupt Flag
4	Update-Ended Interrupt Flag
3 - 0	Reserved

Figure 3-14. Status Register C

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 This bit is used in conjunction with bits 6, 5, and 4. When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When set to 1, this bit indicates that a periodic interrupt occurred.

Bit 5 When set to 1, this bit indicates that an alarm interrupt occurred.

Bit 4 When set to 1, this bit indicates that an update-ended interrupt occurred.

Bits 3 - 0 Reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6 - 0	Reserved

Figure 3-15. Status Register D

Bit 7 This read-only bit monitors the power-sense pin. A low state of this pin indicates a loss of power to the real-time clock (dead battery). When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power.

Bits 6 - 0 Reserved.

CMOS RAM Configuration

The following shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-Time Clock Chip Power
6	Configuration Record and Checksum Status
5	Incorrect Configuration
4	Memory Size Miscompare
3	Fixed Disk Controller/Drive C Initialization Status
2	Time Status Indicator
1	Adapter Configuration Miscompare
0	Adapter ID Time-Out

Figure 3-16. Diagnostic Status Byte

Bit 7 When set to 1, this bit indicates the real-time clock chip lost power.

Bit 6 When this bit is set to 1, the checksum is incorrect.

Bit 5 This is a check, at power-on time, of the Equipment byte. When set to 1, the configuration information is incorrect. Power-on checks require that at least one diskette drive be installed (bit 0 of the Equipment byte, hex 014, is set to 1).

Bit 4 When set to 1, this bit indicates the power-on check determined that the memory size is not the same as in the configuration record.

Bit 3 When set to 1, this bit indicates that the controller or drive C failed initialization, which prevents the system from attempting a power-on reset.

Bit 2 When set to 0, this bit indicates the time is valid. When set to 1, this bit indicates the time is invalid.

Bit 1 This bit indicates if the installed adapters match the configuration information. When this bit is set to 1, the adapters do not match the configuration information.

Bit 0 When set to 1, this bit indicates a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7 - 4	First Diskette Drive Type
3 - 0	Second Diskette Drive Type

Figure 3-17. Diskette Drive Type Byte

Bits 7 - 4 These bits indicate the first diskette drive type, as shown in the following figure.

Bits 7 6 5 4	Function
0 0 0 0	No drive present
0 0 0 1	Double-sided diskette drive (48 tracks per inch, 360KB)
0 0 1 1	High-capacity diskette drive (720KB)
0 1 0 0	High-density diskette drive (1.44MB)

All combinations that are not shown are reserved.

Figure 3-18. Diskette Drive Type Byte (Bits 7 - 4)

Bits 3 - 0 These bits indicate the second diskette drive type, as shown in the following figure.

Bits 3 2 1 0	Function
0 0 0 0	No drive present
0 0 0 1	Double-sided diskette drive (48 tracks per inch, 360KB)
0 0 1 1	High-capacity diskette drive (720KB)
0 1 0 0	High-density diskette drive (1.44MB)

All combinations that are not shown are reserved.

Figure 3-19. Diskette Drive Type Byte (Bits 3 - 0)

First Fixed Disk Drive Type Byte (Hex 011): This byte defines the type of the first fixed disk drive (drive C). Hex 00 indicates that a fixed disk drive is *not* installed.

Second Fixed Disk Drive Type Byte (Hex 012): This byte defines the type of the second fixed disk drive (drive D). Hex 00 indicates that a fixed disk drive is *not* installed.

Note: For more information about fixed disk drive types, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Reserved Byte (Hex 013): This byte is reserved.

Equipment Byte (Hex 014): The equipment byte defines the basic equipment in the system for the power-on diagnostic tests.

Bit	Function
7, 6	Number of Diskette Drives
5, 4	Display Operating Mode
3, 2	Reserved
1	Math Coprocessor Presence
0	Diskette Drive Presence

Figure 3-20. Equipment Byte

Bits 7, 6 These bits indicate the number of diskette drives installed, as shown in the following figure.

Bits 7 6	Number of Diskette Drives
0 0	One Drive
0 1	Two Drives
1 0	Reserved
1 1	Reserved

Figure 3-21. Equipment Byte (Bits 7, 6)

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port, as shown in the following figure.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-Column Mode
1 0	80-Column Mode
1 1	Monochrome Mode

Figure 3-22. Equipment Byte (Bits 5, 4)

Bits 3, 2 Reserved.

Bit 1 When set to 1, this bit indicates that a math coprocessor is installed.

Bit 0 When set to 1, this bit indicates that a diskette drive is installed.

Low and High Base Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 is equal to 640KB. The low byte is hex 15; the high byte is hex 16.

Low and High Expansion Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The hexadecimal values in these bytes represent the number of 1KB blocks of expansion memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 17; the high byte is hex 18.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 33; the high byte is hex 32.

| ***Reserved Byte (Hex 034):*** This byte is reserved.

| ***Low and High Useable Memory Bytes (Hex 035 and 036):*** These
| bytes define the total amount of useable memory above the 1MB
| address space.

| The hexadecimal values in these bytes represent the number of 1KB
| blocks of useable memory. For example, hex 0800 is equal to
| 2048KB. The low byte is hex 35; the high byte is hex 36.

Date Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 through 03F): These bytes are reserved.

Miscellaneous System Functions

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system Watchdog time-out has occurred. The NMI stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts and the IRET instruction restores the interrupt flag to the state it was in prior to the interrupt. A system reset causes a reset of the NMI.

Nonmaskable interrupt requests from system board parity and channel check are subject to mask control with the NMI mask bit in the RT/CMOS Address register. The Watchdog Timer and system channel time-out are not masked by this bit. (See "RT/CMOS RAM I/O Operations" on page 3-14). The power-on default of the NMI mask is 1 (NMI disabled). Prior to enabling the NMI after a power-on reset, the parity check and channel check state are initialized by the POST.

Warning: The operation following a write to hex 0070 should access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the read and write functions of this port are shown in the following figures.

Bit	Function
7	Reset Timer 0 Output Latch (IRQ0)
6 - 4	Reserved
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-23. System Control Port B (Write)

Bit	Function
7	Parity Check
6	Channel Check
5	Timer 2 Output
4	Toggle with Each Refresh Request
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-24. System Control Port B (Read)

Bit 7 Setting this bit to 1 during a write operation, resets IRQ 0. When this port is read and this bit is set to 1, a parity check has occurred.

Bit 6 When this port is read and this bit is set to 1, a channel check has occurred.

Bit 5 When this port is read, this bit indicates the condition of the timer/counter 2 'output' signal.

Bit 4 When this port is being read, this bit toggles for each refresh request.

Bit 3 Setting this bit to 0 enables channel check. It is set to 1 during a power-on reset.

Bit 2 Setting this bit to 0 enables parity checking. This bit is set to 1 during a power-on reset.

Bit 1 Setting this bit to 1 enables speaker data. This bit is set to 0 during a power-on reset.

Bit 0 Setting this bit to 1 enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7, 6	Fixed Disk Activity Light
5	Reserved
4	Watchdog Timer Status
3	Security Lock Latch
2	Reserved
1	Alternate Gate A20
0	Alternate Hot Reset

Figure 3-25. System Control Port A (Hex 0092)

Bits 7, 6 These bits control the fixed-disk activity light. Setting either bit to 1 turns the fixed-disk activity light on. Setting both bits to 0 turns the light off. The power-on reset condition of each bit is 0.

Bit 5 Reserved.

Bit 4 This read-only bit indicates the Watchdog Timer status. When this bit is set to 1, a Watchdog time-out has occurred. For more information about the Watchdog Timer, refer to the *Hardware Interface Technical Reference — Architectures* manual.

Bit 3 This bit provides the security lock for the secured area of RT/CMOS. Setting this bit to 1 electrically locks the 8-byte, power-on password. Once this bit is set by POST, it can only be cleared by turning the system off.

Bit 2 Reserved.

Bit 1 This bit is used to enable the 'address 20' signal (A20) when the microprocessor is in the real address mode. When this bit is set to 0, A20 cannot be used in real mode addressing. This bit is set to 0 during a system reset.

Bit 0 This bit provides an alternate method of resetting the system microprocessor. This alternate method supports operating systems requiring faster operation than was provided on the IBM Personal Computer AT*. Resetting the system microprocessor is used to switch the microprocessor from the protected mode to the real address mode. The alternate reset takes 13.4 microseconds.

This bit is set to 0 either by a system reset or a Write operation. When a Write operation changes this bit from 0 to 1, the alternate reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is 0, POST assumes the system was just powered on. If the bit is 1, POST assumes a switch from the protected mode to the real mode has taken place.

---

* Personal Computer AT is a trademark of the International Business Machines Corporation.

Power-On Password

RT/CMOS RAM has 8 bytes reserved for the power-on password and its check character. The 8 bytes are initialized to hex 00. The microprocessor can only access these bytes during power-on self-test (POST). After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by a program. A power-on password can be from 1 to 7 characters.

During power-on password installation, the password (1 to 7 keyboard scan codes), is stored in the security space.

Power-on password installation is a function of a program contained on the Reference diskette. Once the power-on password utility has been installed, the password can be changed only during the POST. When the new power-on password is installed, changed, or removed, the password is not visible on the display.

The system unit cover can be physically locked to prevent unauthorized access to the battery. This helps prevent unauthorized battery removal and loss of power-on password and configuration information.

For information about the keyboard password, see the keyboard/auxiliary device controller information in the *Hardware Interface Technical Reference — Common Interfaces* manual.

Type 2 Serial Port Controller

The Model 50 does not support FIFO mode operations even if a Type 2 serial controller is installed. Do not enable FIFO operations if the model/submodel byte is hex FC/04.

The serial controller on some Type 2 system boards does not respond the same as other Personal System/2 products. After the initial transmitter-holding-register-empty interrupt, rewriting bit 1 of the Interrupt Enable register as a 1 will not reissue an interrupt. The interrupt is generated only when the Transmitter Holding register becomes empty.

Hardware Compatibility

The Model 50 maintains many of the interfaces used by the IBM Personal Computer AT. In most cases, command and status organization of these interfaces is maintained.

The functional interfaces for the Personal System/2 products are compatible with the following interfaces:

- The Intel** 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller-address/transfer counters, page registers and status fields only. The Command and Request registers are not supported. The rotate and mask functions are not supported. The Mode register is partially supported.
- Generally compatible with the NS16450 serial communications controller.
- The Intel 8088, 8086, and 80286 microprocessors.
- The Intel 8272 diskette drive controller.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The Intel 8042 keyboard port at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.

** Intel is a trademark of the Intel Corporation.

** Motorola is a trademark of Motorola, Incorporated.

- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.
- Generally compatible with the Intel 80287 and 8087 math coprocessors.

Notes:

Index

A

acoustic readings 1-10
activity light, fixed disk 3-26
adapter ID (0000) 3-3
adapter setup 2-4
address maps
  memory 3-8
  POS 2-5
  system 1-6
address space, POS 2-5
alternate reset 3-26
arbiter programming 3-5
arbiter refresh 3-4
arbitration level 3-4
arbitration register 3-5
arbitration, central control point 3-5
A20 gate 3-26

B

base memory bytes 3-23
battery 3-12
block diagram, system board 1-5
bus contention 2-3
bus priority assignments 3-4

C

card selected feedback 2-6
-CD SFDBK 2-6
central arbitration control point 3-5
channel-check latch 3-25
CMOS RAM 3-12
configuration CRC bytes 3-23
configuration, RT/CMOS 3-19
connectors, memory 3-9
control port B 3-24

D

date century byte 3-23
description
  programmable option select 2-3
description, power supply 1-11
diagnostic status byte (RT/CMOS) 3-19
diskette drive enable 2-9
diskette drive type byte 3-20
DMA channels 3-4

E

electrical requirements 1-9
enable I/O functions 2-8
enable NMI 3-13
enable/setup register 2-7
enable, channel check 3-25
equipment byte 3-22
extended arbitration 3-5

F

fault, overvoltage 1-12
features, system 1-4
feedback, card selected 2-6
first fixed disk type byte 3-21
fixed disk drive activity light 1-11
fixed disk drive initialization 3-19
fixed-disk activity light 3-26

G

gate A20 3-26

H

heat output 1-9

© Copyright IBM Corp. 1989, 1990

I

Identification, adapter 3-3
interrupt 0 reset 3-25
interrupts
I/O address map 1-6
I/O function byte 2-8

K

keyboard (electrical) 1-9

L

light, fixed disk drive activity 1-11
light, power 1-11

M

map, memory 3-8
math coprocessor 1-4
memory
  connectors 3-9
  control register 2-9
  map 3-8
  memory module packages 3-7
  performance 1-7
  random access 3-7
  read only 3-7
  refresh 1-7
memory refresh 3-4
memory size miscompare 3-19
microprocessor
  alternate reset 3-26
  real address mode 3-26
miscellaneous ports 3-24
mode switch compatibility 3-26
model byte 1-3
modules, memory 3-7

N

NMI mask 3-13
NMI service 3-4
NMI signal 3-4
noise readings 1-10
nonmaskable interrupt (NMI) 3-24

O

output voltage sequencing 1-12
outputs, power supply 1-11
overvoltage fault 1-12

P

parallel port 2-8
Parity check enable 3-25
password, power-on 3-27
performance, system 1-7
pointing device (electrical) 1-9
port B 3-24
POS
  See programmable option select
POS registers 2-8
power specifications 1-9
power supply description 1-11
power supply LED 1-11
power supply output
 protection 1-12
power supply outputs 1-11
programmable option select 2-3
  enable/setup register 2-7
  registers 2-5
  system board I/O byte 2-8
  system board setup 2-6
  system configuration
   utilities 2-3
programming, arbiter 3-5
protection, power supply 1-12

R

RAM enable 2-9
random access memory (RAM) 3-7
read-only memory 3-7
real mode addressing 3-26
real-time clock bytes 3-15
refresh 3-4, 3-7
refresh request 3-25
registers
  card selected feedback 2-6
  enable/setup 2-7
  memory control 2-9
  miscellaneous system 3-24

registers *(continued)*
port B 3-24
POS 2-5, 2-8
RT/CMOS and NMI mask 3-13
RT/CMOS status registers 3-16
reset, alternate 3-26
RT/CMOS address register 3-13
RT/CMOS RAM 3-12
password 3-26, 3-27
secured area 3-26

S

second fixed disk type byte 3-21
sequencing, output voltage 1-12
serial communications controller 3-28
serial port 2-8
serial port controller 3-28
setup
system board 2-6
system board I/O byte 2-8
warning 2-3
shutdown status byte 3-20
size 1-9
sound specifications 1-10
speaker data enable 3-25
specifications 1-7
status registers (RT/CMOS) 3-16
status, watchdog 3-26
switch to real mode 3-26
system address map 1-6
system board
block diagram 1-5
features 1-4
I/O address map 1-6
I/O byte 2-8
memory 3-7
memory connectors 3-9
memory enable 2-9
memory map 3-8
setup 2-4
system board setup 2-6
system configuration utilities 2-3
system control port A 3-25
system ports, miscellaneous 3-24
system reset 3-24
system unit specifications 1-7

T

time status indicator 3-19
timer status, watchdog 3-26
type 1 memory connector 3-9
type 2 memory connector 3-10

U

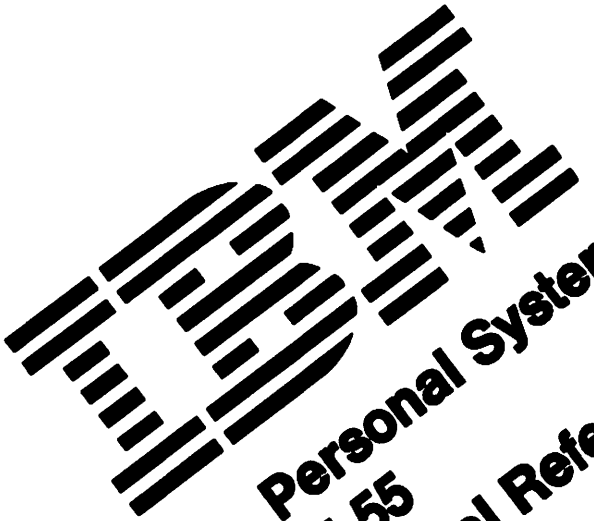
useable memory 3-23
utilities, configuration 2-3

V

valid RAM bit 3-18
video subsystem setup 2-4

W

warning, POS 2-3
watchdog status 3-26
weight 1-9



Personal System/2
Model 55
Technical Reference

Second Edition (October 1990)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer of express or implied warranties in certain transactions, therefore, this statement may not apply to you.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Requests for technical information about IBM products should be made to your IBM Authorized Dealer or your IBM Marketing Representative.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

© Copyright International Business Machines Corporation 1989, 1990. All rights reserved.

Note to U.S. Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Special Notices

References in this publication to IBM products, programs, or services do not imply that IBM intends to make these available in all countries in which IBM operates. Any reference to an IBM product, program or service is not intended to state or imply that only IBM's product, program, or service may be used. Any functionally equivalent product, program, or service that does not infringe any of IBM's intellectual property rights or other legally protectible rights may be used instead of the IBM product, program, or service. Evaluation and verification of operation in conjunction with other products, programs, or services, except those expressly designated by IBM, are the user's responsibility.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

The following terms, denoted by an asterisk (*) in this publication, are trademarks of the IBM Corporation in the United States and/or other countries:

IBM
Micro Channel
Personal Computer AT
Personal System/2
PS/2

The following terms, denoted by a double asterisk (**) in this publication, are trademarks of other companies as follows:

80387SX	Intel Corporation
Intel	Intel Corporation
National Semiconductor	National Semiconductor Corporation
Motorola	Motorola, Incorporated

Preface

This technical reference contains hardware and software interface information specific to the IBM Personal System/2 Model 55 computer. It is intended for those who develop hardware and software products for these systems. Users should understand computer architecture and programming concepts.

This publication consists of the following sections:

Section 1, "System Overview," describes the system, features and specifications.

Section 2, "Programmable Option Select," describes registers used for configuration.

Section 3, "System Board," describes the system specific hardware implementations.

This technical reference should be used with the following publications:

IBM Personal System/2 Hardware Interface Technical Reference — Architectures

IBM Personal System/2 Hardware Interface Technical Reference — Common Interfaces

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference

These publications contain additional information on many of the subjects discussed in this technical reference.

Warning: The term "Reserved" describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

© Copyright IBM Corp. 1989, 1990

Contents

Section 1. System Overview 1-1
Description 1-3
System Board Features 1-3
System Board I/O Address Map 1-5
Specifications 1-6
| Power Supply 1-9
| Outputs 1-9
| Output Protection 1-10
| Voltage Sequencing 1-10

Section 2. Programmable Option Select 2-1
Description 2-3
System Board POS Address Map 2-5
Card Selected Feedback 2-6
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-7
System Board POS Register 2 (Hex 0102) 2-8
System Board POS Register 3 (Hex 0103) 2-9
System Board POS Register 4 (Hex 0104) 2-9
System Board POS Register 5 (Hex 0105) 2-10
Adapter Setup 2-11

Section 3. System Board 3-1
Description 3-3
Microprocessor and Math Coprocessor 3-3
| Micro Channel Implementation 3-3
| Exception Reporting 3-3
Central Arbiter 3-3
Bus Adapter 3-6
Diskette Drive Controller 3-8
Memory 3-9
ROM Subsystem 3-9
RAM Subsystem 3-9
Error Recovery 3-10
System Memory Map 3-11
System Board Memory Connectors 3-12
| RT/CMOS RAM 3-13
Miscellaneous System Functions and Ports 3-22
Nonmaskable Interrupt 3-22
System Control Port B (Hex 0061) 3-23
System Control Port A (Hex 0092) 3-24
Power-On Password 3-26

© Copyright IBM Corp. 1989, 1990

Type 2 Serial Port Controller 3-26
Hardware Compatibility 3-27

Index X-1

Figures

1-1. Model and Submodel Bytes 1-3
1-2. System Board Devices and Features 1-4
1-3. System Board I/O Address Map 1-5
1-4. Performance Specifications 1-6
1-5. Physical Specifications 1-7
1-6. Acoustical Readings 1-8
1-7. Component Maximum Current 1-9
1-8. Channel Load Current 1-9
2-1. System Board POS I/O Address Map 2-5
2-2. Card Selected Feedback Register (Hex 0091) 2-6
2-3. System Board Enable/Setup Register (Hex 0094) 2-7
2-4. System Board POS Register 2 (Hex 0102) 2-8
2-5. Parallel Port Select Bits 2-8
2-6. System Board POS Register 3 (Hex 0103) 2-9
2-7. System Board POS Register 4 (Hex 0104) 2-9
2-8. Memory Card ID Bits 2-10
2-9. System Board POS Register 5 (Hex 0105) 2-10
2-10. Memory Connector Select for POS Register 4 2-11
2-11. Adapter Enable/Setup Register (Hex 0096) 2-11
3-1. Arbitration Bus Priority Assignments 3-4
3-2. Arbitration Register, Write to Hex 0090 3-5
3-3. Arbitration Register, Read Hex 0090 3-5
3-4. Fixed Disk Drive Connector 3-6
3-5. Diskette Drive Connector 3-8
3-6. Memory Error Address Reassignment 3-10
3-7. System Memory Map 3-11
3-8. System Board Memory Connectors 3-12
3-9. RT/CMOS RAM Address Map 3-13
3-10. RT/CMOS Address and NMI Mask Register (Hex 0070) 3-13
3-11. RT/CMOS Data Register (Hex 0071) 3-14
3-12. Real-Time Clock Bytes 3-15
3-13. Status Register A 3-16
3-14. Status Register B 3-16
3-15. Status Register C 3-17
3-16. Status Register D 3-18
3-17. Diagnostic Status Byte 3-18
3-18. Diskette Drive Type Byte 3-19
3-19. Diskette Drive Type Bits 3-19
3-20. Equipment Byte 3-20
3-21. Installed Diskette Drive Bits 3-20
3-22. Display Operating Mode Bits 3-20
3-23. System Control Port B (Write) 3-23

© Copyright IBM Corp. 1989, 1990

3-24. System Control Port B (Read) 3-23
3-25. System Control Port A 3-24

Section 1. System Overview

Description 1-3
System Board Features 1-3
System Board I/O Address Map 1-5
Specifications 1-6
| Power Supply 1-9
| Outputs 1-9
| Output Protection 1-10
| Voltage Sequencing 1-10

© Copyright IBM Corp. 1989, 1990

Notes:

Description

The IBM* Personal System/2* Model 55 is a desktop computer that features the Micro Channel* architecture. It comes with a keyboard, and can support one internal diskette drive and one internal fixed disk drive.

The system can have either a Type 1 and Type 2 system board. The Type 2 system board contains additional memory for configuration information.

Programs can identify the system board by reading the model and submodel bytes. Interrupt hex 15, function code (AH) = hex C0, returns the model byte, submodel byte, and BIOS revision code. The following table lists the model and submodel bytes, the system board types, and the system clock speed for the two Model 55 system boards.

Model Byte	Submodel Bytes	System Clock	System Board Type
F8	0C	16 MHz	Type 1
F8	1E	16 MHz	Type 2

Figure 1-1. Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* and its supplements for a listing of other systems.

System Board Features

The following figure lists the system board devices and features. The *IBM Personal System/2 Hardware Interface Technical Reference* manuals describe devices common to PS/2* products by type number.

* IBM, Personal System/2, PS/2, and Micro Channel are trademarks of the International Business Machines Corporation.

Device	Type	Features
Microprocessor	—	80386SX** 24-bit address and 16-bit data interface
System Timers	1	Channel 0 – System timer Channel 2 – Tone generation for speaker Channel 3 – Watchdog timer
ROM Subsystem	—	128KB (KB = 1024 bytes)
RAM Subsystem	—	1 to 8MB (MB = 1,048,576 bytes) Expandable on the channel to 16MB
CMOS RAM Subsystem	—	64-byte CMOS RAM with real-time clock, calendar, and battery Type 2 system board also has a 2KB CMOS RAM extension with battery
Video Subsystem	1	Auxiliary connector on the channel Analog output 256KB video memory
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal.
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	1	Supports: - 1.44MB formatted diskette density - 720KB formatted diskette density.
Serial Controller	2	RS-232C interface Programmable as serial port 1 or 2 FIFO mode* and character mode
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output
Micro Channel Bus Adapter	—	Four channel connectors for Type 3 adapters: - One 16-bit connector with an auxiliary video extension - Two 16-bit connectors - One 2- by 36-pin card edge connector for the fixed disk drive.
Math Coprocessor Socket	—	Supports 80387SX** math coprocessor option Same clock speed as the system microprocessor

* The Model 55 supports FIFO through ABIOS calls only.

Figure 1-2. System Board Devices and Features

** Trademark of the Intel Corporation.

System Board I/O Address Map

Address (Hex)	Device
0000 - 001F	DMA Controller (0–3)
0020, 0021	Interrupt Controller (Master)
0040, 0042 - 0044, 0047	System Timers
0060	Keyboard, Auxiliary Device
0061	System Control Port B
0064	Keyboard, Auxiliary Device
0070, 0071	RT/CMOS and NMI Mask
0081 - 0083, 0087	DMA Page Registers (0–3)
0089 - 008B, 008F	DMA Page Registers (4–7)
0090	Central Arbitration Control Point
0091	Card Selected Feedback Register
0092	System Control Port A
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
00A0, 00A1	Interrupt Controller (Slave)
00C0 - 00DF	DMA Controller (4–7)
00E0, 00E1	Reserved
00F0 - 00FF	Math Coprocessor
0100 - 0107	Programmable Option Select
01F0 - 01F8	Fixed Disk Drive Controller
0278 - 027B	Parallel Port 3
02F8 - 02FF	Serial Port 2 (RS-232C)
0378 - 037B	Parallel Port 2
03B4, 03B5, 03BA	Video Subsystem
03BC - 03BF	Parallel Port 1
03C0 - 03C5	Video Subsystem
03C6 - 03C9	Video DAC
03CA, 03CC, 03CE, 03CF	Video Subsystem
03D4, 03D5, 03DA	Video Subsystem
03F0 - 03F7	Diskette Drive Controller
03F8 - 03FF	Serial Port 1 (RS-232C)

Figure 1-3. System Board I/O Address Map

Specifications

Device	Number of Waits	Cycle Time (ns)
Microprocessor (16 MHz – 62.5 ns Clock)		
Access to System Board RAM: *		
Memory Read (Page Hit)	0	125
Memory Read (Anticipated Page Miss)	1	187.5
Memory Read (Page Miss)	2	250
Memory Write (Page Hit)	1	187.5
Memory Write (Anticipated Page Miss)	1	187.5
Memory Write (Page Miss)	2	250
Access to Channel:		
Default Transfer Cycle	2	250
Synchronous Transfer Cycle	4	375
Access to ROM	3	312
Refresh Rate (typically performed every 15.1 μs)		625 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (8 MHz – 125 ns Clock):		
Single Transfer: 375 + (I/O Access + Memory Access)		
Burst Transfer: 375 + (I/O Access + Memory Access)N **		
System Board Memory Access		375
Default Transfer Cycle		250
Synchronous Transfer Cycle		375

* Adapters installed in the channel should not rely on monitoring system board memory access, because channel memory control signals may not be present during these accesses.

** N is the number of transfers in the burst.

Note: The cycle times shown for access to system board RAM is based on 85- or 100-nanosecond memory.

Figure 1-4. Performance Specifications

The following figure describes the physical specifications of the system.

Size	
Width	406 mm (16.0 in.)
Depth	397 mm (15.6 in.)
Height	102 mm (4.0 in.)
Weight with DASD	8.64 kg (19 lb)
Cables:	
Power Cable	1.8 m (6 ft)
Keyboard Cable	1.8 m (6 ft)
Air Temperature:	
System On	15.6 to 32.2°C (60 to 90°F)
System Off	10.0 to 43.0°C (50 to 110°F)
Humidity:	
System On	8% to 80%
System Off	8% to 80%
Maximum Altitude	2133.6 m (7000 ft)
Heat Output	140 Watts(480 BTUs/hour)
Acoustical Readings	See Figure 1-6 on page 1-8
Electrical:	
Input Voltage (Range is switch selected; sinewave input is required)	
Low Range	90 (min) – 137 (max) Vac
High Range	180 (min) – 265 (max) Vac
Frequency	50 ± 3Hz/60 ± 3Hz
Input in Kilovolt-Ampere (kVA):	
Minimum Configuration (as shipped by IBM)	0.08 kVa
Maximum Configuration	0.24 kVa
Electromagnetic Compatibility	FCC Class B

Figure 1-5. Physical Specifications

Description	L_{WAd} in bels Operate	Idle	L_{pAm} in dB Operate	Idle	$<L_{pA}>_m$ in dB Operate	Idle
Model 55	5.0	4.7	43	43	40	40

Notes:

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

All measurements made in accordance with ANSI S12.10, and reported in conformance with ISO DIS 9296.

The measurements are preliminary data and subject to change.

Figure 1-6. Acoustical Readings

Power Supply

The power supply converts the ac input voltage to three dc outputs and provides power for the following:

- System board
- Channel adapters
- Internal DASD drives
- Auxiliary device
- Keyboard.

Outputs

The power supply provides separate voltage sources for the system board and the drives. The system-board voltages are +5 Vdc, +12 Vdc, and −12 Vdc. The drive voltages are +5 Vdc and +12 Vdc. The following is a list of the approximate power provided for system components.

System Component	Maximum Current	
	+12 Vdc	+5 Vdc
Internal Fixed Disk Drive (per power supply connector)	0.8 A	0.8 A
Auxiliary Device	None	300 mA
Keyboard	None	275 mA

Figure 1-7. Component Maximum Current

The following are the load currents allowed for each channel connector.

Supply Voltage	Maximum Current
+ 5.0 Vdc	1.6 A
+12.0 Vdc	0.175 A
−12.0 Vdc	0.040 A

Figure 1-8. Channel Load Current

The formulas used to determine the power requirements and the voltage regulation tolerances are in the Micro Channel adapter design information in the *Hardware Interface Technical Reference - Architectures* manual.

Output Protection

A short circuit placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state with no damage to the power supply.

If an overvoltage fault occurs (internal to the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of its nominal value.

If either of these shutdown states is actuated, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least ten seconds.

Voltage Sequencing

At power-on time, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Section 2. Programmable Option Select

Description 2-3
System Board POS Address Map 2-5
Card Selected Feedback 2-6
System Board Setup 2-6
  System Board Enable/Setup Register (Hex 0094) 2-7
  System Board POS Register 2 (Hex 0102) 2-8
  System Board POS Register 3 (Hex 0103) 2-9
  System Board POS Register 4 (Hex 0104) 2-9
    4MB Memory Cards 2-10
    1MB and 2MB Memory Cards 2-10
  System Board POS Register 5 (Hex 0105) 2-10
Adapter Setup 2-11

© Copyright IBM Corp. 1989, 1990

Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used on the Model 55 system board. For additional POS information, refer to the *IBM Personal System/2 Hardware Interface Technical Reference*.

Warning:

- IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignments of the same system resource, improper operation of the feature, loss of data, or damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention occurs, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- The channel reset bit (bit 7) in the Adapter Enable/Setup register (hex 0096) must be 0 to program the adapters.
- The system board does not support 16-bit I/O operations to 8-bit POS registers. Using 16-bit I/O instructions on 8-bit POS registers causes incorrect data to be written to or read from the registers. Only 8-bit transfers are supported for setup operations.

Setup functions respond to I/O addresses hex 0100 through 0107 only when their unique setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

System Board Video Subsystem Setup:

- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 0 to place the system board video into the setup mode.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 7 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system board functions.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register must be set to 1 to allow adapter setup.
- Bit 5 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem.
- Bit 7 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to a system board function.

Other System Board Setup:

- Bit 7 in the System Board Enable/Setup register must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 5 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem.

System Board POS Address Map

The following figure shows the organization of the I/O address space used by system board POS.

Address (Hex)	Function
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
0100	POS Register 0—Reserved
0101	POS Register 1—Reserved
0102	POS Register 2—System Board I/O Register
0103	POS Register 3—Memory Enable Register
0104	POS Register 4—Memory Presence Register
0105	POS Register 5—Memory Control Register
0106	POS Register 6—Reserved
0107	POS Register 7—Reserved

Figure 2-1. System Board POS I/O Address Map

Card Selected Feedback

Whenever an adapter is addressed, it responds by setting the '-card selected feedback' (-CD SFDBK) signal to active. -CD SFDBK is derived from the address decode, driven by a totem-pole driver, and latched by the system board. It can be read through the Card Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs can use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and determine if the video subsystem, system board I/O, or an adapter is addressed and functioning.

Bit	Function
7 - 1	Reserved
0	Card Selected Feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7 - 1 Reserved.

Bit 0 This bit is set to 1 whenever -CD SFDBK was active on a previous cycle or whenever the system board I/O functions (diskette drive, serial, or parallel interfaces) are accessed by an I/O cycle. Reading this register resets the bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information during setup. The diskette drive controller, serial port, and parallel port are treated as a single device. The video subsystem also is an integrated part of the system board, but POS treats it as a separate device. The System Board Enable/Setup register is used to place the system board or the video subsystem in the setup mode.

System Board Enable/Setup Register (Hex 0094)

This is a read/write register. All bits in this register default to 1 (enabled).

Bit	Function
7	Enable/-Setup System Board Functions
6	Reserved
5	Enable/-Setup Video Subsystem
4 - 0	Reserved

Figure 2-3. System Board Enable/Setup Register (Hex 0094)

Bit 7 When set to 0, this bit places various system board I/O functions in the setup mode. The diskette drive controller, serial port, and parallel port are controlled through System Board POS Register 2 (hex 0102). The POS information for memory is in System Board POS Register 3 (hex 0103), POS Register 4 (hex 0104), and POS Register 5 (hex 0105).

When set to 1, this bit enables the system board functions.

Bit 6 Reserved.

Bit 5 When this bit is set to 0, the video subsystem is placed in the setup mode and controlled through POS Register 2 (hex 0102). When this bit is set to 1 and bit 0 in POS Register 2 is set to 1, video is enabled.

Bit 0 of POS Register 2 is the video enable bit. When this bit is set to 0, the video subsystem does not respond to commands, addresses, or data. If video is being generated when the video enable bit is set to 0, the output is still generated. For information on BIOS calls to enable or disable the video, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Note: When video is disabled, access to the digital-to-analog converter (DAC) registers is disabled.

Bits 4 - 0 Reserved.

System Board POS Register 2 (Hex 0102)

When the system board is in the setup mode, this read/write register controls the diskette drive controller, serial port, and parallel port. Reading this register returns the current state of the following system board functions.

Bit	Function
7	Disable Parallel Port Extended Mode
6, 5	Parallel Port Select
4	Enable Parallel Port
3	Serial Port Select
2	Enable Serial Port
1	Enable Diskette Drive Interface
0	Enable System Board

Figure 2-4. System Board POS Register 2 (Hex 0102)

Bit 7 When set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional interface. When set to 1, this bit disables the bidirectional mode. This bit is set to 0 at power-on time, and the power-on self-test (POST) sets it to 1.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Address (Hex)	Interrupt Level
0 0	Parallel 1	03BC - 03BF	7
0 1	Parallel 2	0378 - 037B	7
1 0	Parallel 3	0278 - 027B	7
1 1	Reserved	----------	-

Figure 2-5. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bit 3 When set to 1, this bit sets the system board serial port as Serial 1 (addresses hex 03F8 through 03FF), which uses interrupt level 4. When set to 0, this bit sets the serial port as Serial 2 (addresses hex 02F8 through 02FF), which uses interrupt level 3.

Bit 2 When this bit and bit 0 are set to 1, the system board serial port is enabled.

Bit 1 When this bit and bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When set to 1, this bit allows bits 4, 2, and 1 to enable and disable their respective devices. When set to 0, this bit disables the system board parallel port, the system board serial port, and the diskette drive interface, regardless of the state of bits 4, 2, and 1.

System Board POS Register 3 (Hex 0103)

When the system board is in setup mode, this read/write register controls the system board memory.

Bit	Function
7 - 1	Reserved
0	Enable System Board RAM

Figure 2-6. System Board POS Register 3 (Hex 0103)

Bits 7 - 1 Reserved

Bit 0 When set to 1, this bit enables system board memory. When set to 0, this bit disables system board memory. All RAM installed on the system board is enabled or disabled by this operation.

System Board POS Register 4 (Hex 0104)

The system board has two memory connectors that support 1MB, 2MB, and 4MB memory cards. This read/write register contains information about the memory cards installed. POS Register 5 defines the connector.

Bit	Function
7 - 4	Memory Card ID
3 - 0	Enable Memory Card

Figure 2-7. System Board POS Register 4 (Hex 0104)

Bits 7 - 4 Bits 7 through 4 provide the memory card ID.

Bits 7654	Size	Speed
0000	4MB	80 ns
0001	2MB	100 ns
0010	1MB	100 ns
0011-0100	Reserved	--
0101	2MB	85 ns
0110	1MB	85 ns
0111-1110	Reserved	--
1111	No memory card installed	--

Figure 2-8. Memory Card ID Bits

4MB Memory Cards

Bits 3 - 0 When set to 1, a 4MB memory card is enabled

1MB and 2MB Memory Cards

Bits 3, 2 Reserved

Bit 1 When set to 1, this bit enables the second 1MB on a 2MB memory card.

Bit 0 When set to 1, this bit enables a 1MB memory card or the first 1MB on a 2MB memory card.

System Board POS Register 5 (Hex 0105)

This is the memory control register.

Bit	Function
7, 6	Reserved
5	640KB - 1MB Split Enable
4	ROM Enable
3	Reserved = 1
2 - 0	Memory Connector Select for POS Register 4

Figure 2-9. System Board POS Register 5 (Hex 0105)

Bits 7, 6 Reserved.

Bit 5 When this bit is set to 0, system board RAM between 640KB and 1MB is enabled. Typically, 128KB of this memory is mapped to the system board ROM address space, and the remaining 256KB is mapped to the first available address following the last full 1MB block of

activated system board memory. When set to 1, this bit disables system board RAM between 640KB and 1MB.

Bit 4 This bit determines how addresses hex 0E0000 to 0FFFFF are assigned.

When this bit is set to 1, ROM is enabled; the read-access addresses are assigned to ROM and the write-access addresses are disabled. When this bit is set to 0, ROM is disabled; the read-access addresses are assigned to RAM and the write-access addresses are disabled. Bit 5 of this register must be set to 0 before ROM can be disabled.

Bit 3 This bit is reserved.

Bits 2 - 0 These bits select the memory connector to be used by POS Register 4.

Bits 2 1 0	Function
0 0 0	Memory Connector 1
0 0 1	Memory Connector 2
0 1 0 - 1 1 1	Reserved

Figure 2-10. Memory Connector Select for POS Register 4

Adapter Setup

The Adapter Enable/Setup register (hex 0096) selects the channel connector to be configured.

Bit	Function
7	Channel Reset
6 - 4	Reserved
3	Card Setup Enable
2 - 0	Channel Select 2 - 0

Figure 2-11. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6 - 4 Reserved.

Bit 3 When set to 1, this bit enables the '-card setup' (-CD SETUP) signal selected by bits 2 through 0.

Bits 2 - 0 These bits are the address bits for -CD SETUP. Connectors 1 through 3 of the bus adapter are addressed as 0 through 2, respectively, and the fixed disk drive connector is addressed as 3. When bit 3 is set to 1, these bits select the connector that is put into setup.

Associated with each channel connector is a unique '-card setup' signal used to put the adapters in the setup mode, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Notes:

1. -CD SETUP goes active only when an operation is performed in the I/O address range hex 0100 through 0107.
2. The status of the Adapter Enable/Setup register (hex 0096) can be read by a program. However, when the register is read, bits 6 through 4 are set to 1.

Section 3. System Board

Description 3-3
Microprocessor and Math Coprocessor 3-3
| Micro Channel Implementation 3-3
| Exception Reporting 3-3
Central Arbiter 3-3
Arbitration Bus Priority Assignments 3-4
Central Arbiter Programming 3-5
Bus Adapter 3-6
Diskette Drive Controller 3-8
Memory 3-9
ROM Subsystem 3-9
RAM Subsystem 3-9
Error Recovery 3-10
System Memory Map 3-11
System Board Memory Connectors 3-12
| RT/CMOS RAM 3-13
RT/CMOS Address and NMI Mask Register (Hex 0070) . . 3-13
RT/CMOS Data Register (Hex 0071) 3-14
RT/CMOS RAM I/O Operations 3-14
Real-Time Clock Bytes (Hex 000-00D) 3-15
CMOS RAM Configuration 3-18
Miscellaneous System Functions and Ports 3-22
Nonmaskable Interrupt 3-22
System Control Port B (Hex 0061) 3-23
System Control Port A (Hex 0092) 3-24
Power-On Password 3-26
Type 2 Serial Port Controller 3-26
Hardware Compatibility 3-27

© Copyright IBM Corp. 1989, 1990

Notes:

Description

This section describes the microprocessor, math coprocessor, channel differences, memory subsystems, and miscellaneous system ports and connectors for the Model 55. Additional information on these topics can be found in the *Hardware Interface Technical Reference* listed in the preface of this manual.

Microprocessor and Math Coprocessor

The 80386SX microprocessor used in the Model 55 runs at 16MHz and has a 24-bit address and a 16-bit data interface. The 80386SX microprocessor is software-compatible with the 80386 microprocessor.

The 80387SX math coprocessor is matched to the speed of the system microprocessor and operates in the synchronous mode. The 80387SX math coprocessor is software-compatible with the 80387 math coprocessor.

Micro Channel Implementation

This section describes the implementation of the Micro Channel architecture on Model 55 systems. For general Micro Channel architecture information, refer to the *Hardware Interface Technical Reference*.

Exception Reporting

Exceptions should be reported using the asynchronous channel check procedure. The synchronous channel check procedure is not supported.

Central Arbiter

The central arbitration control point gives intelligent subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. The central arbiter supports up to 15 arbitrating devices (levels 0 through E) and the system microprocessor (level F).

Arbitration Bus Priority Assignments

The following figure shows the assignment of arbitration levels. The functions with the lowest arbitration level have the highest priority.

ARB Level	Primary Assignment
-2	Memory Refresh
-1	NMI
0	DMA Channel 0 (Programmable to any arbitration level)
1	DMA Channel 1
2	DMA Channel 2
3	DMA Channel 3
4	DMA Channel 4 (Programmable to any arbitration level)
5	DMA Channel 5
6	DMA Channel 6
7	DMA Channel 7
8 - E	Available
F	System Microprocessor

Figure 3-1. Arbitration Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation, and by the previous controlling master. The diskette drive controller should not be held inactive for more than 12 microseconds to prevent overrun.

Nonmaskable interrupt (NMI) service is executed at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal (ARB/-GNT) is in the arbitrate state.

When the central arbitration control point receives a level -1 request (NMI, a system-board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level -1 request, and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following figures.

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Mask
5	Enable Extended Arbitration (Not Supported)
4 - 0	Reserved

Figure 3-2. Arbitration Register, Write to Hex 0090

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Masked by NMI
5	Bus Time-Out
4	Reserved
3 - 0	Value of Arbitration Bus During Previous Grant State

Figure 3-3. Arbitration Register, Read Hex 0090

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 extends the arbitration cycle from a minimum of 400 nanoseconds to a minimum of 800 nanoseconds. The Model 55 does not support this mode of operation. Setting this bit to 1 can cause unpredictable results.

Reading this bit as a 1 indicates that a bus time-out has occurred. The bus-time-out indication is not reset until bit 6 of this register is set to 0.

Bit 4 This bit is reserved and should be 0.

Bits 3 - 0 These bits are undefined for a write operation and should be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Bus Adapter

The Model 55 uses a direct bus attachment board to provide four channel connectors:

- Two 16-bit Micro Channel connectors
- One 16-bit Micro Channel connector with an auxiliary video extension
- One card edge connector for the fixed disk drive.

The adapters are installed into the direct bus attachment board horizontally.

When in the setup mode, the fixed disk drive is addressed as channel connector 3 through the Adapter Enable/Setup register (hex 0096). See "Adapter Setup" on page 2-11. For more POS information about the fixed disk drive, refer to the technical reference for that drive.

The fixed disk drive connector is a 2- by 36-pin connector on the top edge of the direct bus attachment board. The following figure shows the signal assignments and pin numbering for the connector.

Pin	Side A I/O	Signal	Pin	Side B I/O	Signal
1	O	-CD SETUP	1	O	A15
2	O	A13	2	O	A14
3	N/A	Ground	3	N/A	Ground
4	O	A11	4	O	Reserved
5	O	A10	5	N/A	Ground
6	O	A09	6	O	A12
7	O	+5 Vdc	7	O	-CMD
8	O	A08	8	I	-CD SFDBK
9	O	A07	9	N/A	Ground
10	O	A06	10	I/O	D01
11	N/A	Ground	11	I/O	D03
12	O	A05	12	I/O	D04
13	O	A04	13	N/A	Ground
14	O	A03	14	O	CHRESET
15	O	+5 Vdc	15	I/O	D08
16	O	A02	16	I/O	D09
17	O	A01	17	N/A	Ground
18	O	A00	18	I/O	D12
19	O	+12 Vdc	19	I/O	D14
20	O	-ADL	20	I/O	D15
21	I	-PREEMPT	21	N/A	Ground
22	I	-BURST	22	I/O	D00
23	O	+5 Vdc	23	I/O	D02
24	I	ARB 00	24	I/O	D05
25	I	ARB 01	25	N/A	Ground
26	I	ARB 02	26	I/O	D06
27	N/A	+12 Vdc	27	I/O	D07
28	I	ARB 03	28	I/O	D10
29	O	ARB/-GNT	29	N/A	Ground
30	O	-TC	30	I/O	D11
31	N/A	+5 Vdc	31	I/O	D13
32	O	-S0	32	O	-SBHE
33	O	-S1	33	N/A	Ground
34	O	M/-IO	34	I	-CD DS 16
35	N/A	Ground	35	I	-IRQ 14
36	I	CD CHRDY	36	N/A	Ground

Figure 3-4. Fixed Disk Drive Connector

Diskette Drive Controller

The system board uses the Type 1 diskette drive controller. However, several pin assignments of the 2- by 20-pin connector are different from the ones shown in the *IBM Personal System/2 Hardware Interface Technical Reference*. The following figure shows the signal assignments and pin numbering for the connector.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Reserved	2	O	-High Density Select
3	N/A	+5 Vdc	4	N/A	Reserved
5	N/A	Ground	6	N/A	+12 Vdc
7	N/A	Ground	8	I	-Index
9	N/A	Ground	10	N/A	Reserved
11	N/A	Ground	12	O	-Drive Select
13	N/A	Ground	14	N/A	Reserved
15	N/A	Ground	16	O	-Motor Enable
17	N/A	Ground	18	O	-Direction
19	N/A	Ground	20	O	-Step
21	N/A	Ground	22	O	-Write Data
23	N/A	Ground	24	O	-Write Enable
25	N/A	Ground	26	I	-Track 0
27	N/A	Ground	28	I	-Write Protect
29	N/A	Ground	30	I	-Read Data
31	N/A	Ground	32	O	-Head 1 Select
33	N/A	Ground	34	I	-Diskette Change
35	N/A	Ground	36	N/A	Ground
37	N/A	Reserved	38	O	+5 Vdc
39	N/A	Ground	40	O	+12 Vdc

Figure 3-5. Diskette Drive Connector

Memory

The Model 55 uses the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- RT/CMOS RAM.

ROM Subsystem

The ROM subsystem consists of 128KB. ROM is active at power-on time and is assigned the top of the first and last 1MB of address space (0E0000 to 0FFFFF and FE0000 to FFFFFF). After POST ensures that system memory is operating properly, the ROM code is copied to RAM at the same address space, and ROM is disabled.

ROM or RAM access at address space hex 0E0000 to 0FFFFF is controlled by the ROM enable bit in System Board POS Register 5, hex 0105. When enabled, ROM is not parity-checked and operates with three 62.5-nanosecond wait states.

RAM Subsystem

The RAM subsystem on the system board starts at address hex 000000 of the address space. The RAM subsystem is 18 bits wide: 16 data bits and 2 parity bits. One parity bit is generated for each byte of data written. During a read operation, one parity bit is checked for each byte of data read by the device controlling the bus.

Two memory connectors are provided on the system board. Each connector can support 1MB, 2MB, or 4MB of memory.

The system enables and disables the 1MB and 2MB memory cards in 1MB blocks. Each 1MB block must start on a 1MB boundary. Because 128KB of I/O ROM, 128KB of system board ROM, and 128KB of video memory are mapped within the first 1MB of address space, the first physical 1MB of RAM cannot be mapped to contiguous addresses and is therefore split at the 640KB boundary creating a 384KB overflow. The high 128KB of the overflow is mapped to the system board ROM address space; the remaining 256KB, called the *split memory block*, is either disabled or mapped to the first available address following the last full 1MB of activated system board memory. Split-memory-block remapping and disabling are controlled by System Board POS Register 5, hex 0105.

Note: The 4MB memory card cannot be enabled or disabled in 1MB blocks.

Additional memory can be added in any of the Micro Channel connectors. However, the total amount of memory installed must not exceed the 16MB addressing limit of the DMA controller. The total amount of usable memory is less than the amount of memory installed because of ROM-to-RAM remapping.

Error Recovery

If POST detects a memory error on the 1MB or 2MB memory card, an attempt is made to deactivate the physical 1MB block of memory that contains the error. The addresses assigned to the deactivated block are reassigned to the next physical block of system board memory, if installed (the first 1MB of memory address space cannot be assigned to memory installed in any of the Micro Channel connectors). If 1MB of valid system board memory cannot be found, the system sets the memory size according to the last good memory available and allows a system reset; however, if a minimum of 64KB of good memory cannot be found, POST cannot recover from the error.

Note: The 4MB memory card cannot be enabled or disabled in 1MB blocks.

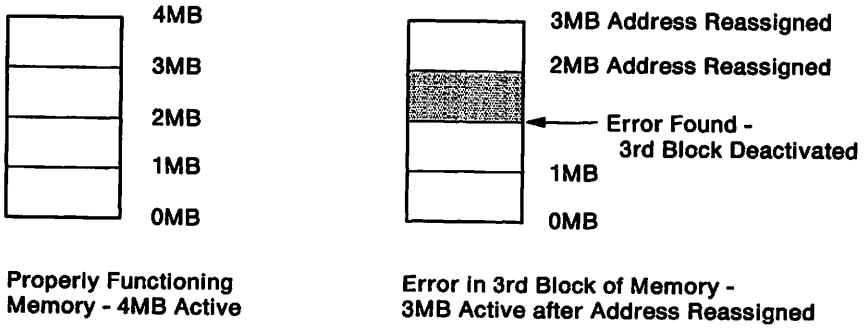


Figure 3-6. Memory Error Address Reassignment

If the first physical 1MB of memory is disabled, the split-memory block and ROM-to-RAM remap feature will not be enabled.

System Memory Map

Memory is mapped by System Board POS Register 5, hex 0105.

Warning: IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignments of the same system resource, improper operation of the feature, loss of data, or damage to the hardware.

The first 640KB of system board RAM is mapped starting at address hex 000000. A 256-byte and 1KB portion of this RAM is reserved as BIOS data areas. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for details.

The following figure shows the memory map for a properly functioning system. Memory can be mapped differently if POST detects an error in system board memory or RT/CMOS RAM. In the following figure, the variable *X* represents the number of 1MB blocks of system board memory starting at or above the hex 100000 boundary. The variable *Y* represents the number of 1MB blocks of addressable memory installed in the channel starting at or above the hex 100000 boundary (*Y* cannot exceed 14.75).

Hex Range	Function
000000 to 09FFFF	640KB System Board RAM
0A0000 to 0BFFFF	128KB Video RAM
0C0000 to 0DFFFF	Channel ROM
0E0000 to 0FFFFF	128K System Board ROM mapped to RAM
100000 to (100000 + *X*MB)	*X*MB System Board RAM
(100000 + *X*MB) to (100000 + *X*MB + 256KB)	256KB System Board RAM (Split Memory Block)
(100000 + *X*MB + 256KB) to (100000 + *X*MB + 256KB + *Y*MB)	*Y*MB Channel RAM
(100000 + *X*MB + 256KB + *Y*MB) to FDFFFF	Not Used
FE0000 to FFFFFF	128KB System Board ROM (Same as 0E0000 to 0FFFFF)

Figure 3-7. System Memory Map

System Board Memory Connectors

The system board has two 72-pin memory connectors that support 1MB, 2MB, and 4MB memory cards. The following figure shows the pin assignments for the connectors.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Ground	37	I/O	Parity Data High
2	I/O	Data 0	38	I/O	Parity Data High
3	I/O	Data 0	39	N/A	Ground
4	I/O	Data 1	40	O	CAS 0
5	I/O	Data 1	41	O	CAS 2
6	I/O	Data 2	42	O	CAS 3
7	I/O	Data 2	43	O	CAS 1
8	I/O	Data 3	44	O	RAS 0
9	I/O	Data 3	45	O	RAS 1
10	O	+5 Vdc	46	O	Block Select 1
11	O	-CAS Parity	47	O	Write Enable
12	O	Address 0	48	N/A	Reserved
13	O	Address 1	49	I/O	Data 8
14	O	Address 2	50	I/O	Data 8
15	O	Address 3	51	I/O	Data 9
16	O	Address 4	52	I/O	Data 9
17	O	Address 5	53	I/O	Data 10
18	O	Address 6	54	I/O	Data 10
19	N/A	Reserved	55	I/O	Data 11
20	I/O	Data 4	56	I/O	Data 11
21	I/O	Data 4	57	I/O	Data 12
22	I/O	Data 5	58	I/O	Data 12
23	I/O	Data 5	59	O	+5 Vdc
24	I/O	Data 6	60	I/O	Data 13
25	I/O	Data 6	61	I/O	Data 13
26	I/O	Data 7	62	I/O	Data 14
27	I/O	Data 7	63	I/O	Data 14
28	O	Address 7	64	I/O	Data 15
29	O	Block Select 0	65	I/O	Data 15
30	O	+5 Vdc	66	O	Block Select 2
31	O	Address 8	67	I	Presence Detect 0
32	O	Address 9	68	I	Presence Detect 1
33	O	RAS 3	69	I	Presence Detect 2
34	O	RAS 2	70	I	Presence Detect 3
35	I/O	Parity Data Low	71	O	Block Select 3
36	I/O	Parity Data Low	72	N/A	Ground

RAS = Row Address Strobe
CAS = Column Address Strobe

Figure 3-8. System Board Memory Connectors

RT/CMOS RAM

The RT/CMOS RAM (real-time clock/complementary metal-oxide semiconductor RAM) chip contains the real-time clock and 64 bytes of CMOS RAM. The clock circuitry uses 14 bytes of this memory, and the rest is allocated to configuration and system status information. A battery is built into the chip to keep the RT/CMOS RAM active when the power supply is not on.

The Type 2 system board has an additional 2KB CMOS RAM extension with a built-in battery, for configuration and other system information.

The following figure shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000 - 00D	Real-Time Clock Bytes
00E	Diagnostic Status Byte
00F	Shutdown Status Byte
010	Diskette Drive Type Byte
011	Fixed Disk Drive Type Byte
012	Reserved
013	Reserved
014	Equipment Byte
015, 016	Low and High Base Memory Bytes
017, 018	Low and High Expansion Memory Bytes
019 - 031	Reserved
032, 033	Configuration CRC Bytes
034 - 036	Reserved
037	Date Century Byte
038 - 03F	Reserved

Figure 3-9. RT/CMOS RAM Address Map

RT/CMOS Address and NMI Mask Register (Hex 0070)

This register is used in conjunction with the RT/CMOS Data register (hex 0071) to read from and write to the RT/CMOS RAM bytes.

Bit	Function
7	NMI Mask
6	Reserved
5 - 0	RT/CMOS RAM Address

Figure 3-10. RT/CMOS Address and NMI Mask Register (Hex 0070)

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Bit 7 When this bit is set to 1, the NMI is masked off (disabled). This bit is set to 1 by a power-on reset. This is a write-only bit.

Bit 6 Reserved.

Bits 5 - 0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This register is used in conjunction with the RT/CMOS Address and Mask register (hex 0070) to read from and write to the RT/CMOS RAM bytes.

Bit	Function
7 - 0	RT/CMOS Data

Figure 3-11. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts should be masked to prevent other interrupt routines from changing the RT/CMOS Address register before data is read or written. After I/O operations, the RT/CMOS Address and NMI Mask register (hex 0070) should be left pointing to Status Register D (hex 00D).

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Writing to the RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS Address and NMI Mask register (hex 0070).
2. Write the data to the RT/CMOS Data register (hex 0071).

Reading from the RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Read the data from the RT/CMOS Data register (hex 0071).

Real-Time Clock Bytes (Hex 000-00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following figure.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second Alarm	1
002	Minutes	2
003	Minute Alarm	3
004	Hours	4
005	Hour Alarm	5
006	Day of Week	6
007	Date of Month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-12. Real-Time Clock Bytes

Note: The Setup program initializes Status Registers A, B, C, and D when the time and date are set. Interrupt hex 1A is the BIOS interface to read and set the time and date, and it initializes the register the same way as the Setup program.

Status Register A (Hex 00A)

Bit	Function
7	Update in Progress
6 - 4	22-Stage Divider
3 - 0	Rate Selection Bits

Figure 3-13. Status Register A

Bit 7 When set to 1, this bit indicates the time-update cycle is in progress. When set to 0, it indicates that the current date and time can be read.

Bits 6 - 4 These bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768-kHz time base. This is the only value supported by the system for proper timekeeping.

Bits 3 - 0 These bits allow the selection of a divider output frequency. The system initializes the rate selection bits to a binary 0110, which selects a 1.024-kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Periodic Interrupt Enable
5	Alarm Interrupt Enable
4	Update-Ended Interrupt Enabled
3	Square Wave Enabled
2	Date Mode
1	24-Hour Mode
0	Daylight-Saving Time Enabled

Figure 3-14. Status Register B

Bit 7 When set to 0, this bit updates the cycle, normally by advancing the counts at a rate of one per second. When set to 1, this bit immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This bit is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

Bit 5 When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit indicates whether the binary-coded-decimal (BCD) or binary format is used for time-and-date calendar updates. When set to 1, this bit indicates the binary format. The system initializes this bit to 0.

Bit 1 This bit indicates if the hours byte is in 12-hour or 24-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When set to 1, this bit enables the daylight-saving-time mode. When set to 0, this bit disables the mode and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt Request Flag
6	Periodic Interrupt Flag
5	Alarm Interrupt Flag
4	Update-Ended Interrupt Flag
3 - 0	Reserved

Figure 3-15. Status Register C

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When set to 1, this bit indicates that a periodic interrupt occurred.

Bit 5 When set to 1, this bit indicates that an alarm interrupt occurred.

Bit 4 When set to 1, this bit indicates that an update-ended interrupt occurred.

Bits 3 - 0 Reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6 - 0	Reserved

Figure 3-16. Status Register D

Bit 7 This read-only bit monitors the internal battery. When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power.

Bits 6 - 0 Reserved.

CMOS RAM Configuration

The following shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-Time Clock Chip Power
6	Configuration Record and Checksum Status
5	Incorrect Configuration
4	Memory Size Mismatch
3	Fixed Disk Controller/Drive C Initialization Status
2	Time Status Indicator
1	Adapter Configuration Miscompare
0	Adapter ID Time-Out

Figure 3-17. Diagnostic Status Byte

Bit 7 When set to 1, this bit indicates that the real-time clock chip lost power.

Bit 6 When set to 1, this bit indicates that the checksum is incorrect.

Bit 5 This is a power-on check of the equipment byte (hex 014). When set to 1, this bit indicates that the configuration information is incorrect.

Bit 4 When set to 1, this bit indicates that the memory size does not match the configuration information.

Bit 3 When set to 1, this bit indicates that the controller or fixed disk drive failed initialization.

Bit 2 When set to 1, this bit indicates that the time is invalid.

Bit 1 When set to 1, this bit indicates that the adapters do not match the configuration information.

Bit 0 When set to 1, this bit indicates that a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7 - 4	Diskette Drive Type
3 - 0	Reserved

Figure 3-18. Diskette Drive Type Byte

Bits 7 - 4 These bits indicate the diskette drive type.

Bits 7 6 5 4	Function
0 0 0 0	No drive present
0 0 1 1	High-capacity diskette drive (720KB)
0 1 0 0	High-density diskette drive (1.44MB)

Note: All combinations that are not shown are reserved.

Figure 3-19. Diskette Drive Type Bits

Bits 3 - 0 Reserved.

Fixed Disk Drive Type Byte (Hex 011): This byte defines the type of fixed disk drive installed. Hex 00 indicates that a fixed disk drive is *not* installed.

Note: For more information about fixed disk drive types, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Reserved Bytes (Hex 012, 013): These bytes are reserved.

Equipment Byte (Hex 014): This byte defines the basic equipment in the system for the power-on diagnostic tests.

Bit	Function
7, 6	Number of Diskette Drives
5, 4	Display Operating Mode
3, 2	Reserved
1	Math Coprocessor Presence
0	Diskette Drive Presence

Figure 3-20. Equipment Byte

Bits 7, 6 These bits indicate the number of diskette drives installed, as shown in the following figure.

Bits 7 6	Number of Diskette Drives
0 0	One Drive
0 1	Reserved
1 0	Reserved
1 1	Reserved

Figure 3-21. Installed Diskette Drive Bits

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port, as shown in the following figure.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-Column Mode
1 0	80-Column Mode
1 1	Monochrome Mode

Figure 3-22. Display Operating Mode Bits

Bits 3, 2 Reserved.

Bit 1 When set to 1, this bit indicates that a math coprocessor is installed.

Bit 0 When set to 1, this bit indicates that a diskette drive is installed.

Low and High Base Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 is equal to 640KB. The low byte is hex 015; the high byte is hex 016.

Low and High Expansion Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The hexadecimal values in these bytes represent the number of 1KB blocks of expansion memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 017; the high byte is hex 018.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check (CRC) data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 033; the high byte is hex 032.

Reserved Bytes (Hex 034 through 036): These bytes are reserved.

Date Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 through 03F): These bytes are reserved.

Miscellaneous System Functions and Ports

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system watchdog time-out has occurred. The NMI stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts, and the IRET instruction restores the interrupt flag to the state it was in before the interrupt. A system reset causes a reset of the NMI.

The NMI requests from system board parity and channel check are subject to mask control with the NMI mask bit in the RT/CMOS Address register. The watchdog timer and system channel time-out are not masked by this bit. See "RT/CMOS Address and NMI Mask Register (Hex 0070)" on page 3-13. The power-on default of the NMI mask is 1 (NMI disabled). Before the NMI is enabled after a power-on reset, the parity-check and channel-check states are initialized by POST.

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the write and read functions of this port are shown in the following figures.

Bit	Function
7	Reset Timer 0 Output Latch (IRQ0)
6 - 4	Reserved
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-23. System Control Port B (Write)

Bit	Function
7	Parity Check
6	Channel Check
5	Timer 2 Output
4	Toggles with Each Refresh Request
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-24. System Control Port B (Read)

Bit 7 When this bit is set to 1 during a write operation, IRQ0 is reset. When read as a 1, this bit indicates a parity check has occurred.

Bit 6 When read as a 1, this bit indicates a channel check has occurred.

Bit 5 When read, this bit indicates the condition of the timer/counter 2 'output' signal.

Bit 4 When read, this bit toggles for each refresh request.

Bit 3 When set to 0, this bit enables channel check. This bit is set to 1 during a power-on reset.

Bit 2 When set to 0, this bit enables parity check. This bit is set to 1 during a power-on reset.

Bit 1 When set to 1, this bit enables speaker data.

Bit 0 When set to 1, this bit enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7 - 5	Reserved
4	Watchdog Timer Status
3	Security Lock Latch
2	Reserved = 0
1	Alternate Gate A20
0	Alternate Hot Reset

Figure 3-25. System Control Port A

Bits 7 - 5 Reserved.

Bit 4 This read-only bit indicates the watchdog timer status. When this bit is set to 1, a watchdog time-out has occurred. For more information about the watchdog timer, refer to the *IBM Personal System/2 Hardware Interface Technical Reference*.

Bit 3 This bit provides the security lock for the secured area of RT/CMOS. When this bit is set to 1, the 8-byte, power-on password is electrically locked. Once this bit is set by POST, it can be cleared only by turning the system off.

Bit 2 Reserved.

Bit 1 This bit is used to enable the 'address 20' signal (A20) when the microprocessor is in the real address mode. When this bit is set to 0, A20 cannot be used in real mode addressing. This bit is set to 0 during a system reset.

Bit 0 This bit provides an alternate method of resetting the system microprocessor. This alternate method supports operating systems requiring faster operation than was provided on the IBM Personal Computer AT*. Resetting the system microprocessor switches the microprocessor from the protected mode to the real address mode. The alternate reset takes 13.4 microseconds.

This bit is set to 0 by either a system reset or a write operation. When a write operation changes this bit from 0 to 1, the alternate reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is 0, POST assumes the system was just powered on. If the bit is 1, POST assumes a switch from the protected mode to the real mode has taken place.

When bit 0 is used to reset the system microprocessor to the real mode, the following procedure must be used.

1. Disable all maskable and non-maskable interrupts.
2. Reset the system microprocessor by writing bit 0 to 1.
3. Issue a Halt instruction to the system microprocessor.

If this procedure is not followed, the results will be unpredictable.

Note: Whenever possible, BIOS or ABIOS should be used as an interface to reset the system microprocessor to the real mode.

* Trademark of the International Business Machines Corporation.

Power-On Password

Eight bytes of RT/CMOS RAM are reserved for the power-on password and its check character. The microprocessor can access these bytes only during POST. After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by a program.

Installing the password is a function of a program on the Reference Diskette. The power-on password does not appear on the screen when it is installed, changed, or removed. Once the power-on password has been installed, it can be changed only during POST.

The power-on password can be bypassed (erased) by using the following procedure:

1. Power off the system.
2. Disconnect the speaker/password security connector from the bus adapter.
3. Rotate the speaker/password security connector 180 degrees and reconnect it.
4. Power on the system.

The system unit cover can be physically locked to prevent access to the speaker/password security connector.

The Model 55 also has a keyboard password. See "Keyboard and Auxiliary Device Controller" in the *IBM Personal System/2 Hardware Interface Technical Reference* for more information.

Type 2 Serial Port Controller

Some Type 2 serial controllers used on the Model 55 system board do not respond as described in the *Hardware Interface Technical Reference.*

After the FIFO mode is enabled, bit 6 of the Interrupt Identification register is erroneously set to 0, indicating a Type 1 serial controller is installed. Any application program or operating system that uses bit 6 of the Interrupt Identification register as an indicator to determine FIFO support will default to the character mode. This indicator is ignored by the Model 55 ABIOS. Therefore, programs that operate through ABIOS can use the FIFO mode. The ABIOS routines also clear any error indications remaining after a mode change.

Some application programs reset the received-data-ready indication by writing bit 0 of the Line Status register as a 0. This method can cause compatibility problems and is not supported by Type 1 or Type 2 serial controllers. To avoid compatibility problems, bit 0 of the Line Status register can be reset to 0 by reading the data and discarding the data if it is not used.

Hardware Compatibility

The Model 55 maintains many of the interfaces used by the IBM Personal Computer AT. In most cases command and status organization of these interfaces is maintained.

The functional interfaces for the Model 55 are compatible with the following interfaces:

- The Intel** 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller-address/transfer counters, page registers and status fields only. The Command and Request registers are not supported. The rotate and mask functions are not supported. The Mode register is partially supported.
- Generally compatible with the National Semiconductor** NS16550A serial communications controller.
- The Intel 8088, 8086, 80286, and 80386 microprocessors.
- The Intel 8272 diskette drive controller. The BIOS limits support to diskette drives that have a 3-millisecond step rate during recalibration.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The Intel 8042 keyboard port at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.

** Trademark of the Intel Corporation.

** Trademark of the National Semiconductor Corporation.

** Trademark of Motorola, Incorporated.

- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.
- Generally compatible with the Intel 80387, 80287, and 8087 math coprocessors.

Whenever possible, BIOS or ABIOS should be used as an interface to reset the system microprocessor to the real mode.

The system microprocessor also can be reset to the real mode through bit 0 of port hex 0064 or hex 0092. When using either of these ports, the following procedure must be used.

1. Disable all maskable and non-maskable interrupts.
2. Reset the system microprocessor.
3. Issue a Halt instruction to the system microprocessor.

If this procedure is not followed, the results will be unpredictable.

Index

A

adapter
  enable/setup register 2-11
  setup 2-4
address and NMI mask register, RT/CMOS 3-13
address map
  memory 3-11
  POS I/O 2-5
  reassignment 3-10
  system board I/O 1-5
address 20 gate 3-24
alternate reset 3-25
altitude 1-7
anticipated page miss 1-6
arbiter programming 3-5
arbitration control point 3-3
arbitration level 3-4
arbitration register 3-5
arbitration, central control point 3-5
audio subsystem 1-4

B

base memory bytes 3-21
battery 3-18
bus adapter 3-6, 3-26
bus contention 2-3
bus priority assignments 3-4

C

cables 1-7
card selected feedback 2-6
card setup 2-11
-CD SETUP 2-11
-CD SFDBK 2-6
central arbitration control point 3-3
channel 3-3
  check enable 3-23
  check latch 3-23
channel *(continued)*
  connector 1-4, 3-6
  DMA 1-4, 3-4
  reset 2-11
clock, real-time 3-13, 3-15
CMOS RAM 1-4, 3-13—3-22
compatibility 3-27
configuration
  CRC bytes 3-21
  RT/CMOS 3-18
connector
  channel 1-4, 3-6
  diskette drive 3-8
  fixed disk drive 3-6
  memory 3-12
contention, bus 2-3
control ports, system 3-23—3-25
controller
  diskette drive 1-4, 2-8
  DMA 1-4
  interrupt 1-4
  keyboard/auxiliary device 1-4
  parallel 1-4
  serial 1-4, 3-26
coprocessor, math 1-4, 3-3
current, electrical 1-7

D

data register, RT/CMOS 3-14
date century byte 3-21
depth, system unit 1-7
description, power supply 1-9
device types 1-3
diagnostic status byte (RT/CMOS) 3-18
diskette drive
  connector 3-8
  controller 2-8
  type byte 3-19
diskette overruns 3-4
display operating mode 3-20

© Copyright IBM Corp. 1989, 1990

DMA
channels 1-4, 3-4
controller 1-4
performance 1-6

E

enable NMI 3-13
equipment byte 3-20
error recovery 3-10
extended arbitration 3-5

F

fault, overvoltage 1-10
feedback, card selected 2-6
fixed disk drive
connector 3-6
initialization 3-18
type byte 3-20

G

gate A20 3-24

H

height, system unit 1-7
humidity 1-7

I

identifier, model 1-3
interrupt
controller 1-4
IRQ0 reset 3-23
NMI reset 3-22
I/O
address map 1-5
RT/CMOS RAM operations 3-14
system board 2-8

K

keyboard
cable 1-7
password 3-26

M

math coprocessor 1-4, 3-3
measurements, system unit 1-7
memory
bytes 3-21
card ID bits 2-10
connector 3-12
control register 2-10
description 3-9
error recovery 3-10
performance 1-6
RAM 3-9
read 1-6
reassigning 3-10
refresh 3-4
ROM 3-9
RT/CMOS RAM 3-13
setup on system board 2-9
size miscompare 3-18
split 2-11
system memory map 3-11
write 1-6
Micro Channel architecture
arbitration control point 3-3
bus adapter 1-4, 3-6
disk drive 3-6
fixed disk drive 3-6
general information 3-3
microprocessor
alternate reset 3-25
description 3-3
features 1-4
mode switch compatibility 3-25
performance 1-6
real address mode 3-24
mode switch, protected 3-25
model/submodel bytes 1-3

N

NMI mask register 3-13
NMI service 3-4
NMI signal 3-4
nonmaskable interrupt (NMI) 3-22

O

output voltage sequencing 1-10
outputs, power supply 1-9
overvoltage fault 1-10

P

page hit 1-6
page miss 1-6
parallel port 1-4, 2-8
parity check enable 3-23
password
  keyboard 3-26
  power-on 3-24, 3-26
performance, system 1-6
port
  parallel 1-4, 2-8
  serial 1-4, 2-8
  system 3-22
POS
  See programmable option select (POS)
POST 3-9
power
  cable 1-7
  loss 3-18
  specifications 1-7
power supply description 1-9
power supply output protection 1-10
power supply outputs 1-9
power-on password 3-24, 3-26
programmable option select (POS)
  adapter enable/setup register 2-11
  address map 2-5
  card selected feedback register 2-6
  description 2-3
  setup procedures 2-4
  system board enable/setup register 2-7
  system board I/O 2-8
  system board POS registers 2-10
  system board setup 2-6
programmable option select (POS) *(continued)*
  system configuration utilities 2-3, 3-11
  system memory map 3-11
  video 2-7
  warning 2-3, 3-11
programming, arbiter 3-5
protected mode switch 3-25
protection, power supply 1-10

R

RAM (random access memory) 1-4, 3-9
random access memory (RAM) 1-4, 3-9
read-only memory (ROM) 1-4, 3-9
real mode switch 3-25
real-time clock 3-13, 3-15
recovery, error 3-10
refresh 3-4
refresh request 1-6, 3-23
register
  adapter enable/setup 2-11
  card selected feedback 2-6
  memory control 2-10
  miscellaneous system 3-22
  RT/CMOS address and NMI mask 3-13
  RT/CMOS data 3-14
  RT/CMOS status 3-16—3-18
  system board enable/setup 2-7
  system board POS 2-5—2-10
  system control 3-23
reset, alternate 3-25
ROM enable 2-10
ROM (read-only memory) 1-4, 3-9
RT/CMOS RAM
  address and NMI mask register 3-13
  address map 3-13
  configuration bytes 3-18
  data register 3-14
  description 3-13
  diagnostic status byte 3-18
  I/O operations 3-14

RT/CMOS RAM *(continued)*
power-on password 3-26
secured area 3-24
status registers 3-16—3-18

S

sequencing, output voltage 1-10
serial port 1-4, 2-8
setup
bus contention 2-3
system board 2-4, 2-6
system board I/O 2-8
system memory map 3-11
video 2-7
shutdown status byte 3-19
signal
card selected feedback 2-6
card setup 2-11
channel reset 2-11
size, system unit 1-7
speaker data enable 3-23
specifications
performance 1-6
physical 1-7
status registers
(RT/CMOS) 3-16—3-18
switch to real 3-25
system
configuration utilities 2-3, 3-11
control ports 3-23—3-25
description 1-3
functions, miscellaneous 3-22
performance 1-6
reset 3-22
specifications 1-7
timers 1-4
system board
address map 1-5
description 3-3
enable/setup register 2-7
features 1-3
I/O 2-8
memory connector 3-12
memory register 2-9
model identifier 1-3
POS I/O address map 2-5
system board *(continued)*
POS registers 2-10
setup 2-4, 2-6

T

temperature 1-7
time status indicator 3-19
timers, system 1-4
type identifier 1-3

V

video
setup 2-7
subsystem 1-4, 2-4

W

warning
arbitration 3-4
central arbiter 3-5
NMI mask 3-22
POS 2-3, 3-11
RT/CMOS 3-14
watchdog status 3-24
weight, system unit 1-7
width, system unit 1-7

Numerics

80386SX microprocessor 1-4, 1-6, 3-3
80387SX math coprocessor 1-4, 3-3

Personal System/2
Model 56
Technical Reference

Note

Before using this information and the product it supports, be sure to read the general information under "Notices" on page vii.

Third Edition (October 1992)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer of express or implied warranties in certain transactions, therefore, this statement may not apply to you.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Requests for technical information about IBM products should be made to your IBM Authorized Dealer or your IBM Marketing Representative.

© Copyright International Business Machines Corporation 1991, 1992. All rights reserved.
Note to U.S. Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Contents

Figures v

Notices vii
Trademarks and Service Marks vii

Preface ix

Section 1. System Overview 1-1
Description 1-3
System Board Devices and System Features 1-4
System Board I/O Address Map 1-8
Micro Channel Compatibility 1-10
Specifications 1-11
Power Supply 1-15
Outputs 1-16
Output Protection 1-17
Voltage Sequencing 1-17
Power Supply Connectors 1-17

Section 2. Programmable Option Select 2-1
Description 2-3
POS Address Map 2-5
Card Selected Feedback Register (Hex 0091) 2-6
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-7
System Board Group 1 POS Register 2 (Hex 0102) 2-8
System Board Group 1 POS Register 3 (Hex 0103) 2-10
System Board Group 1 POS Register 4 (Hex 0104) 2-11
System Board Group 1 POS Register 5 (Hex 0105) 2-11
System Board Group 2 POS Register 2 (Hex 0102) 2-12
System Board Group 2 POS Register 3 (Hex 0103) 2-12
System Board Group 3 POS Register 4 (Hex 0104) 2-13
System Board SCSI Controller POS Register 2 (Hex 0102) . . 2-13
System Board SCSI Controller POS Register 3 (Hex 0103) . . 2-14
Adapter Enable/Setup Register (Hex 0096) 2-14

Section 3. System Board 3-1
Description 3-3
Microprocessor—Type 1 Systems 3-3
Microprocessor—Type 2 Systems 3-3
Programming Model 3-4
Instructions 3-4

© Copyright IBM Corp. 1991, 1992

| Microprocessor—Type 3 Systems 3-4
Cache Operation 3-5
Cacheable Address Space 3-6
Math Coprocessor 3-6
Micro Channel Implementation 3-6
Central Arbiter 3-6
Bus Adapter 3-9
| Diskette Drive Connector 3-10
System Board Memory Connectors 3-11
| SCSI-Device Connector 3-12
Memory 3-13
ROM Subsystem 3-14
| RAM Subsystem 3-14
| Memory Interleaving Option 3-15
| Memory-Presence Detect Signals 3-15
| System Memory Map 3-16
Memory Controller Registers 3-16
RT/CMOS RAM 3-18
NVRAM 3-28
| Vital Product Data 3-28
Miscellaneous System Functions and Ports 3-28
| Nonmaskable Interrupt 3-28
System Control Port B (Hex 0061) 3-29
System Control Port A (Hex 0092) 3-30
| Power-On Password 3-31
| Privileged-Access Password 3-32
Keyboard Password 3-32
| Cover Lock and Tamper-Evident Switch 3-32
| Selectable Boot Sequence 3-32
Hardware Compatibility 3-33
| Error Codes 3-34

Appendix. 386SLC Instruction Cycle Times A-1

Index X-1

Figures

1-1.	Model and Submodel Bytes	1-3
1-2.	System Board Devices and System Features—56 SX and 56 SLC Models	1-4
1-3.	System Board Devices and System Features—56 486SLC2 Models	1-6
1-4.	System Board I/O Address Map	1-8
1-5.	Performance Specifications—56 SX and 56 SLC Models	1-11
1-6.	Performance Specifications—56 486SLC2 Models	1-12
1-7.	Physical Specifications—56 SX and 56 SLC Models	1-13
1-8.	Physical Specifications—56 486SLC2 Models	1-14
1-9.	Acoustical Readings	1-15
1-10.	Component Maximum Current	1-16
1-11.	Channel Load Current	1-16
1-12.	Voltage Assignments for the Internal Power-Supply Connectors	1-17
2-1.	POS I/O Address Map	2-5
2-2.	Card Selected Feedback Register (Hex 0091)	2-6
2-3.	Devices Supported in Setup Mode	2-7
2-4.	System Board Enable/Setup Register (Hex 0094)	2-7
2-5.	System Board POS Register 2 (Hex 0102)	2-8
2-6.	Parallel Port Select Bits	2-9
2-7.	System Board Group 1 POS Register 3 (Hex 0103)—Write	2-10
2-8.	System Board POS Group 1 Register 3 (Hex 0103)—Read Index 00	2-10
2-9.	System Board POS Group 1 Register 3 (Hex 0103)—Read Index 04	2-11
2-10.	System Board Group 1 POS Register 4 (Hex 0104)	2-11
2-11.	System Board Group 1 POS Register 5 (Hex 0105)	2-11
2-12.	System Board Group 2 POS Register 2 (Hex 0102)	2-12
2-13.	System Board Group 2 POS Register 3 (Hex 0103)	2-12
2-14.	Serial Port Addresses	2-12
2-15.	System Board Group 3 POS Register 4 (Hex 0104)	2-13
2-16.	System Board SCSI Controller POS Register 2 (Hex 0102)	2-13
2-17.	System Board SCSI Controller POS Register 3 (Hex 0103)	2-14
2-18.	System Board SCSI Controller ID	2-14
2-19.	Adapter Enable/Setup Register (Hex 0096)	2-14
3-1.	Arbitration Bus Priority Assignments	3-7
3-2.	Arbitration Register (Hex 0090)—Write	3-8
3-3.	Arbitration Register (Hex 0090)—Read	3-8

© Copyright IBM Corp. 1991, 1992

3-4.	Diskette Drive Connector	3-10
3-5.	System Board Memory Connectors	3-11
3-6.	SCSI Device Cable Internal Connector Pin Assignments	3-12
3-7.	System Board SCSI Device External Connector	3-13
3-8.	Memory Interleaving Configurations	3-15
3-9.	Presence-Detect Bits	3-15
3-10.	System Memory Map	3-16
3-11.	Memory-Fault RAS Capture Register (I/O Port Hex 00E2)	3-17
3-12.	Fixed RAS Signals	3-17
3-13.	Memory-Controller-Fault Address Register (I/O Port Hex 00E4)	3-18
3-14.	Memory-Controller-Fault Address Registers (I/O Port Hex 00E5)	3-18
3-15.	RT/CMOS RAM Address Map	3-19
3-16.	RT/CMOS Address and NMI Mask Register (Hex 0070)	3-19
3-17.	RT/CMOS Data Register (Hex 0071)	3-20
3-18.	Real-Time Clock Bytes (Hex 000–00D)	3-21
3-19.	Status Register A (Hex 00A)	3-21
3-20.	Status Register B (Hex 00B)	3-22
3-21.	Status Register C (Hex 00C)	3-23
3-22.	Status Register D (Hex 00D)	3-23
3-23.	Diagnostic Status Byte (Hex 00E)	3-24
3-24.	Diskette Drive Type Byte (Hex 010)	3-25
3-25.	Diskette Drive Type Byte (Bits 7–4)	3-25
3-26.	Diskette Drive Type Byte (Bits 3–0)	3-25
3-27.	Equipment Byte (Hex 014)	3-26
3-28.	Installed Diskette Drive Bits	3-26
3-29.	Display Operating-Mode Bits	3-26
3-30.	System Control Port B (Hex 0061)—Write	3-29
3-31.	System Control Port B (Hex 0061)—Read	3-29
3-32.	System Control Port A (Hex 0092)	3-30
3-33.	POST Error Messages	3-35
A-1.	Instruction Cycle Times	A-1

Notices

References in this publication to IBM products, programs, or services do not imply that IBM intends to make these available in all countries in which IBM operates. Any reference to an IBM product, program or service is not intended to state or imply that only IBM's product, program, or service may be used. Any functionally equivalent product, program, or service that does not infringe any of IBM's intellectual property rights or other legally protectable rights may be used instead of the IBM product, program, or service. Evaluation and verification of operation in conjunction with other products, programs, or services, except those expressly designated by IBM, are the user's responsibility.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

Trademarks and Service Marks

The following terms, denoted by an asterisk (*) in this publication, are trademarks of the IBM Corporation in the United States and/or other countries:

IBM
Micro Channel
Personal Computer AT
Personal System/2
PS/2
XGA

The following terms, denoted by a double asterisk (**) in this publication, are trademarks of other companies as follows:

Intel	Intel Corporation
Motorola	Motorola, Incorporated

© Copyright IBM Corp. 1991, 1992

Notes:

Preface

The Technical Reference library is intended for those who develop hardware and software products for IBM Personal Computers and IBM Personal System/2 products. Users should understand computer architecture and programming concepts.

Additions and changes have been made since the second edition of this manual. New or changed information is marked in the text with the same mark that is in the margin of this text.

This manual consists of the following sections:

Section 1, "System Overview," describes the system, features, and specifications.

Section 2, "Programmable Option Select," describes the registers used for configuration.

Section 3, "System Board," describes the system-specific hardware implementations of the Micro Channel architecture.

This technical reference should be used with the following publications. These publications contain additional information on many of the subjects discussed in this technical reference.

IBM Personal System/2 Hardware Interface Technical Reference—Architectures

IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces

IBM Personal System/2 Hardware Interface Technical Reference—Video Subsystems

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference

Information about diskette drives, fixed disk drives, adapters, and external options are in separate option technical references.

Warning: The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

© Copyright IBM Corp. 1991, 1992

Notes:

Section 1. System Overview

| Description 1-3
| System Board Devices and System Features 1-4
| System Board I/O Address Map 1-8
| Micro Channel Compatibility 1-10
| Specifications 1-11
Power Supply 1-15
Outputs 1-16
Output Protection 1-17
Voltage Sequencing 1-17
Power Supply Connectors 1-17

© Copyright IBM Corp. 1991, 1992

Notes:

Description

The IBM* Personal System/2* (PS/2*) Model 56 systems are Micro Channel* systems. They are self-contained desktop computer systems with a keyboard. The systems can support a maximum of three internal drives. Two of these drives can be either removable-media direct access storage devices (DASD) (diskette, tape, optical), or nonremovable-media DASD devices. If there is a third device, it is a hidden nonremovable-media DASD device.

Programs can identify the system board by reading the model and submodel bytes. Interrupt 15H, function code (AH)=C0H, returns the model byte, submodel byte, and BIOS revision code. The microprocessor on Type 2 and Type 3 systems contains an internal cache and cache controller.

The following figure lists the model names, model and submodel bytes, system board types, and system-clock speed for all Model 56 system boards.

Model Name	Model Byte (Hex)	Submodel Byte (Hex)	System Board Type	System Clock
56 SX	F8	26	Type 1	20 MHz
56 SLC	F8	25	Type 2	20 MHz
56 486SLC2	F8	38	Type 3	25 MHz/50 MHz

Figure 1-1. Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems.

* Trademark of the IBM Corporation.

System Board Devices and System Features

The following figure lists the system board devices and system features for the 56 SX and the 56 SLC models. The *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* describes devices common to PS/2 products by type number.

Device	Type	Features
Microprocessor	—	Type 1 systems (56 SX models) - 80386SX - 24-bit address, 16-bit data interface Type 2 systems (56 SLC models) - IBM 386SLC - 24-bit address, 16-bit data interface - 8KB instruction and data cache with parity
System Timers	1	Channel 0-System timer Channel 2-Tone generation for speaker Channel 3-Watchdog timer
ROM Subsystem	—	128KB logical ROM (KB equals 1024 bytes) 256KB physical ROM
RAM Subsystem	—	Three connectors (4MB to 16MB) (MB equals 1048576 bytes) Connectors will accommodate 2MB, 4MB, and 8MB memory modules.
CMOS RAM Subsystem	—	64-byte CMOS RAM with real-time clock/calendar 8KB CMOS RAM extension Battery backup
Audio Subsystem	1	Driven by - System-timer channel 2 - The 'audio sum node' signal
DMA Controller	1	Eight independent DMA channels Single or burst transfers with read verification
Video Subsystem	1	16-bit VGA - 132-column text mode - Mainframe interactive (MFI) support

Figure 1-2 (Part 1 of 2). System Board Devices and System Features—56 SX and 56 SLC Models

Device	Type	Features
Interrupt Controller	1	16 levels of system interrupts Interrupts are level sensitive
Keyboard/Auxiliary Device Controller	2	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	2	Supports - 3.5-in. diskette drive (1.44MB and 2.88MB) - 5.25-in. diskette drive (360KB and 1.2MB)
Serial Controller Port	4	One RS-232C interface - One 25-pin connector Programmable as serial ports 1 – 16 DMA, FIFO, and character modes
Parallel Controller Port	3	Programmable as parallel port 1 – 4 Supports bidirectional input and output Supports DMA operation
SCSI Controller	1	Supports one internal SCSI device Supports up to seven total SCSI devices
Micro Channel Bus Adapter	—	Three connectors for Type 3 adapters - One 16-bit connector with an auxiliary video extension (slot 2) - Two 16-bit connectors
Math Coprocessor Socket	—	Supports 80387SX math coprocessor option with the same clock speed as the system microprocessor

Figure 1-2 (Part 2 of 2). System Board Devices and System Features—56 SX and 56 SLC Models

The following figure lists the system board devices and system features for the 56 486SLC2 models. The *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* describes devices common to PS/2 products by type number.

Device	Type	Features
Microprocessor	---	Type 3 systems (56 486SLC2 models) - IBM 486SLC2 - 24-bit address, 16-bit data interface - 16KB instruction and data cache with parity
System Timers	1	Channel 0-System timer Channel 2-Tone generation for speaker Channel 3-Watchdog timer
ROM Subsystem	---	128KB logical ROM (KB equals 1024 bytes) 256KB physical ROM
RAM Subsystem	---	Three connectors (8MB to 16MB) (MB equals 1048576 bytes) Connectors will accommodate 2MB, 4MB, and 8MB memory modules.
CMOS RAM Subsystem	---	64-byte CMOS RAM with real-time clock/calendar 8KB CMOS RAM extension Battery backup
EEPROM Subsystem	---	128-byte electrically-erasable programmable read-only memory (EEPROM) Unique system board identifier
Audio Subsystem	1	Driven by - System-timer channel 2 - The 'audio sum node' signal
DMA Controller	1	Eight independent DMA channels Single or burst transfers with read verification

Figure 1-3 (Part 1 of 2). System Board Devices and System Features—56 486SLC2 Models

Device	Type	Features
Video Subsystem	3	XGA*-2 video - VGA mode - Updated XGA modes - 132-column text mode - 1MB of video memory
Interrupt Controller	1	16 levels of system interrupts Interrupts are level sensitive
Keyboard/Auxiliary Device Controller	2	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	3	Supports - 3.5-in. diskette drive (1.44MB and 2.88MB) - 3.5-in. diskette drive (2.88MB with electronic eject) - 5.25-in. diskette drive (360KB and 1.2MB)
Serial Controller Port	4	RS-232C interface - Two 9-pin connectors Programmable as serial ports 1 – 16 DMA, FIFO, and character modes
Parallel Controller Port	3	Programmable as parallel port 1 – 4 Supports bidirectional input and output Supports DMA operation
SCSI Controller	1	Supports up to two internal SCSI devices Supports up to seven total SCSI devices
Micro Channel Bus Adapter	---	Three connectors for Type 3 adapters - One 16-bit connector with an auxiliary video extension (slot 2) - Two 16-bit connectors
Math Coprocessor Socket	---	Supports 80387SX math coprocessor option with the same clock speed as the system microprocessor

Figure 1-3 (Part 2 of 2). System Board Devices and System Features—56 486SLC2 Models

* Trademark of the IBM Corporation.

System Board I/O Address Map

The following figure is the Model 56 system board I/O address map.

Address (Hex)	Device
0000–001F	DMA controller (0–3)
0020, 0021	Interrupt controller
0040, 0042–0044, 0047	System timers
004B–004F	32-bit free running timer (Type 3 system board only)
0060	Keyboard, auxiliary device
0061	System Control Port B
0064	Keyboard, auxiliary device
0066–0067	Keyboard, auxiliary device
0070, 0071	RT/CMOS and NMI mask
0074, 0075, 0076	8K *x*8 NVRAM
0078–007C	Reserved
0081–0083, 0087	DMA Page registers (0–3)
0089–008B, 008F	DMA Page registers (4–7)
0090	Central arbitration control point
0091	Card Selected Feedback register
0092	System Control Port A
0094	System Board Enable/Setup register
0096	Adapter Enable/Setup register
00A0, 00A1	Interrupt controller
00C0–00DF	DMA controller (4–7)
00E0–00E5	Memory controller
00F0–00FF	Math coprocessor
0100–0107	Programmable option select
0278–027D	Parallel Port 3
02F8–02FF	Serial Port 2
0378–037D	Parallel Port 2
03B4, 03B5, 03BA	Video subsystem
03BC–03BF	Parallel Port 1
03C0–03C5	Video subsystem
03C6–03C9	Video DAC
03CA, 03CC, 03CE, 03CF	Video subsystem
03D4, 03D5, 03DA	Video subsystem
03F0–03F7	Diskette drive controller
03F8–03FF	Serial Port 1
1278–127D	Enhanced Parallel Port 1
1378–137D	Parallel Port 4

Figure 1-4 (Part 1 of 2). System Board I/O Address Map

Address (Hex)	Device
2100 – 210F	XGA video instance 0
2110 – 211F	XGA video instance 1
2120 – 212F	XGA video instance 2
2130 – 213F	XGA video instance 3
2140 – 214F	XGA video instance 4
2150 – 215F	XGA video instance 5
2160 – 216F	XGA video instance 6
2170 – 217F	XGA video instance 7
3220 – 3227	Serial Port 3
3228 – 322F	Serial Port 4
3540 – 3547	SCSI controller
3A20 – 3A27	Serial Port 9
3A28 – 3A2F	Serial Port 10
3A30 – 3A37	Serial Port 11
3A38 – 3A3F	Serial Port 12
3A80 – 3A87	Serial Port 13
3A88 – 3A8F	Serial Port 14
3A90 – 3A97	Serial Port 15
3A98 – 3A9F	Serial Port 16
4220 – 4227	Serial Port 5
4228 – 422F	Serial Port 6
4620 – 462F	Serial port arbitration-level control
5220 – 5227	Serial Port 7
5228 – 522F	Serial Port 8
82F8 – 82FF	Enhanced Serial Port 2
83F8 – 83FF	Enhanced Serial Port 1
B220 – B227	Enhanced Serial Port 3
B228 – B22F	Enhanced Serial Port 4
BA20 – BA27	Enhanced Serial Port 9
BA28 – BA2F	Enhanced Serial Port 10
BA30 – BA37	Enhanced Serial Port 11
BA38 – BA3F	Enhanced Serial Port 12
BA80 – BA87	Enhanced Serial Port 13
BA88 – BA8F	Enhanced Serial Port 14
BA90 – BA97	Enhanced Serial Port 15
BA98 – BA9F	Enhanced Serial Port 16
C220 – C227	Enhanced Serial Port 5
C228 – C22F	Enhanced Serial Port 6
D220 – D227	Enhanced Serial Port 7
D228 – D22F	Enhanced Serial Port 8

Figure 1-4 (Part 2 of 2). System Board I/O Address Map

Micro Channel Compatibility

The following terms describe system limitations supporting Micro Channel.

Streaming Data

The system board supports 10-MHz streaming-data procedures involving transfers between adapters; but the devices on the system board do not *use* the streaming-data procedures. Transfers default to the basic transfer procedure.

Data Parity

The system board supports data-parity procedures involving transfers between adapters; but the devices on the system board do not *use* the data-parity procedures. Transfers default to the basic transfer procedure.

Select Feedback Return Indicator (Port Hex 91)

The system board supports the 'selected feedback return' indicator except for the I/O devices at addresses below hex 0100. These devices are controlled by the system master only and should not be accessed by bus masters.

Synchronous Channel Check

Synchronous channel checks for errors other than Micro Channel data-parity errors are not supported in this system.

Synchronous channel checks for data-parity errors, typically issued by slaves, are the responsibility of the master that owned the channel and issued the access to the slave. However, in this system, these channel checks are detected by logic on the system board, resulting in a nonmaskable interrupt (NMI).

DMA

In this system, the DMA controller supports DMA slaves with 8-bit or 16-bit data widths.

Specifications

The following figure contains the performance specifications for the 56 SX and the 56 SLC models.

Device	Cycle Time (ns)
Microprocessor (20 MHz—50 ns Clock)	
Pipelined access to system board RAM†	
Memory read/write (page hit)	100
Memory read/write (page miss/bank miss)	150
Memory read/write (page miss)	200
Nonpipelined access to system board RAM†	
Memory read/write (page hit)	150
Memory read/write (page miss/bank miss)	200
Memory read/write (page miss)	250
Access to Channel	
Default transfer cycle	250
Synchronous transfer cycle	350
Access to ROM	200
Refresh Rate (typically performed every 15.1 μs)	500 (min) 800 (typical)
Bus-Master Access to System Board RAM	
Page hit	320 (min)
Page miss	370 (min)
DMA Controller (10 MHz—100 ns Clock)	
Single transfer: 300 + (I/O access + memory access)	
Burst transfer: 300 + (I/O access + memory access)*n*‡	
System board memory access	200—350
Default transfer cycle	350 (min)
Synchronous transfer cycle	450 (min)

† Adapters installed in the channel should not rely on monitoring system board memory access, because channel-memory control signals might not be present during these accesses.

‡ *n* equals the number of transfers in the burst.

Note: The cycle times shown for access to system board RAM are based on 70-nanosecond memory.

Figure 1-5. Performance Specifications—56 SX and 56 SLC Models

The following figure contains the performance specifications for the 56 486SLC2 models.

Device	Cycle Time (ns)
Microprocessor (25 MHz—40 ns Clock)	
Pipelined access to system board RAM†	
Memory read/write (page hit)	80
Memory read/write (page miss/bank miss)	120
Memory read/write (page miss)	160
Nonpipelined access to system board RAM†	
Memory read/write (page hit)	120
Memory read/write (page miss/bank miss)	160
Memory read/write (page miss)	200
Access to Channel	
Default transfer cycle	240
Synchronous transfer cycle	320
Access to ROM	200
Refresh Rate (typically performed every 15.1 μs)	400 (min) 640 (typical)
Bus-Master Access to System Board RAM	
Page hit	300 (min)
Page miss	320 (min)
DMA Controller (12.5 MHz—80 ns Clock)	
Single transfer: 240 + (I/O access + memory access)	
Burst transfer: 240 + (I/O access + memory access)*n*‡	
System board memory access	160 – 320
Default transfer cycle	305 (min)
Synchronous transfer cycle	405 (min)

† Adapters installed in the channel should not rely on monitoring system board memory access, because channel-memory control signals might not be present during these accesses.

‡ *n* equals the number of transfers in the burst.

Note: The cycle times shown for access to system board RAM are based on 70-nanosecond memory.

Figure 1-6. Performance Specifications—56 486SLC2 Models

The following figure describes the physical specifications of the 56 SX and the 56 SLC models.

Specification	Measurements
Size	
Width	360 mm (14.2 in.)
Depth	395 mm (15.6 in.)
Height	115 mm (4.5 in.)
Weight	
Minimum configuration	
56 SX and 56 SLC models	10.9 kg (24.0 lb)
56 LS and 56 SLC LS models	9.6 kg (21.1 lb)
Maximum configuration	11.8 kg (26 lb)
Cables	
Power cable	1.8 m (6 ft)
Keyboard cable	2.7 m (9 ft)
Air Temperature	
System on	10.0 to 35.0°C (50 to 95°F) 0 – 7000 ft
System off	10.0 to 43.0°C (50 to 110°F)
Humidity	
System on	8% to 85%
System off	8% to 80%
Maximum Altitude	2133.6 m (7000 ft)
Heat Output	(196 watts) 671 BTU/Hr
Acoustical Readings	See Figure 1-9 on page 1-15
Electrical	
Input voltage (range is automatically selected; sinewave input is required)	
Low range	90 (min) – 137 (max) V ac
High range	180 (min) – 265 (max) V ac
Input frequency	50 ± 3 Hz or 60 ± 3 Hz
Maximum current draw	
Low range	4.6 A
High range	2.0 A
Input in kilovolt-ampere (kVA)	
Minimum configuration (as shipped by IBM)	0.0063 kVA
Maximum configuration	0.30 kVA
Electromagnetic Compatibility	FCC Class A (When the 56 LS and 56 SLC LS are connected to Token-Ring Network) FCC Class B

Figure 1-7. Physical Specifications—56 SX and 56 SLC Models

The following figure describes the physical specifications of the 56 486SLC2 models.

Specification	Measurements
Size	
Width	360 mm (14.2 in.)
Depth	395 mm (15.6 in.)
Height	115 mm (4.5 in.)
Weight	
Minimum configuration	11.8 kg (26 lb)
Maximum configuration	13.6 kg (30 lb)
Cables	
Power cable	1.8 m (6 ft)
Keyboard cable	2.7 m (9 ft)
Air Temperature	
System on	10.0 to 35.0°C (50 to 95°F) 0 – 3000 ft 10.0 to 32.2°C (50 to 90°F) 3000 – 7000 ft
System off	10.0 to 43.0°C (50 to 110°F)
Humidity	
System on	8% to 85%
System off	5% to 85%
Maximum Altitude	2133.6 m (7000 ft)
Heat Output as shipped	(35 watts) 123 BTUs per hour
Maximum configuration	(250 watts) 875 BTUs per hour
Acoustical Readings	See Figure 1-9 on page 1-15
Electrical	
Input voltage (range is automatically selected; sinewave input is required)	
Low range	90 (min) – 137 (max) V ac
High range	180 (min) – 265 (max) V ac
Input frequency	50 ± 3 Hz or 60 ± 3 Hz
Power Supply	118 watts
Maximum current draw	
Low range	3.5 A
High range	1.75 A
Input in kilovolt-ampere (kVA)	
Minimum configuration (as shipped by IBM)	0.06 kVA
Maximum configuration	0.35 kVA
Electromagnetic Compatibility	FCC Class B

Figure 1-8. Physical Specifications—56 486SLC2 Models

| The following figure contains the acoustical readings for all Model 56 | systems.

Description	L_{WAd} in bels Operate	Idle	L_{pAm} in dB Operate	Idle	$<L_{pA}>_m$ in dB Operate	Idle
Model 56	5.1	5.0	42	41	36	36

Notes

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

All measurements are made in accordance with ANSI standard 12.10 and reported in conformance with ISO DIS 9296.

The measurements are preliminary data and subject to change.

Figure 1-9. Acoustical Readings

Power Supply

The power supply converts the ac input voltage to three dc output voltages and provides power for the following:

- System board
- Micro Channel adapters
- Internal DASD drives
- Auxiliary devices
- Keyboard

The power switch and two light-emitting diodes (LED) are on the front of the system unit. The power supply is operating properly when the green LED is lit. The amber LED is the fixed-disk-activity indicator.

Outputs

The power supply provides separate voltage sources for the system board and the drives. The system board voltages are +5 V dc, +12 V dc, and −12 V dc. The drive voltages are +5 V dc and +12 V dc.

The following figure shows the maximum current provided for system components.

System Component	Maximum Current	
	+12 V dc	+5 V dc
Internal fixed disk drives†	2.8 A	2.71 A
Auxiliary device	None	300 mA
Keyboard	None	275 mA
† Total for two power-supply connectors.		

Figure 1-10. Component Maximum Current

The following figure shows the maximum load currents allowed for each channel connector.

Supply Voltage	Maximum Load Current
+ 5.0 V dc	1.6 A
+12.0 V dc	0.175 A
−12.0 V dc	0.040 A

Figure 1-11. Channel Load Current

The formulas used to determine the power requirements and the voltage regulation tolerances are in the Micro Channel architecture information in the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures.*

Output Protection

A short circuit placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state, with no damage to the power supply.

If an overvoltage fault occurs in the power supply, the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of the nominal value of the power supply.

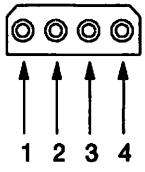
If either of these shutdown states occurs, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least ten seconds.

Voltage Sequencing

During power-on, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Power Supply Connectors

The power supply provides two 4-pin connectors for internal devices. The total power used by both connectors must not exceed the amount shown in Figure 1-10 on page 1-16.



Pin	Signal	Pin	Signal
1	+12 V dc	3	dc return
2	dc return	4	+5 V dc

Figure 1-12. Voltage Assignments for the Internal Power-Supply Connectors

Notes:

Section 2. Programmable Option Select

| Description 2-3
POS Address Map 2-5
Card Selected Feedback Register (Hex 0091) 2-6
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-7
System Board Group 1 POS Register 2 (Hex 0102) 2-8
| System Board Group 1 POS Register 3 (Hex 0103) 2-10
System Board Group 1 POS Register 4 (Hex 0104) 2-11
System Board Group 1 POS Register 5 (Hex 0105) 2-11
| System Board Group 2 POS Register 2 (Hex 0102) 2-12
| System Board Group 2 POS Register 3 (Hex 0103) 2-12
System Board Group 3 POS Register 4 (Hex 0104) 2-13
System Board SCSI Controller POS Register 2 (Hex 0102) . . 2-13
System Board SCSI Controller POS Register 3 (Hex 0103) . . 2-14
Adapter Enable/Setup Register (Hex 0096) 2-14

© Copyright IBM Corp. 1991, 1992

Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used on all Model 56 system boards. For additional POS information, refer to the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures.*

Warning:

- IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignments of the same system resource, improper operation of the feature, loss of data, or damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention occurs, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- The channel-reset bit (bit 7) in the Adapter Enable/Setup register (hex 0096) must be set to 0 to program the adapters.
- The system board does not support 16-bit I/O operations to 8-bit POS registers. Using 16-bit I/O instructions on 8-bit POS registers causes incorrect data to be written to or read from the registers. Only 8-bit transfers are supported for setup operations.

Setup functions respond to I/O addresses hex 0100 through hex 0107 only when their unique setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

System Board Video Subsystem Setup:

- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 0 to place the system board video into the setup mode.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bits 7, 6, 4, and 3 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system board functions.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register must be set to 1 to allow adapter setup.
- Bits 7–3 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to system board or video subsystem functions.

System Board Setup Group 1:

- Bit 7 in the System Board Enable/Setup register must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bits 6–3 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem or other system board functions.

System Board Setup Group 2:

- Bit 6 in the System Board Enable/Setup register must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bits 7, 5, 4, and 3 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem or other system board functions.

System Board Setup Group 3:

- Bit 4 in the System Board Enable/Setup register must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bits 7, 6, 5, and 3 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem or other system board functions.

System Board SCSI Controller Setup:

- Bit 3 in the System Board Enable/Setup register must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bits 7–4 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem or other system board functions.

POS Address Map

The following figure shows the organization of the I/O address space used by POS. Bit 0 of POS Register 2 and bits 6 and 7 of POS Register 5 are fixed. All other bits in POS Registers 2 through 5 are free form.

Address (Hex)	Function
0094	System Board Enable/Setup register
0096	Adapter Enable/Setup register
0100	POS Register 0—Adapter Identification byte (low byte)
0101	POS Register 1—Adapter Identification byte (high byte)
0102	POS Register 2—Option Select Data byte 1 – Bit 0 is card enable
0103	POS Register 3—Option Select Data byte 2
0104	POS Register 4—Option Select Data byte 3
0105	POS Register 5—Option Select Data byte 4
0106	Reserved
0107	Reserved

Figure 2-1. POS I/O Address Map

Card Selected Feedback Register (Hex 0091)

Whenever an adapter is addressed, it responds by setting the '-card selected feedback' (-CD SFDBK) signal to active. -CD SFDBK is derived from the address decode, driven by a totem-pole driver, and latched by the system board. It can be read through the Card Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs can use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and determine if the video subsystem, system board I/O, or an adapter is addressed and functioning.

Bit	Function
7–1	Reserved
0	Card selected feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7–1 These bits are reserved.

Bit 0 This bit is set to 1 whenever -CD SFDBK was active on a previous cycle or whenever the system board I/O functions (diskette drive, serial, or parallel interfaces) are accessed by an I/O cycle. Reading this register resets the bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information during setup. The diskette drive controller, serial port, and parallel port are treated as a single device. The video subsystem also is an integrated part of the system board, but POS treats it as a separate device. The System Board Enable/Setup register is used to place the system board or the video subsystem in the setup mode.

Figure 2-3 indicates the group, POS register number, and I/O function supported.

Group	POS Register	Device
1	2	Diskette drive Parallel port controllers
1	3	Memory connectors
1	4	Diskette arbitration level
1	5	Parallel port arbitration level
2	2, 3	Serial port controller
3	4	SCSI controller arbitration level
SCSI Controller	2, 3	Enable SCSI controller

Figure 2-3. Devices Supported in Setup Mode

System Board Enable/Setup Register (Hex 0094)

This is a read/write register. All bits in this register default to 1 (enabled).

Bit	Function
7	Enable/setup system board group 1
6	Enable/setup system board group 2
5	Enable/setup video subsystem
4	Enable/setup system board group 3
3	Enable/setup SCSI controller
2–0	Reserved

Figure 2-4. System Board Enable/Setup Register (Hex 0094)

Bit 7 When this bit is set to 0, it places the diskette drive controller, parallel port controllers, memory connectors, diskette arbitration level, and parallel port arbitration level in setup mode.

When this bit is set to 1, it enables the system board functions.

Bit 6 When this bit is set to 0, it places the system board serial controller in setup mode. System Board Group 2 POS Register 2 (hex 0102) includes the serial port enable and interrupt-level selection. The serial port address selection is in System Board Group 2 POS Register 3 (hex 0103).

Bit 5 When this bit is set to 0, the video subsystem is placed in the setup mode and controlled through Group 1 POS Register 2 (hex 0102). When this bit is set to 1 and bit 0 in Group 1 POS Register 2 is set to 1, video is enabled.

Bit 0 of Group 1 POS Register 2 is the video-enable bit. When this bit is set to 0, the video subsystem does not respond to commands, addresses, or data. If video is being generated when the video-enable bit is set to 0, the output is still generated. For information on BIOS calls to enable or disable the video, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*.

Note: When the video subsystem is disabled, access to the Digital-to-Analog Converter (DAC) registers is disabled.

Bit 4 When this bit is set to 0, the system board bus controller is placed in setup mode and controlled through POS Register 4 (hex 0104). POS Register 4 includes the system board SCSI-controller arbitration level. All other bits in POS Register 4 and POS Register 5 are reserved.

Bit 3 When this bit is set to 0, the system board SCSI controller is placed in setup mode and is controlled through POS Register 2 (hex 0102). When this bit is set to 1 and bit 0 in POS Register 2 is set to 1, the system board SCSI controller is enabled.

Bits 2–0 These bits are reserved.

System Board Group 1 POS Register 2 (Hex 0102)

When the system board is in the setup mode, this read/write register controls the diskette drive controller, serial port, and parallel port. Reading this register returns the current state of these system board functions.

Bit	Function
7	Disable parallel port extended mode
6, 5	Select parallel port
4	Enable parallel port
3	Reserved
2	Reserved
1	Enable diskette drive interface
0	Enable system board

Figure 2-5. System Board POS Register 2 (Hex 0102)

Bit 7 When this bit is set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional (extended mode) interface. When this bit is set to 1, this bit disables the bidirectional mode. This bit is set to 0 after power-on.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Hex Address	Interrupt Level
0 0	Parallel 1	03BC–03BF†	7
0 1	Parallel 2	0378–037D	7
1 0	Parallel 3	0278–027D	7
1 1	Parallel 4	1378–137D	7

† The addresses are hex 1278–127D for the DMA operations.

Figure 2-6. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bits 3, 2 These bits are reserved.

Bit 1 When this bit and bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When this bit is set to 1, bits 4 and 1 can enable and disable their respective devices. When this bit is set to 0, this bit disables the diskette drive interface and system board serial and parallel ports, regardless of the state of bits 4 and 1.

System Board Group 1 POS Register 3 (Hex 0103)

The system board has connectors that provide for installation of three single inline memory modules (memory modules) (for more information about these memory connectors, see "System Board Memory Connectors" on page 3-11). Information about each memory module is contained in four read-only data bits in POS Register 3. Each set of data bits is selected by writing the appropriate index to the write-only index register.

POS Register 3 provides access to the read-only data bits and a write-only index register. To determine the memory information for a particular connector, write the appropriate index to POS Register 3, then read POS Register 3. The following figure shows the relationship of the index value, the memory connector, and the available data register information.

Index Value (Hex)	Function
00	Presence detection information for memory connectors 2 and 1
04	Presence detection information for memory connector 3

Note: All values that are not shown are reserved.

Figure 2-7. System Board Group 1 POS Register 3 (Hex 0103)—Write

The following information is returned by reading POS Register 3 after the appropriate index value has been written to POS Register 3. For coding of the presence detection signals, see Figure 3-9 on page 3-15.

Index 00 Bit	Function
7	Presence detect 3, memory connector 2
6	Presence detect 2, memory connector 2
5	Presence detect 1, memory connector 2
4	Presence detect 0, memory connector 2
3	Presence detect 3, memory connector 1
2	Presence detect 2, memory connector 1
1	Presence detect 1, memory connector 1
0	Presence detect 0, memory connector 1

Figure 2-8. System Board POS Group 1 Register 3 (Hex 0103)—Read Index 00

Index 04 Bit	Function
7–4	Reserved
3	Presence detect 3, memory connector 3
2	Presence detect 2, memory connector 3
1	Presence detect 1, memory connector 3
0	Presence detect 0, memory connector 3

Figure 2-9. System Board POS Group 1 Register 3 (Hex 0103)—Read Index 04

System Board Group 1 POS Register 4 (Hex 0104)

This register is used to specify the diskette arbitration level.

Bit	Function
7–4	Reserved
3–0	Diskette arbitration level

Figure 2-10. System Board Group 1 POS Register 4 (Hex 0104)

Bits 7–4 These bits are reserved.

Bits 3–0 These bits select the diskette arbitration level.

System Board Group 1 POS Register 5 (Hex 0105)

This register is used to specify the arbitration level used by the parallel port controller.

Bit	Function
7–4	Reserved
3–0	Parallel port arbitration level

Figure 2-11. System Board Group 1 POS Register 5 (Hex 0105)

Bits 7–4 These bits are reserved.

Bits 3–0 These bits are used to select the arbitration level used by the parallel port controller.

System Board Group 2 POS Register 2 (Hex 0102)

This register is used to enable the system board serial ports.

Bit	Function
7–6	Reserved
5	Enable Serial Port B
4	Enable Serial Port A
3–2	Reserved
1	Select Serial Port B interrupt
0	Select Serial Port A interrupt

Figure 2-12. System Board Group 2 POS Register 2 (Hex 0102)

Bits 7–6 These bits are reserved.

Bit 5 When this bit is set to 1 and bit 0 in POS Register 2 (Group 1) is set to 1, Serial Port B is enabled.

Bit 4 When this bit is set to 1 and bit 0 in POS Register 2 (Group 1) is set to 1, Serial Port A is enabled.

Bit 3–2 These bits are reserved.

Bit 1 When this bit is set to 1, Serial Port B uses IRQ4. When this bit is set to 0, Serial Port B uses IRQ3.

Bit 0 When this bit is set to 1, Serial Port A uses IRQ4. When this bit is set to 0, Serial Port A uses IRQ3.

System Board Group 2 POS Register 3 (Hex 0103)

This register is used to select the address of the serial ports.

Bit	Function
7–4	Serial Port B address
3–0	Serial Port A address

Figure 2-13. System Board Group 2 POS Register 3 (Hex 0103)

Bits 7–4 These bits are used to determine the address of Serial Port B.

Bits 3–0 These bits are used to determine the address of Serial Port A.

Bits 7 6 5 4 3 2 1 0	Assignment	Hex Address	
		Compatible	Extended
0 0 0 0	Serial 1	03F8 – 03FF	83F8 – 83FF
0 0 0 1	Serial 2	02F8 – 02FF	82F8 – 82FF
0 0 1 0	Serial 3	3220 – 3227	B220 – B227
0 0 1 1	Serial 4	3228 – 322F	B228 – B22F
0 1 0 0	Serial 5	4220 – 4227	C220 – C227
0 1 0 1	Serial 6	4228 – 422F	C228 – C22F
0 1 1 0	Serial 7	5220 – 5227	D220 – D227
0 1 1 1	Serial 8	5228 – 522F	D228 – D22F
1 0 0 0	Serial 9	3A20 – 3A27	BA20 – BA27
1 0 0 1	Serial 10	3A28 – 3A2F	BA28 – BA2F
1 0 1 0	Serial 11	3A30 – 3A37	BA30 – BA37
1 0 1 1	Serial 12	3A38 – 3A3F	BA38 – BA3F
1 1 0 0	Serial 13	3A80 – 3A87	BA80 – BA87
1 1 0 1	Serial 14	3A88 – 3A8F	BA88 – BA8F
1 1 1 0	Serial 15	3A90 – 3A97	BA90 – BA97
1 1 1 1	Serial 16	3A98 – 3A9F	BA98 – BA9F

Figure 2-14. Serial Port Addresses

System Board Group 3 POS Register 4 (Hex 0104)

This register is used to select the arbitration level of the SCSI controller on the system board.

Bit	Function
7 – 4	SCSI arbitration level (system board)
3 – 0	Reserved

Figure 2-15. System Board Group 3 POS Register 4 (Hex 0104)

Bits 7 – 4 These bits select the SCSI arbitration level.

Bits 3 – 0 These bits are reserved.

System Board SCSI Controller POS Register 2 (Hex 0102)

This register is used to enable the system board SCSI controller.

Bit	Function
7 – 1	Reserved
0	Enable SCSI

Figure 2-16. System Board SCSI Controller POS Register 2 (Hex 0102)

Bits 7–1 These bits are reserved.

Bit 0 When this bit is set to 1, this bit enables the system board SCSI controller.

System Board SCSI Controller POS Register 3 (Hex 0103)

This register is used to select the SCSI ID for the system board SCSI controller.

Bit	Function
7–5	SCSI ID
4–0	Reserved

Figure 2-17. System Board SCSI Controller POS Register 3 (Hex 0103)

Bits 7–5 These bits determine the SCSI ID for the system board SCSI controller as follows:

Bits 7 6 5	System Board SCSI ID
0 0 0	0
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	4
1 0 1	5
1 1 0	6
1 1 1	7

Figure 2-18. System Board SCSI Controller ID

Bits 4–0 These bits are reserved.

Adapter Enable/Setup Register (Hex 0096)

This read/write register resets the channel, enables the '-card setup' signal, and configures the connectors.

Bit	Function
7	Channel reset
6–4	Reserved
3	Enable card setup
2–0	Channel select 2–0

Figure 2-19. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When this bit is set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6–4 These bits are reserved and must be set to 0.

Bit 3 When this bit is set to 1, this bit enables the '-card setup' signal selected by bits 2–0.

Bits 2–0 These bits are the address bits for the '-card setup' signal to the connectors. Connectors 1 through 5 are addressed as 0 through 4. When bit 3 is set to 1, these bits select the connector or function for setup cycles.

Each channel connector has a unique '-card setup' signal (-CD SETUP) associated with it. This signal is used to select the adapters for setup cycles, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Note: -CD SETUP goes active only when an operation is performed in the I/O address range hex 0100 through 0107.

Notes:

Section 3. System Board

| Description 3-3
Microprocessor—Type 1 Systems 3-3
Microprocessor—Type 2 Systems 3-3
Programming Model 3-4
Instructions 3-4
| Microprocessor—Type 3 Systems 3-4
Cache Operation 3-5
Cacheable Address Space 3-6
Math Coprocessor 3-6
Micro Channel Implementation 3-6
Central Arbiter 3-6
Arbitration Bus Priority Assignments 3-7
Central Arbiter Programming 3-8
Bus Adapter 3-9
| Diskette Drive Connector 3-10
System Board Memory Connectors 3-11
| SCSI-Device Connector 3-12
Memory 3-13
ROM Subsystem 3-14
| RAM Subsystem 3-14
| Memory Interleaving Option 3-15
| Memory-Presence Detect Signals 3-15
| System Memory Map 3-16
Memory Controller Registers 3-16
Memory-Fault RAS Capture Register (I/O Port Hex 00E2) . 3-17
Memory-Controller-Fault Address Registers (I/O Ports Hex 00E4 and Hex 00E5) 3-17
RT/CMOS RAM 3-18
RT/CMOS Address and NMI Mask Register (Hex 0070) . . 3-19
RT/CMOS Data Register (Hex 0071) 3-20
RT/CMOS RAM I/O Operations 3-20
Real-Time Clock Bytes (Hex 000—00D) 3-21
CMOS RAM Configuration 3-24
NVRAM 3-28
| Vital Product Data 3-28
Miscellaneous System Functions and Ports 3-28
| Nonmaskable Interrupt 3-28
System Control Port B (Hex 0061) 3-29
System Control Port A (Hex 0092) 3-30
| Power-On Password 3-31
| Privileged-Access Password 3-32
Keyboard Password 3-32

© Copyright IBM Corp. 1991, 1992

| Cover Lock and Tamper-Evident Switch 3-32
| Selectable Boot Sequence 3-32
Hardware Compatibility 3-33
| Error Codes 3-34

Description

This section describes the microprocessors, math coprocessor, channel differences, memory subsystems, and miscellaneous system ports and connectors for the all Model 56 systems. Additional information on these topics can be found in the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces.*

Type 1 systems contain an 80386SX microprocessor, Type 2 systems contain a 386SLC microprocessor, and Type 3 systems contain a 486SLC2 microprocessor. To identify the microprocessor used in the system unit, use INT 15H, function code 0C9H. This returns the microprocessor type and stepping level.

Microprocessor—Type 1 Systems

The 80386SX microprocessor used in Type 1 systems runs at 20 MHz and has a 24-bit address and a 16-bit data interface. The 80386SX microprocessor is software compatible with the 80386DX microprocessor. The type for the 80386SX is hex 023.

Microprocessor—Type 2 Systems

The 386SLC microprocessor used in Type 2 systems runs at 20 MHz and has an 8KB, 2-way set-associative store-through instruction and data cache. It contains an internal 32-bit data path (including the path to the cache) with external 16-bit data and 24-bit address paths. The 386SLC maintains binary compatibility with programs written for the 80386SX. The type for the IBM 386SLC is hex 0A3.

Programming Model

The IBM 386SLC microprocessor implements the same registers and bit descriptions as the Intel** 80386SX with the following additions:

- The 386SLC implements the WP bit in the CR0 of the Intel486** microprocessor.
- The 386SLC implements the PCD bit in the Page Table Entry of the Intel486 microprocessor.

Instructions

The 386SLC microprocessor decodes the same instructions as the 80386SX. The 386SLC microprocessor also decodes the following 6 Intel486 instructions:

- BSWAP
- XADD
- CMPXCHG
- INVD
- WBINVD
- INVLPG

Microprocessor—Type 3 Systems

The 486SLC2 microprocessor used in Type 3 systems runs at 50 MHz internally and 25 MHz externally. It has a 24-bit address and a 16-bit data interface. The 486SLC2 microprocessor is software compatible with the 80486SX microprocessor, the 80386DX microprocessor, and the 80386SX microprocessor. The type for the 486SLC2 is hex 0A4.

** Trademark of Intel Corporation.

Cache Operation

The cache in the 386SLC microprocessor (8KB) and the 486SLC2 microprocessor (16KB) enables it to read instructions and data much faster than if the microprocessor had to access system memory. When instructions are first used or data is first read or written, they are transferred to the cache from main memory. This enables future accesses to the instructions or data to occur much faster.

The cache is disabled and empty when the microprocessor comes out of the reset state. The cache is tested and enabled during the power-on self-test (POST).

The cache is loaded from system memory in 16-byte increments. These increments are referred to as a cache line. A cache line is aligned on a paragraph boundary. A reference to any byte contained in the line results in the entire cache line being read into the cache (if the data was not already in the cache). When the microprocessor gives up control of the system bus, the cache enters a "snoop" mode and monitors all write operations. If a memory write occurs to a location that is in the cache, the corresponding cache line is invalidated.

When the microprocessor performs a memory read, the address is used to find the data in the cache. If the data is found (a hit), it is read from the cache and no external bus cycle occurs. If the data is not found (a miss), an external bus cycle is used to read the data from system memory. If the address of the missed data is in cacheable address space, the data is stored in the cache and the rest of the cache line is read.

When the microprocessor performs a memory write, the address is used to search the cache. If found, the data is written to the cache. Then (hit or miss), an external bus cycle is used to write the data to system memory. If the address of the write operation was not in the cache but was in cacheable address space, the data is read back into the cache and the rest of the cache line is read.

Cacheable Address Space

Cacheable address space is defined as system memory that resides on the system board (0–640KB and 1MB–16MB). Nothing in the address range hex A0000–DFFFF is cached, and no memory that is located in any Micro Channel slot is cached. Nothing in the I/O address space is cached.

ROM address space (hex E0000–FFFFF) is cacheable for *read operations only*. If data in this address range is already in cache and the address range is written to, the cached line is invalidated and is read again from the ROM.

Math Coprocessor

The 80387SX math coprocessor is matched to the speed of the system microprocessor and operates in the synchronous mode. The 80387SX math coprocessor is software compatible with the 80387DX math coprocessor.

Micro Channel Implementation

This section describes the implementation of the Micro Channel architecture on Model 56 systems. For general Micro Channel architecture information, refer to the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures*.

Central Arbiter

The central arbitration control point gives programmable subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. The central arbiter supports up to 15 arbitrating devices (levels 0 through E) and the system microprocessor (level F).

Note: The system board SCSI controller performs cycles at arbitration level F if the Micro Channel arbitration level is F when the SCSI controller requests the bus.

Arbitration Bus Priority Assignments

The following figure shows the assignment of arbitration levels. The functions with the *lowest* arbitration level have the *highest* priority.

ARB Level	Primary Assignment
−2	Memory refresh
−1	NMI
0	DMA channel 0 (Programmable to any arbitration level)
1	DMA channel 1
2	DMA channel 2
3	DMA channel 3
4	DMA channel 4 (programmable to any arbitration level)
5	DMA channel 5
6	DMA channel 6
7	DMA channel 7
8−E	Available
F	System microprocessor

Figure 3-1. Arbitration Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so that diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, normally on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation, and by the previous controlling master. To prevent overrun, the diskette drive controller should not be held inactive for more than 12 microseconds.

Nonmaskable interrupt (NMI) service is executed at a priority level higher than 0, called −1. Memory refresh is prioritized at −2, two levels higher than 0. Levels −1 and −2 are reached on the system board only, while the 'arbitrate/-grant' signal (ARB/-GNT) is in the arbitration state.

When the central arbitration control point receives a level −1 request (NMI, a system board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level −1 request and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following figures.

Bit	Function
7	Enable system microprocessor cycle
6	Arbitration mask
5	Enable extended arbitration (not supported)
4–0	Reserved

Figure 3-2. Arbitration Register (Hex 0090)—Write

Bit	Function
7	Enable system microprocessor cycle
6	Arbitration masked by NMI
5	Bus time-out
4	Reserved
3–0	Value of arbitration bus during previous grant state

Figure 3-3. Arbitration Register (Hex 0090)—Read

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 1 by POST.

Reading this bit as a 1 indicates that the system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Note: On 56 models that have a Type 3 system board (all 486SLC2 models) reading this bit as a 1 indicates that a bus timeout has occurred, and has masked arbitration. This bit will not be set in response to a memory parity error or channel check.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 enables extended arbitration. The minimum arbitration cycle is 300 nanoseconds; this bit extends that minimum cycle to 600 nanoseconds. This bit is set to 0 during POST.

Reading this bit as a 1 indicates that a bus time-out has occurred and resets bit 6 in this register to 0.

Bit 4 This bit is reserved and must be set to 0.

Bits 3–0 These bits are undefined for a write operation and must be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Bus Adapter

The Model 56 uses a direct bus attachment board to provide three channel connectors:

- Two 16-bit Micro Channel connectors
- One 16-bit Micro Channel connector with an auxiliary video extension.

The adapters are installed horizontally into the direct bus attachment board.

Diskette Drive Connector

The diskette drive cable connects to the system board and provides two 2- by 17-pin connectors for attaching internal diskette drives. Each connector passes control and data signals between the diskette drive controller on the system board and the drives. It also provides the power to each drive.

The following figure shows the signal assignments and pin numbers for the diskette drive connectors.

Pin	Signal	Pin	Signal
1	Ground	2	Data rate select 1
3	+5 V dc	4	Drive type ID 1/Drive status 1
5	Ground	6	+12 V dc
7	Ground	8	-Index
9	Drive type ID 0/Drive status 0	10	Reserved
11	Ground	12	-Drive select
13	Ground	14	-Security Command
15	Ground	16	-Motor enable
17	Media type ID 1/Drive status 3	18	-Direction in
19	Ground	20	-Step
21	Ground	22	-Write data
23	Ground	24	-Write enable
25	Ground	26	-Track 0
27	Media type ID 0/Drive status 2	28	-Write protect
29	Ground	30	-Read data
31	Ground	32	-Head 1 select
33	Data rate select 0	34	-Diskette change

Figure 3-4. Diskette Drive Connector

System Board Memory Connectors

The Model 56 system board has three 72-pin connectors for single inline memory modules (memory modules).

The following figure shows the pin assignments for the 1- by 72-pin memory connectors. Refer to "Memory-Presence Detect Signals" on page 3-15 for decoding of the presence-detect signals.

Pin	Signal	Pin	Signal
1	Ground	37	Parity data 1
2	Data 0	38	Parity data 3
3	Data 16	39	Ground
4	Data 1	40	Column address strobe 0
5	Data 17	41	Column address strobe 2
6	Data 2	42	Column address strobe 3
7	Data 18	43	Column address strobe 1
8	Data 3	44	Row address strobe 0
9	Data 19	45	Row address strobe 1
10	+5 V dc	46	Block select 1
11	-Column address strobe parity	47	Write enable
12	Address 0	48	Reserved
13	Address 1	49	Data 8
14	Address 2	50	Data 24
15	Address 3	51	Data 9
16	Address 4	52	Data 25
17	Address 5	53	Data 10
18	Address 6	54	Data 26
19	Reserved	55	Data 11
20	Data 4	56	Data 27
21	Data 20	57	Data 12
22	Data 5	58	Data 28
23	Data 21	59	+5 V dc
24	Data 6	60	Data 29
25	Data 22	61	Data 13
26	Data 7	62	Data 30
27	Data 23	63	Data 14
28	Address 7	64	Data 31
29	Block select 0	65	Data 15
30	+5 V dc	66	Block select 2
31	Address 8	67	Presence detect 0
32	Address 9	68	Presence detect 1
33	Row address strobe 3	69	Presence detect 2
34	Row address strobe 2	70	Presence detect 3
35	Parity data 2	71	Block select 3
36	Parity data 0	72	Ground

Figure 3-5. System Board Memory Connectors

SCSI-Device Connector

The SCSI-device cable connects to the system board and provides up to two 2- by 25-pin connector for attaching internal SCSI devices. The Model 56 system board has one 2- by 30-pin connector for attaching external SCSI devices.

The following figure shows the pin assignments for the 2- by 25-pin internal SCSI connector.

Pin	Signal	Pin	Signal
1	Ground	26	+Terminal power
2	Data 0	27	Ground
3	Ground	28	Ground
4	Data 1	29	Ground
5	Ground	30	Ground
6	Data 2	31	Ground
7	Ground	32	-Attention
8	Data 3	33	Ground
9	Ground	34	Ground
10	Data 4	35	Ground
11	Ground	36	-Busy
12	Data 5	37	Ground
13	Ground	38	-Acknowledge
14	Data 6	39	Ground
15	Ground	40	-Reset
16	Data 7	41	Ground
17	Ground	42	-Message
18	Data P	43	Ground
19	Ground	44	-Select
20	Ground	45	Ground
21	Ground	46	-Control/data
22	Ground	47	Ground
23	Ground	48	-Request
24	Ground	49	Ground
25	Not connected	50	-Input/output

Figure 3-6. SCSI Device Cable Internal Connector Pin Assignments

The following figure shows the pin assignments for the 2- by 30-pin external SCSI connector.

Pin	Signal	Pin	Signal
1	Ground	31	Ground
2	Data 0	32	-Attention
3	Ground	33	Ground
4	Data 1	34	Ground
5	Ground	35	Ground
6	Data 2	36	-Busy
7	Ground	37	Ground
8	Data 3	38	-Acknowledge
9	Ground	39	Ground
10	Data 4	40	-Reset
11	Ground	41	Ground
12	Data 5	42	-Message
13	Ground	43	Ground
14	Data 6	44	-Select
15	Ground	45	Ground
16	Data 7	46	-Control/data
17	Ground	47	Ground
18	Data P	48	-Request
19	Ground	49	Ground
20	Ground	50	-Input/output
21	Ground	51	Ground
22	Ground	52	Reserved
23	Ground	53	Reserved
24	Ground	54	Reserved
25	Not connected	55	Reserved
26	+Terminal power	56	Reserved
27	Ground	57	Reserved
28	Ground	58	Reserved
29	Ground	59	Reserved
30	Ground	60	Reserved

Figure 3-7. System Board SCSI Device External Connector

Memory

The Model 56 uses the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- Real-time clock and CMOS RAM (RT/CMOS RAM)
- Nonvolatile random access memory (NVRAM)

ROM Subsystem

The ROM subsystem consists of 256KB of physical memory in two 128KB pages. Mapped ROM is active at power-on time and is assigned to the top of the first and last 1MB of address space (hex 0E0000—0FFFFF and hex FE0000—FFFFFF). After POST ensures that system memory is operating properly, the ROM code is copied to RAM at the same address space, and ROM is disabled.

Access to ROM or RAM at address space hex 0E0000—0FFFFF is controlled by the ROM enable bit in the Memory-Controller Configuration register. When ROM is enabled, it is not parity-checked, and operates with two 50-nanosecond wait states.

RAM Subsystem

The RAM subsystem on the system board starts at address hex 000000 of the address space. The RAM subsystem is 18 bits wide: 16 data bits and 2 parity bits. One parity bit is generated for each byte of data written. During a read operation, one parity bit is checked for each byte of data that is read by the device controlling the bus.

Three memory connectors are provided on the system board. Each connector can support 2MB, 4MB, or 8MB memory.

The system enables and disables memory in 1MB blocks. Each 1MB block must start on a 1MB boundary. Because 128KB of I/O ROM, 128KB of system board ROM, and 128KB of video memory are mapped within the first 1MB of address space, the first physical 1MB of RAM cannot be mapped to contiguous addresses and is split at the 640KB boundary, creating a 384KB overflow. The high 128KB of the overflow is mapped to the system board ROM address space; the remaining 256KB, called the *split memory block*, is either reserved for system use or mapped to the first available address following the last full 1MB of activated system board memory. Split-memory-block remapping and disabling are controlled by the Memory-Controller Configuration register. The presence of the split memory block in the memory address space, might be affected by nonsystem memory.

Memory Interleaving Option

The system board memory controller supports interleaving for specific memory configurations. The following figure lists the interleaving configurations for the three memory connectors for Type 1 and Type 2 system boards only. The Type 3 system board (56 486SLC2 models) does not support memory interleaving.

Memory Connector 1	Memory Connector 2	Memory Connector 3
2MB	Empty	Empty
2MB	2MB	Empty
2MB	2MB	2MB
4MB	4MB	Empty
4MB	4MB	4MB

Figure 3-8. Memory Interleaving Configurations

Memory-Presence Detect Signals

The memory-presence detect signals are used by the system to determine the size and speed of memory on the memory module. The pins are either not connected (1) or connected to ground (0).

A set of 4 bits shows the state of all memory-presence detect signals for a specific memory connector; the bit is set to 0 when the signal is connected to ground. The following figure shows the information indicated by these bits as well as the bank size of the memory module. All combinations that are not shown are reserved.

Presence Detect 3 2 1 0	Single Inline Memory Module Definition	Bank Size
1 1 0 0	2MB 70-ns memory	1MB
0 1 0 0	4MB 70-ns memory	4MB
1 0 1 1	8MB 70-ns memory	4MB

Figure 3-9. Presence-Detect Bits

System Memory Map

Memory is mapped by Memory Controller registers.

The first 640KB of system board RAM is mapped starting at address hex 000000. A 256-byte area and a 1KB area of this RAM are reserved as BIOS data areas. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for details.

The following figure shows the memory map for a properly functioning system. Memory can be mapped differently if POST detects an error in system board memory or RT/CMOS RAM. In the following figure, the variable *x* represents the number of 1MB blocks of system board memory starting at or above the hex 100000 boundary.

Hex Address Range	Function
000000 to 09FFFF†	640KB system board RAM
0A0000 to 0BFFFF	128KB video RAM
0C0000 to 0DFFFF	Feature adapter ROM
0E0000 to 0FFFFF†	128K system board ROM mapped to RAM
100000 to (100000 + xMB) − 1†	xMB system board RAM
(100000 + xMB) to (100000 + xMB + 256KB) − 1†	256KB system board RAM (split memory block)
FE0000 to FFFFFF	128KB system board ROM (same as 0E0000 to 0FFFFF)

† These address ranges are cacheable on Type 2 and Type 3 systems.

Figure 3-10. System Memory Map

Memory Controller Registers

The memory controller, which is located on the system board, has several internal registers that are used to control the memory installed in the memory connectors on the system board. The memory controller manages this memory in banks of 1MB or 4MB. Memory is enabled in 1MB increments.

Memory-parity error information is provided through the following internal registers:

- Memory-Fault Row Address Strobe (RAS) Capture register
- Two Memory-Controller Fault Address registers.

Memory-Fault RAS Capture Register (I/O Port Hex 00E2)

Bits in this register are set by a system board parity check. The RAS signal that is active at the time of the parity check is held until the system microprocessor reads this register.

Bit	Function
7, 6	Reserved
5	RAS5
4	RAS4
3	RAS3
2	RAS2
1	RAS1
0	RAS0

Figure 3-11. Memory-Fault RAS Capture Register (I/O Port Hex 00E2)

Bits 7, 6 These bits are reserved.

Bits 5–0 The system board memory connectors are wired with fixed RAS signals as follows:

Memory Connector	RAS Signals
Memory connector 1	RAS0, RAS1
Memory connector 2	RAS2, RAS3
Memory connector 3	RAS4, RAS5

Figure 3-12. Fixed RAS Signals

Memory-Controller-Fault Address Registers (I/O Ports Hex 00E4 and Hex 00E5)

These registers capture the high-order memory address when a system board parity check occurs. The address remains in the registers until the registers are read by the system microprocessor.

The following figure shows the failing memory-address space address bits for the Memory-Controller-Fault Address register (I/O Port Hex 00E4).

I/O Port Hex 00E4	Failing-Address Bit
7	15
6	14
5	13
4	12
3	11
2	10
1	09
0	08

Figure 3-13. Memory-Controller-Fault Address Register (I/O Port Hex 00E4)

The following figure shows the failing memory-address space address bits for the Memory-Controller-Fault Address register (I/O Port Hex 00E5).

I/O Port Hex 00E5	Failing-Address Bit
7	23
6	22
5	21
4	20
3	19
2	18
1	17
0	16

Figure 3-14. Memory-Controller-Fault Address Registers (I/O Port Hex 00E5)

RT/CMOS RAM

The RT/CMOS RAM (real-time clock/complementary metal-oxide semiconductor RAM) module contains the real-time clock and 64 bytes of CMOS RAM. The clock uses 14 bytes of this memory, and the rest is allocated to configuration and system status information. A battery, which is located on the bus adapter, keeps the RT/CMOS RAM active when the power supply is off.

The system board has an additional 8KB CMOS RAM extension that is used to store configuration and other system information. This RAM extension is kept active by the battery on the bus adapter.

The following figure shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000–00D	Real-Time Clock bytes
00E	Diagnostic Status byte
00F	Shutdown Status byte
010	Diskette Drive Type byte
011	Fixed Disk Drive Type byte
012	Reserved
013	Reserved
014	Equipment byte
015, 016	Low and High Base-Memory bytes
017, 018	Low and High Expansion-Memory bytes
019–031	Reserved
032, 033	Configuration CRC bytes
034	Reserved
035, 036	Low and high usable memory above 1MB
037	Date-Century byte
038–03F	Reserved

Figure 3-15. RT/CMOS RAM Address Map

RT/CMOS Address and NMI Mask Register (Hex 0070)

This register is used with the RT/CMOS Data register (hex 0071) to read from and write to the RT/CMOS RAM bytes.

Warning: The operation following a write operation to this register should access the RT/CMOS Data register; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Bit	Function
7	NMI mask
6	Reserved
5–0	RT/CMOS RAM address

Figure 3-16. RT/CMOS Address and NMI Mask Register (Hex 0070)

Bit 7 When this write-only bit is set to 1, the NMI is masked (disabled). This bit is set to 1 by a power-on reset.

Bit 6 This bit is reserved.

Bits 5–0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This register is used with the RT/CMOS Address and NMI Mask register to read from and write to the RT/CMOS RAM bytes.

Bit	Function
7–0	RT/CMOS data

Figure 3-17. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts must be masked to prevent other interrupt routines from changing the CMOS Address register before data is read from or written to.

Warning: The operation following a write operation to hex 0070 must access hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Writing to RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Write the data to address hex 0071.
3. Write the address, hex 0F, to the RT/CMOS and NMI Mask register; this leaves hex 0070 pointing to the Shutdown Status byte (hex 0F).
4. Read address hex 0071 to restore the RT/CMOS (see the warning above).

Reading from RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Read the data from address hex 0071.
3. Write the address, hex 0F, to the RT/CMOS and NMI Mask register; this leaves hex 0070 pointing to the Shutdown Status byte (hex 0F).
4. Read address hex 0071 to restore the RT/CMOS.

Real-Time Clock Bytes (Hex 000 – 00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following figure.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second alarm	1
002	Minutes	2
003	Minute alarm	3
004	Hours	4
005	Hour alarm	5
006	Day of week	6
007	Date of month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-18. Real-Time Clock Bytes (Hex 000 – 00D)

Note: The system initializes Status Registers A and B when the time and date are set. Interrupt 1AH is the BIOS interface to read and set the time and date, and it initializes the registers in the same way as the system does.

Status Register A (Hex 00A)

Bit	Function
7	Update in progress
6 – 4	22-stage divider
3 – 0	Rate-selection bits

Figure 3-19. Status Register A (Hex 00A)

Bit 7 When this bit is set to 1, this bit indicates that the time-update cycle is in progress. When this bit is set to 0, it indicates that the current date and time can be read.

Bits 6 – 4 These bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768-kHz time base. This is the only value supported by the system for proper timekeeping.

Bits 3–0 These bits allow the selection of a divider-output frequency. The system initializes the rate-selection bits to binary 0110, which selects a 1.024-kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Enable periodic-interrupt
5	Enable alarm-interrupt
4	Enable update-ended interrupt
3	Enable square wave
2	Date mode
1	24-hour mode
0	Enable daylight saving time mode

Figure 3-20. Status Register B (Hex 00B)

Bit 7 When this bit is set to 0, it updates the cycle by advancing the counts at a rate of one per second. When this bit is set to 1, it immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This bit is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status register A. When this bit is set to 1, it enables the interrupt. The system initializes this bit to 0.

Bit 5 When this bit is set to 1, it enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When this bit is set to 1, it enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When this bit is set to 1, it enables the square-wave frequency as set by the rate-selection bits in Status register A. The system initializes this bit to 0.

Bit 2 This bit indicates whether the binary-coded-decimal (BCD) or binary format is used for time-and-date calendar updates. When this bit is set to 1, it indicates the binary format. The system initializes this bit to 0.

Bit 1 This bit indicates if the hours byte is in 12-hour or 24-hour mode. When this bit is set to 1, it indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When this bit is set to 1, it enables the daylight-saving-time mode. When this bit is set to 0, it disables the modes and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt-request flag
6	Periodic-interrupt flag
5	Alarm-interrupt flag
4	Update-ended interrupt flag
3–0	Reserved

Figure 3-21. Status Register C (Hex 00C)

Note: Interrupts are enabled by bits 6, 5, and 4 in Status register B.

Bit 7 When this bit is set to 1, it indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When this bit is set to 1, it indicates that a periodic interrupt occurred.

Bit 5 When this bit is set to 1, it indicates that an alarm interrupt occurred.

Bit 4 When this bit is set to 1, it indicates that an update-ended interrupt occurred.

Bits 3–0 These bits are reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6–0	Reserved

Figure 3-22. Status Register D (Hex 00D)

Bit 7 This read-only bit monitors the internal battery. When this bit is set to 1, it indicates that the real-time clock has power. When this bit is set to 0, it indicates that the real-time clock has lost power.

Bits 6–0 These bits are reserved.

CMOS RAM Configuration

The following shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-time clock power
6	Configuration record and checksum status
5	Incorrect configuration
4	Memory-size mismatch
3	Fixed disk controller/drive C initialization status
2	Time status indicator
1	Adapter configuration miscompare
0	Adapter ID time-out

Figure 3-23. Diagnostic Status Byte (Hex 00E)

Bit 7 When this bit is set to 1, it indicates that the real-time clock lost power.

Bit 6 When this bit is set to 1, it indicates that a checksum is incorrect.

Bit 5 When this bit is set to 1, it indicates that the configuration information is incorrect.

Bit 4 When this bit is set to 1, it indicates that the memory size does not match the configuration information.

Bit 3 When this bit is set to 1, it indicates that the controller or fixed disk drive failed initialization.

Bit 2 When this bit is set to 1, it indicates that the time and date are invalid.

Bit 1 When this bit is set to 1, it indicates that the adapters do not match the configuration information.

Bit 0 When this bit is set to 1, it indicates that a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is used by POST and BIOS.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7–4	First diskette drive type
3–0	Second diskette drive type

Figure 3-24. Diskette Drive Type Byte (Hex 010)

Bits 7–4 These bits indicate the first diskette drive type, as shown in the following figure.

Bits 7 6 5 4	Function
0 0 0 0	No drive present
0 0 0 1	5.25-inch, 360KB diskette drive
0 0 1 0	5.25-inch, 1.2MB diskette drive
0 0 1 1	3.5-inch, 720KB diskette drive
0 1 0 0	3.5-inch, 1.44MB diskette drive
0 1 1 0	3.5-inch, 2.88MB diskette drive

Note: All combinations that are not shown are reserved.

Figure 3-25. Diskette Drive Type Byte (Bits 7–4)

Bits 3–0 These bits indicate the second diskette drive type, as shown in the following figure.

Bits 3 2 1 0	Function
0 0 0 0	No drive present
0 0 0 1	5.25-inch, 360KB diskette drive
0 0 1 0	5.25-inch, 1.2MB diskette drive
0 0 1 1	3.5-inch, 720KB diskette drive
0 1 0 0	3.5-inch, 1.44MB diskette drive
0 1 1 0	3.5-inch, 2.88MB diskette drive

Note: All combinations that are not shown are reserved.

Figure 3-26. Diskette Drive Type Byte (Bits 3–0)

Fixed Disk Drive Type Byte (Hex 011): This byte defines the type of fixed disk drive installed. Hex 000 indicates that a fixed disk drive is *not* installed. This byte is not used for SCSI fixed disk drives.

Note: For more information about fixed disk drives, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Reserved Bytes (Hex 012, 013): These bytes are reserved.

Equipment Byte (Hex 014): This byte defines the basic equipment in the system for the power-on diagnostic tests.

Bit	Function
7, 6	Number of diskette drives other than physical drive 0
5, 4	Display operating mode
3, 2	Reserved
1	Math coprocessor presence
0	Diskette drive 0 presence

Figure 3-27. Equipment Byte (Hex 014)

Bits 7, 6 These bits indicate the number of diskette drives other than drive 0 installed, as shown in the following figure.

Bits 7 6	Number of Diskette Drives
0 0	No other drive
0 1	One other drive
1 0	Two other drives
1 1	Reserved

Figure 3-28. Installed Diskette Drive Bits

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port, as shown in the following figure.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-column mode
1 0	80-column mode
1 1	Monochrome mode

Figure 3-29. Display Operating-Mode Bits

Bits 3, 2 These bits are reserved.

Bit 1 When this bit is set to 1, it indicates that a math coprocessor is installed.

Bit 0 When this bit is set to 1, it indicates that physical diskette drive 0 is installed.

Low and High Base-Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The hexadecimal value in these bytes represents the number of 1KB blocks of *base memory*. For example, hex 0280 indicates 640KB. The low byte is hex 015; the high byte is hex 016.

Low and High Expansion-Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The hexadecimal value in these bytes represent the number of 1KB blocks of *expansion memory*. For example, hex 0800 indicates 2048KB. The low byte is hex 017; the high byte is hex 018.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check (CRC) data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 033; the high byte is hex 032.

Reserved Byte (Hex 034): This byte is reserved.

Low and High Usable Memory Bytes (Hex 035 and 036): These bytes define the total amount of contiguous memory from 1MB to 16MB.

The hexadecimal value in these bytes represent the number of 1KB blocks of usable memory. For example, hex 0800 indicates 2408KB. The low byte is hex 035; the high byte is hex 036.

Date Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 – 03F): These bytes are reserved.

NVRAM

The NVRAM contains, among other things, the system configuration information. The entire RAM is reserved for system use.

| Vital Product Data

| On 56 models with a Type 3 system board (486SLC2 models), the
| system board has a unique vital product data (VPD) code. This code
| is stored in NVRAM and contains various system identification
| information. Interrupt 15H, function code (AH)=D2H, returns the
| system identification information. See the *IBM Personal System/2*
| *and Personal Computer BIOS Interface Technical Reference* for more
| information.

Miscellaneous System Functions and Ports

| Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system watchdog time-out has occurred. The NMI (except cache parity error) stops all arbitration on the bus until bit 6 of the
| Arbitration register (I/O address hex 0090) is set to 0. (On the 56
| 486SLC2 models, only the channel time-out NMI stops arbitration on
| the bus.) This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts, and the IRET instruction restores the interrupt flag to the state it was in before the interrupt. A system reset causes a reset of the NMI.

The NMI requests from system board parity and channel check are subject to mask control with the NMI mask bit in the RT/CMOS Address register. The watchdog timer, system channel time-out, and cache parity error are not masked by this bit. See "RT/CMOS Address and NMI Mask Register (Hex 0070)" on page 3-19. The power-on default of the NMI mask is 1 (NMI disabled). Before the NMI is enabled after a power-on reset, the parity-check and channel-check states are initialized by POST.

Warning: The operation following a write operation to this register must access the RT/CMOS Data register; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the write and read functions of this port are shown in the following figures.

Bit	Function
7	Reset timer 0 output latch (IRQ0)
6–4	Reserved
3	Enable channel check
2	Enable parity check
1	Enable speaker data
0	Timer 2 gate to speaker

Figure 3-30. System Control Port B (Hex 0061)—Write

Bit	Function
7	Parity check
6	Channel check
5	Timer 2 output
4	Toggles with each refresh request
3	Enable channel check
2	Enable parity check
1	Enable speaker data
0	Timer 2 gate to speaker

Figure 3-31. System Control Port B (Hex 0061)—Read

Bit 7 When this bit is set to 1 during a write operation, IRQ0 is reset. When read as a 1, this bit indicates that a parity check has occurred.

Bit 6 When read as a 1, this bit indicates that a channel check has occurred.

Bit 5 When read, this bit indicates the condition of the timer/counter 2 'output' signal.

Bit 4 When read, this bit toggles for each refresh request.

Bit 3 When this bit is set to 0, it enables a channel check. This bit is set to 1 during a power-on reset.

Bit 2 When this bit is set to 0, it enables a parity check. This bit is set to 1 during a power-on reset.

Bit 1 When this bit is set to 1, it enables speaker data.

Bit 0 When this bit is set to 1, it enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7–5	Reserved
4	Watchdog timer status
3	Security lock latch
2	Reserved
1	Alternate gate A20
0	Alternate hot reset

Figure 3-32. System Control Port A (Hex 0092)

Bits 7–5 These bits are reserved.

Bit 4 This read-only bit indicates the watchdog-timer status. When this bit is set to 1, a watchdog time-out has occurred. For more information about the watchdog timer, refer to the System Timers section of the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces*.

Bit 3 This bit provides the security lock for the secured area of RT/CMOS. When this bit is set to 1, the 8-byte, power-on password is electronically locked. After this bit is set by POST, it can be cleared only by turning the system off.

Bit 2 This bit is reserved.

Bit 1 This bit is ORed with bit 1 in the Keyboard Output port to enable the 'address 20' signal (A20). When both bits are set to 0, A20 is disabled and set to 0. This bit is set to 0 during POST. See the Keyboard and Auxiliary Device Controller section of the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces*.

Bit 0 This bit provides an alternative method of resetting the system microprocessor. This alternative method supports operating systems that require faster operation than was provided on the IBM Personal Computer AT*. Resetting the system microprocessor switches the microprocessor from protected mode to real-address mode. The alternative reset takes 13.4 microseconds.

This bit is set to 0 by either a system reset or a write operation. When a write operation changes this bit from 0

* Trademark of the IBM Corporation.

to 1, the alternative reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is set to 0, POST assumes that the system was just powered-on. If the bit is set to 1, POST assumes that a switch from the protected mode to the real mode has taken place.

When bit 0 is used to reset the system microprocessor to the real mode, the following procedure *must* be used:

1. Disable all maskable and nonmaskable interrupts.
2. Reset the system microprocessor by writing a 1 to bit 0.
3. Issue a Halt instruction to the system microprocessor.
4. Reenable all maskable and nonmaskable interrupts.

If this procedure is not followed, the results will be unpredictable.

Note: Whenever possible, BIOS or ABIOS should be used as an interface to reset the system microprocessor to the real mode. See *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for more information about BIOS.

Power-On Password

RT/CMOS RAM has 8 bytes reserved for the power-on password and its check character. The 8 bytes are initialized to hex 00. The microprocessor can access these bytes only during power-on self-test (POST). After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by a program. During power-on password installation, the password (1 to 7 characters), is stored in the security space.

Installing the password is a function of a program on the Reference Diskette. The power-on password does not appear on the screen when it is installed, changed, or removed. After the power-on password has been installed, it can be changed or removed only during POST.

Privileged-Access Password

The privileged-access password (on 56 486SLC2 models only) is also a function of the Reference Diskette. This password, when set and entered correctly, will give the owner access to the entire system, overriding the power-on password. It is stored in electrically-erasable programmable read-only memory (EEPROM), and is only accessible by the processor during power-on self-test (POST) and during system configuration. Afterwards, the locations are locked from further access.

Warning: If the owner forgets the privileged-access password after it has been set, the system board must be replaced to make the system operational.

Keyboard Password

The Model 56 also can have a keyboard password. See the Keyboard and Auxiliary Device Controller section of the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* for more information.

Cover Lock and Tamper-Evident Switch

All 56 486SLC2 models have an electro-mechanical cover lock. In the locked position, it mechanically prevents the cover from being removed. If the covers are forced open, the tamper-evident cover switch detects the intrusion. The next time the system is powered-on, POST displays a message informing the user that the system covers have been tampered with.

Note: When the cover is removed, power is removed from the system. If you want to run the system with the cover off, you must move the security switch to the "up" or "on" position.

Selectable Boot Sequence

The selectable boot sequence allows the user to specify the order in which 1 to 4 bootable devices are searched when looking for the boot startup record of an operating system. Diskette drives, fixed disk drives, and remote initial program load (RIPL) can be part of the search sequence. Changing the sequence for selectable boot affects the drive-letter assignment each time the system is reset, either as a power-on reset or a soft reset.

The user selects the boot sequence by using the Select startup sequence menu on the System Reference Diskette, and selecting from a list of possible devices. After the sequence is selected, it is stored in nonvolatile RAM (NVRAM). On the 56 486SLC2, the boot sequence is stored in electrically-erasable programmable read-only memory (EEPROM). When the system is booted, it searches for a device that contains a bootable record, using the specified sequence.

After the operating system is booted, the drive lettering is determined by the sequence and by which device contained the bootable source.

Note: Selectable boot affects adapters that use initialization programs. See the Setup section of *IBM Personal System/2 Hardware Interface Technical Reference—Architectures* for more details.

Hardware Compatibility

The Model 56 maintains many of the interfaces used by previous PS/2 products. In most cases, command and status organization of these interfaces is maintained.

The functional interfaces for the Model 56 are compatible with the following:

- The Intel 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller-address/transfer counters, page registers and status fields only. The Command and Request registers are not supported. The Rotate and Mask functions are not supported. The Mode register is partially supported.
- The NS16450 serial port.
- The Intel 8088, 8086, 80286, and 80386 microprocessors.
- The Intel 8272 diskette drive controller.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The keyboard interface at address hex 0060.

** Trademark of Motorola, Incorporated.

- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in DOS mode.
- Generally compatible with the Intel 80387, 80287, and 8087 math coprocessors.

Error Codes

POST returns a message in the form of a multiple-character code to indicate the type of test that failed. Two formats are used for these error messages:

- A 12-character code for all errors *that are* related to SCSI devices:
  - The first four characters identify the device type.
  - The next eight characters identify specifics of the error.
- An 8-character error code for all errors *that are not* related to SCSI devices.

The 8-character error code consists of two 4-character elements; the major error code and the minor error code. The following figure lists the failure and the associated error code.

Major Code	Minor Code	Description
0001		System bus error - system board
	0100	Unexpected interrupt
	0200	Timer failure
	0300	Timer interrupt failure
	0400	Protected mode failure
	0500	Last keyboard command not accepted
	0600	Converting logic test
	0700	NMI test failed
	0800	Timer bus-test failed
	0900	Low MB chip select test failed
	10*xx*	System board memory parity error
	11*xx*	I/O channel-check error
	1200	Watchdog time-out
	1300	DMA arbitration time-out
	1400	Channel feature card ROM checksum error
	1500	ROM checksum error or DMA error
	1600	System board port read/write failure
	1800	System board parity
	2000	Microprocessor test error
	6000	System board ID not recognized
	6100	Dead battery
	6300	Clock not updating
	6400	Memory-configuration error
	6500	Adapter ID mismatch
	6600	Adapter-busy error
	6700	Clock not updating
	6900	System board and processor card configuration mismatch
	7100	Rolling-bit-test failure on CMOS shutdown address byte
	7200	Rolling-bit-test failure on NVRAM diagnostic byte
	7300	Bad CMOS/NVRAM checksum
	7400	Bad configuration
	7500	Bad EEPROM
	7600	Tamper evident
	7700	Bad EEPROM
	7800	Bad EEPROM
	7900	NVRAM error log full
	8100	Unsupported configurations
	8200	Privileged-access switch (JMP2) is not in the write-enable position
	8300	Privileged-access password required
	8400	Bad power-on password
	8500	Bad startup sequence
	8600	Password protection hardware error
	8700	Serial number error
	8800	Bad EEPROM checksum
	8900	Excessive incorrect password attempts

Figure 3-33 (Part 1 of 2). POST Error Messages

Major Code	Minor Code	Description
0002		Memory errors
	0xxx	Memory error
	1xxx	Unrecoverable error in first 1MB
	2100	ROM-to-RAM remapping error
	25xx	Unsupported memory-type installed
0003		Keyboard
	0100	Keyboard error
	0200	Keyboard locked
	0300	Keyboard-to-system board interface error
	0400	Keyboard clock high
	0500	No keyboard +5 V dc
0006		Diskette
	0100	Diskette drive or controller error
	0200	Diskette IPL boot record not valid
	0400	Non-media sense
	0500	Diskette drive locked
0011	0100	Serial port A error
0012	0100	Serial port B error
0017		Fixed disk error
	8000	Fixed disk 0 failed
	8100	Fixed disk 1 failed
	8200	Disk-controller error
	9000	Fixed disk 0 error
	9100	Fixed disk 1 error
0024	0100	System board video error
0037	xxxx	System board SCSI controller error
0086		Mouse
	0100	System-bus error - keyboard/pointing device interface
	0200	Pointing-device error
	0300	Pointing-device or system-bus error
0096	xxxx	SCSI adapter with cache error
0112	xxxx	SCSI adapter error
0129	0200	Cache error
0208 to 0241	xxxx	SCSI device test failure
1999		Special instruction codes
	00xx	Initial microcode load (IML) error
	03xx	No bootable device
	04xx	IML-to-system mismatch

Figure 3-33 (Part 2 of 2). POST Error Messages

Appendix. 386SLC Instruction Cycle Times

The following are the instruction timings for the IBM 386SLC. All cache-off timings are considered cache-miss situations. Any instructions not listed are the same as for the Intel 80386SX.

Mnemonic	16-Bit Real Mode Cache-Miss Cycles Base Rep	16-Bit Real Mode Cache-Hit Cycles Base Rep	16-Bit Protected Mode Cache-Miss Cycles Base Rep	16-Bit Protected Mode Cache-Hit Cycles Base Rep
adc mb,ib	7	5	7	5
adc mb,rb	7	5	7	5
adc mw,iw	7	5	7	5
adc mw,rw	7	5	7	5
adc rb,ib	2	2	2	2
adc rb,mb	6	4	6	4
adc rb,rb	2	2	2	2
adc rw,iw	2	2	2	2
adc rw,mw	6	4	6	4
adc rw,rw	2	2	2	2
add mb,ib	7	5	7	5
add mb,rb	7	5	7	5
add mw,iw	7	5	7	5
add mw,rw	7	5	7	5
add rb,ib	2	2	2	2
add rb,mb	5	3	5	3
add rb,rb	2	2	2	2
add rw,iw	2	2	2	2
add rw,mw	5	3	5	3
add rw,rw	2	2	2	2
and mb,ib	7	5	7	5
and mb,rb	7	5	7	5
and mw,iw	7	5	7	5
and mw,rw	7	5	7	5
and rb,ib	2	2	2	2
and rb,mb	5	3	5	3
and rb,rb	2	2	2	2
and rw,iw	2	2	2	2
and rw,mw	5	3	5	3
and rw,rw	2	2	2	2
bound rdw,mqw	15	10	15	10
bound rw,mdw	11	10	11	10
bsf rdw,mdw	40	37	40	37
bsf rdw,rdw	35	35	35	35
bsf rw,mw	26	25	26	25
bsf rw,rw	23	23	23	23

Figure A-1 (Part 1 of 8). Instruction Cycle Times

© Copyright IBM Corp. 1991, 1992

Mnemonic	16-Bit Real Mode Cache-Miss Cycles Base	16-Bit Real Mode Cache-Miss Cycles Rep	16-Bit Real Mode Cache-Hit Cycles Base	16-Bit Real Mode Cache-Hit Cycles Rep	16-Bit Protected Mode Cache-Miss Cycles Base	16-Bit Protected Mode Cache-Miss Cycles Rep	16-Bit Protected Mode Cache-Hit Cycles Base	16-Bit Protected Mode Cache-Hit Cycles Rep
bsr rdw,mdw	38		35		38		35	
bsr rdw,rdw	33		33		33		33	
bsr rw,mw	24		23		24		23	
bsr rw,rw	21		21		21		21	
bt mdw,ib	8		5		8		5	
bt mdw,rdw	14		11		14		11	
bt mw,ib	6		5		6		5	
bt mw,rw	12		11		12		11	
bt rdw,ib	3		3		3		3	
bt rdw,rdw	3		3		3		3	
bt rw,ib	3		3		3		3	
bt rw,rw	3		3		3		3	
btc mdw,ib	9		8		9		8	
btc mdw,rdw	15		13		15		13	
btc mw,ib	8		8		8		8	
btc mw,rw	13		13		13		13	
btc rdw,ib	6		6		6		6	
btc rdw,rdw	6		6		6		6	
btc rw,ib	6		6		6		6	
btc rw,rw	6		6		6		6	
btr mdw,ib	9		8		9		8	
btr mdw,rdw	15		13		15		13	
btr mw,ib	8		8		8		8	
btr mw,rw	13		13		13		13	
btr rdw,ib	6		6		6		6	
btr rdw,rdw	6		6		6		6	
btr rw,ib	6		6		6		6	
btr rw,rw	6		6		6		6	
bts mdw,ib	9		8		9		8	
bts mdw,rdw	15		13		15		13	
bts mw,ib	8		8		8		8	
bts mw,rw	13		13		13		13	
bts rdw,ib	6		6		6		6	
bts rdw,rdw	6		6		6		6	
bts rw,ib	6		6		6		6	
bts rw,rw	6		6		6		6	
call cs:ip	20		14		32		19	
call disp	9		5		9		5	
call far m	27		17		39		22	
call m	14		10		14		10	
call rw	11		7		11		7	
cli	5		5		5		5	
cmc	2		2		2		2	

Figure A-1 (Part 2 of 8). Instruction Cycle Times

Mnemonic	16-Bit Real Mode Cache-Miss Cycles Base Rep	16-Bit Real Mode Cache-Hit Cycles Base Rep	16-Bit Protected Mode Cache-Miss Cycles Base Rep	16-Bit Protected Mode Cache-Hit Cycles Base Rep
cmp mb,ib	5	3	5	3
cmp mb,rb	5	3	5	3
cmp mw,iw	5	3	5	3
cmp mw,rw	5	3	5	3
cmp rb,ib	2	2	2	2
cmp rb,mb	6	4	6	4
cmp rb,rb	2	2	2	2
cmp rw,iw	2	2	2	2
cmp rw,mw	6	4	6	4
cmp rw,rw	2	2	2	2
cmpsb	12	10	12	10
cmpsw	12	10	12	10
cmpsd	16	10	16	10
dec mb	6	4	6	4
dec mw	6	4	6	4
dec rb	2	2	2	2
dec rw	2	2	2	2
enter	7	7	7	7
imul mb	6	4	6	4
imul mw	6	4	6	4
imul rb	2	2	2	2
imul rw	2	2	2	2
imul rw,rw,iw	19	19	19	19
in rb,dx	14	14	7	7
in rb,ib	12	12	6	6
in rw,dx	14	14	7	7
in rw,ib	12	12	6	6
inc mb	6	4	6	4
inc mw	6	4	6	4
inc rb	2	2	2	2
inc rw	2	2	2	2
int ib	43	35	76	64
iret	31	26	42	30
jcond not taken	3	3	3	3
jcond taken	9	5	9	5
jcxz not taken	3	3	3	3
jcxz taken	9	5	9	5
jmp cs:ip	16	12	27	16
jmp disp	9	5	9	5
jmp far m	23	15	34	19
jmp m	13	8	13	8
jmp rw	10	6	10	6
lds rw,mw	7	6	23	12

Figure A-1 (Part 3 of 8). Instruction Cycle Times

Mnemonic	16-Bit Real Mode Cache-Miss Cycles Base Rep	16-Bit Real Mode Cache-Hit Cycles Base Rep	16-Bit Protected Mode Cache-Miss Cycles Base Rep	16-Bit Protected Mode Cache-Hit Cycles Base Rep
leave	5	4	5	4
les rw,mw	7	6	23	12
lodsb	5	5	5	5
lodsd	7	5	7	5
lodsw	5	5	5	5
loop not taken	11	9	11	9
loop taken	9	5	9	5
loopc not taken	14	12	14	12
loopc taken	12	8	12	8
mov m,s	2	2	2	2
mov mb,ib	2	2	2	2
mov mb,rb	2	2	2	2
mov mw,iw	2	2	2	2
mov mw,rw	2	2	2	2
mov rb,ib	2	2	2	2
mov rb,mb	4	2	4	2
mov rb,rb	2	2	2	2
mov rw,iw	2	2	2	2
mov rw,mw	4	2	4	2
mov rw,rw	2	2	2	2
mov rw,s	2	2	2	2
mov s,m	5	4	18	9
mov s,rw	2	2	15	8
movsb	9	8	9	8
movsd	11	8	11	8
movsw	9	8	9	8
movsx rdw,mb	6	5	6	5
movsx rdw,mw	6	5	6	5
movsx rw,mb	6	5	6	5
movzx rdw,mb	6	5	6	5
movzx rdw,mw	6	5	6	5
movzx rw,mb	6	5	6	5
mul mb	16	15	16	15
mul mw	16	15	16	15
mul rb	13	13	13	13
mul rw	13	13	13	13
neg mb	6	4	6	4
neg mw	6	4	6	4
neg rb	2	2	2	2
neg rw	2	2	2	2
not mb	6	4	6	4
not mw	6	4	6	4
not rb	2	2	2	2
not rw	2	2	2	2

Figure A-1 (Part 4 of 8). Instruction Cycle Times

Mnemonic	16-Bit Real Mode Cache-Miss Cycles Base Rep	16-Bit Real Mode Cache-Hit Cycles Base Rep	16-Bit Protected Mode Cache-Miss Cycles Base Rep	16-Bit Protected Mode Cache-Hit Cycles Base Rep
or mb,ib	7	5	7	5
or mb,rb	7	5	7	5
or mw,iw	7	5	7	5
or mw,rw	7	5	7	5
or rb,ib	2	2	2	2
or rb,mb	5	3	5	3
or rb,rb	2	2	2	2
or rw,iw	2	2	2	2
or rw,mw	5	3	5	3
or rw,rw	2	2	2	2
out dx,rb	12	12	6	6
out dx,rw	12	12	6	6
out ib,rb	11	11	5	5
out	11	11	5	5
pop m	6	5	6	5
pop rw	4	2	4	2
pop s	5	4	18	9
popa	25	24	25	24
popad	33	24	66	65
popf	8	7	6	5
push m	6	5	6	5
push rw	2	2	2	2
push s	2	2	2	2
push iw	2	2	2	2
pusha	24	24	24	24
pushad	32	25	66	66
pushf	7	7	5	5
rep:cmpsb	10+4*n*†	9+2*n*	10+4*n*	9+2*n*
rep:cmpsw	10+4*n*	9+2*n*	10+4*n*	9+2*n*
rep:cmpsd	10+8*n*	9+2*n*	10+8*n*	9+2*n*
rep:lodsb	5+6*n*	5+6*n*	5+6*n*	5+6*n*
rep:lodsd	5+8*n*	5+6*n*	5+8*n*	5+6*n*
rep:lodsw	5+6*n*	5+6*n*	5+6*n*	5+6*n*
rep:movsb	8+5*n*	8+2*n*	8+5*n*	8+2*n*
rep:movsw	8+5*n*	8+2*n*	8+5*n*	8+2*n*
rep:movsd	8+8*n*	8+2*n*	8+8*n*	8+2*n*
rep:scasb	8+4*n*	8+2*n*	8+4*n*	8+2*n*
rep:scasw	8+4*n*	8+2*n*	8+4*n*	8+2*n*
rep:scasd	8+6*n*	8+2*n*	8+6*n*	8+2*n*

† *n* represents the number of additional cycles.

Figure A-1 (Part 5 of 8). Instruction Cycle Times

Mnemonic	16-Bit Real Mode Cache-Miss Cycles Base Rep	16-Bit Real Mode Cache-Hit Cycles Base Rep	16-Bit Protected Mode Cache-Miss Cycles Base Rep	16-Bit Protected Mode Cache-Hit Cycles Base Rep
rep:stosb	5+2*n*	5+2*n*	5+2*n*	5+2*n*
rep:stosw	5+2*n*	5+2*n*	5+2*n*	5+2*n*
rep:stosd	5+4*n*	5+2*n*	5+4*n*	5+2*n*
ret	11	7	11	7
ret iw	11	7	11	7
retf	21	13	33	19
retf iw	21	13	33	19
rol mb,cl	7	6	7	6
rol mb,ib	7	6	7	6
rol mw,cl	7	6	7	6
rol mw,ib	7	6	7	6
rol rb,cl	3	3	3	3
rol rb,ib	3	3	3	3
rol rw,cl	3	3	3	3
rol rw,ib	3	3	3	3
ror mb,cl	7	6	7	6
ror mb,ib	7	6	7	6
ror mw,cl	7	6	7	6
ror mw,ib	7	6	7	6
ror rb,cl	3	3	3	3
ror rb,ib	3	3	3	3
ror rw,cl	3	3	3	3
ror rw,ib	3	3	3	3
sahf	3	3	3	3
sal mb,cl	7	6	7	6
sal mb,ib	7	6	7	6
sal mw,cl	7	6	7	6
sal mw,ib	7	6	7	6
sal rb,cl	3	3	3	3
sal rb,ib	3	3	3	3
sal rw,cl	3	3	3	3
sal rw,ib	3	3	3	3
sar mb,cl	7	6	7	6
sar mb,ib	7	6	7	6
sar mw,cl	7	6	7	6
sar mw,ib	7	6	7	6
sar rb,cl	3	3	3	3
sar rb,ib	3	3	3	3
sar rw,cl	3	3	3	3
sar rw,ib	3	3	3	3

Figure A-1 (Part 6 of 8). Instruction Cycle Times

Mnemonic	16-Bit Real Mode Cache-Miss Cycles Base Rep	16-Bit Real Mode Cache-Hit Cycles Base Rep	16-Bit Protected Mode Cache-Miss Cycles Base Rep	16-Bit Protected Mode Cache-Hit Cycles Base Rep
sbb mb,ib	7	5	7	5
sbb mb,rb	7	5	7	5
sbb mw,iw	7	5	7	5
sbb mw,rw	7	5	7	5
sbb rb,ib	2	2	2	2
sbb rb,mb	6	4	6	4
sbb rb,rb	2	2	2	2
sbb rw,iw	2	2	2	2
sbb rw,mw	6	4	6	4
sbb rw,rw	2	2	2	2
scasb	8	7	8	7
scasd	10	7	10	7
scasw	8	7	8	7
shl mb,cl	7	6	7	6
shl mb,ib	7	6	7	6
shl mw,cl	7	6	7	6
shl mw,ib	7	6	7	6
shl rb,cl	3	3	3	3
shl rb,ib	3	3	3	3
shl rw,cl	3	3	3	3
shl rw,ib	3	3	3	3
shld mw,rw,cl	7	6	7	6
shld mw,rw,ib	7	6	7	6
shld rw,rw,cl	3	3	3	3
shld rw,rw,ib	3	3	3	3
shld mdw,rdw,cl	9	6	9	6
shld mdw,rdw,ib	9	6	9	6
shld rdw,rdw,cl	3	3	3	3
shld rdw,rdw,ib	3	3	3	3
shr mb,cl	7	6	7	6
shr mb,ib	7	6	7	6
shr mw,cl	7	6	7	6
shr mw,ib	7	6	7	6
shr rb,cl	3	3	3	3
shr rb,ib	3	3	3	3
shr rw,cl	3	3	3	3
shr rw,ib	3	3	3	3
shrd mw,rw,cl	7	6	7	6
shrd mw,rw,ib	7	6	7	6
shrd rw,rw,cl	3	3	3	3
shrd rw,rw,ib	3	3	3	3
shrd mdw,rdw,cl	9	6	9	6
shrd mdw,rdw,ib	9	6	9	6
shrd rdw,rdw,cl	3	3	3	3
shrd rdw,rdw,ib	3	3	3	3
stc	2	2	2	2

Figure A-1 (Part 7 of 8). Instruction Cycle Times

Mnemonic	16-Bit Real Mode Cache-Miss Cycles Base	16-Bit Real Mode Cache-Miss Cycles Rep	16-Bit Real Mode Cache-Hit Cycles Base	16-Bit Real Mode Cache-Hit Cycles Rep	16-Bit Protected Mode Cache-Miss Cycles Base	16-Bit Protected Mode Cache-Miss Cycles Rep	16-Bit Protected Mode Cache-Hit Cycles Base	16-Bit Protected Mode Cache-Hit Cycles Rep
std	2		2		2		2	
sti	5		5		5		5	
stosb	5		5		5		5	
stosd	5		5		5		5	
stosw	5		5		5		5	
sub mb,ib	7		5		7		5	
sub mb,rb	7		5		7		5	
sub mw,iw	7		5		7		5	
sub mw,rw	7		5		7		5	
sub rb,ib	2		2		2		2	
sub rb,mb	6		4		6		4	
sub rb,rb	2		2		2		2	
sub rw,iw	2		2		2		2	
sub rw,mw	6		4		6		4	
sub rw,rw	2		2		2		2	
test mb,ib	5		3		5		3	
test mw,iw	5		3		5		3	
test rb,ib	2		2		2		2	
test rb,mb	5		3		5		3	
test rb,rb	2		2		2		2	
test rw,iw	2		2		2		2	
test rw,mw	5		3		5		3	
test rw,rw	2		2		2		2	
xlat	5		4		5		4	
xor mb,ib	7		5		7		5	
xor mb,rb	7		5		7		5	
xor mw,iw	7		5		7		5	
xor mw,rw	7		5		7		5	
xor rb,ib	2		2		2		2	
xor rb,mb	5		3		5		3	
xor rb,rb	2		2		2		2	
xor rw,iw	2		2		2		2	
xor rw,mw	5		3		5		3	
xor rw,rw	2		2		2		2	

Figure A-1 (Part 8 of 8). Instruction Cycle Times

Index

Numerics

386SLC microprocessor 1-11, 3-3
486SLC2 microprocessor 1-12, 3-4
80386SX microprocessor 1-11, 3-3
80387SX math coprocessor 3-6

A

adapter
  setup 2-4
adapter setup register 2-14
address 20 gate 3-30
address and NMI mask register, RT/CMOS 3-19
address map
  memory 3-16
  POS I/O 2-5
  system board I/O 1-8
alternate reset 3-30
altitude 1-13, 1-14
anticipated page miss 1-11, 1-12
arbiter programming 3-8
arbitration control point 3-6
arbitration level 3-7
arbitration register 3-8
arbitration, central control point 3-8

B

base memory bytes 3-27
battery 3-23
boot sequence 3-32
bus adapter 3-9
bus contention 2-3
bus priority assignments 3-7

C

cables 1-13, 1-14
cache
  address space 3-6
cache *(continued)*
  operation 3-5
card selected feedback register 2-6
-CD SFDBK 2-6
central arbitration control point 3-6
channel 1-4, 3-6
  check enable 3-29
  check latch 3-29
  connector 3-9
  DMA 3-7
clock, real-time 3-18, 3-21
CMOS RAM 3-18—3-27
codes, POST error 3-34
compatibility 3-33
configuration
  CRC bytes 3-27
  RT/CMOS 3-24
connector
  channel 3-9
  drives 3-10
  memory 3-11, 3-12
contention, bus 2-3
control ports, system 3-29—3-30
controller
coprocessor, math 3-6
cover lock 3-32
current, electrical 1-13, 1-14

D

data register, RT/CMOS 3-20
date century byte 3-27
date status indicator 3-24
depth, system unit 1-13, 1-14
description, power supply 1-15
diagnostic status byte (RT/CMOS) 3-24
diskette drive
diskette drive connector 3-10
diskette drive connectors 3-10
diskette drive information, POS 2-11

© Copyright IBM Corp. 1991, 1992

diskette drive type byte 3-24
diskette overruns 3-7
display operating mode 3-26
DMA
  channels 3-7
  performance 1-11, 1-12

E

enable NMI 3-19
equipment byte 3-26
error codes, POST 3-34
extended arbitration 3-9

F

failures and messages, POST 3-34
fault, overvoltage 1-17
feedback, card selected 2-6
fixed disk drive
  initialization 3-24
  type byte 3-25

G

gate A20 3-30

H

height, system unit 1-13, 1-14
humidity 1-13, 1-14

I

I/O
  address map 1-8
  RT/CMOS RAM operations 3-20
instruction cycle times A-1
interleaving, memory 3-15
  mem.interleaving 3-15
interrupt
  IRQ0 reset 3-29
  NMI reset 3-28

K

keyboard
  cable 1-13, 1-14
  password 3-32

L

low and high usable memory
  byte 3-27

M

math coprocessor 3-6
measurements, system unit 1-13, 1-14
memory
  bytes 3-27
  connectors 3-11, 3-12
  description 3-13
  performance 1-11, 1-12
  RAM 3-14
  read 1-11, 1-12
  refresh 3-7
  ROM 3-14
  RT/CMOS RAM 3-18
  size miscompare 3-24
  system memory map 3-16
  write 1-11, 1-12
memory information, POS 2-10
memory-presence detect signals 3-15
messages, POST error 3-34
Micro Channel 1-4
Micro Channel architecture
  arbitration control point 3-6
  bus adapter 3-9
  general information 3-6
microprocessor
  386SLC 3-3
  386SLC instructions 3-4
  386SLC programming considerations 3-4
  486SLC2 3-4
  80386SX 3-3
  alternate reset 3-30
  mode switch compatibility 3-30

microprocessor *(continued)*
performance 1-11, 1-12
mode switch, protected 3-30

N

NMI mask register 3-19
NMI service 3-7
NMI signal 3-7
nonmaskable interrupt (NMI) 3-28
nonvolatile RAM (NVRAM) 3-28

O

operating system boot sequence 3-32
output voltage sequencing 1-17
outputs, power supply 1-16
overvoltage fault 1-17

P

page hit 1-11, 1-12
page miss 1-11, 1-12
parallel port select 2-9
parity check enable 3-29
password
keyboard 3-32
power-on 3-30, 3-31
privileged-access 3-32
performance, system 1-11, 1-12
port
system 3-28
POS
See programmable option select (POS)
POS address map 2-5
POS register 3 2-10
POS register, diskette drive 2-11
POST (power-on self-test) 3-14, 3-31
POST error codes 3-34
power
cable 1-13, 1-14
loss 3-23
specifications 1-13, 1-14
power supply 1-4
power supply description 1-15
power supply output protection 1-17
power supply outputs 1-16
power-on password 3-30, 3-31
power-on self-test (POST) 3-14, 3-31
privileged-access password 3-32
programmable option select (POS)
address map 2-5
card selected feedback register 2-6
description 2-3
setup procedures 2-4
system board enable/setup register 2-7
system board setup 2-6
system configuration utilities 2-3
system memory map 3-16
video 2-7
warning 2-3
programming, arbiter 3-8
protected mode switch 3-30
protection, power supply 1-17

R

RAM (random access memory) 3-14
random access memory (RAM) 3-14
read-only memory (ROM) 3-14
real mode switch 3-30
real-time clock 3-18, 3-21
refresh 3-7
refresh request 1-11, 1-12, 3-29
register
adapter setup 2-14
card selected feedback 2-6
miscellaneous system 3-28
RT/CMOS address and NMI mask 3-19
RT/CMOS data 3-20
RT/CMOS status 3-21—3-23
system board enable/setup 2-7
system board POS 2-5

register *(continued)*
system control 3-29
reset, alternate 3-30
ROM (read-only memory) 3-14
RT/CMOS RAM
address and NMI mask register 3-19
address map 3-19
configuration bytes 3-24
data register 3-20
description 3-18
diagnostic status byte 3-24
I/O operations 3-20
power-on password 3-31
secured area 3-30
status registers 3-21—3-23

S

selectable boot 3-32
sequencing, output voltage 1-17
set configuration 3-32
setup
bus contention 2-3
system board 2-6
system board group 1 2-4
system board group 2 2-4
system board group 3 2-5
system board SCSI controller setup 2-5
system memory map 3-16
video 2-7
shutdown status byte 3-24
signal
card selected feedback 2-6
size, system unit 1-13, 1-14
speaker data enable 3-29
specifications
performance 1-11, 1-12
physical 1-13, 1-14
startup sequence 3-32
status registers
(RT/CMOS) 3-21—3-23
switch to real mode 3-30
system
configuration utilities 2-3
control ports 3-29—3-30
system *(continued)*
functions, miscellaneous 3-28
performance 1-11, 1-12
reset 3-28
specifications 1-13, 1-14
system board
address map 1-8
description 3-3
enable/setup register 2-7
memory connector 3-11, 3-12
microprocessors 3-3
POS I/O address map 2-5
setup 2-4, 2-5, 2-6
system description 1-3

T

tamper-evident switch 3-32
temperature 1-13, 1-14
time status indicator 3-24

V

video
setup 2-7
subsystem 2-4
vital product data (VPD) 3-28
VPD 3-28

W

warning
arbitration 3-7
central arbiter 3-9
NMI mask 3-28
POS 2-3
RT/CMOS 3-19
watchdog status 3-30
weight, system unit 1-13, 1-14
width, system unit 1-13, 1-14

Personal System/2
Model 57
Technical Reference

Note

Before using this information and the product it supports, be sure to read the general information under "Notices" on page vii.

Third Edition (October 1992)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer of express or implied warranties in certain transactions, therefore, this statement may not apply to you.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Requests for technical information about IBM products should be made to your IBM Authorized Dealer or your IBM Marketing Representative.

© Copyright International Business Machines Corporation 1991, 1992. All rights reserved.
Note to U.S. Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Contents

Figures v

Notices vii
Trademarks and Service Marks vii

Preface ix

Section 1. System Overview 1-1
Description 1-3
System Board Devices and System Features 1-4
System Board I/O Address Map 1-10
Micro Channel Compatibility 1-12
Specifications 1-13
Power Supply 1-17
Outputs 1-18
Output Protection 1-19
Voltage Sequencing 1-19
Power Supply Connectors 1-19

Section 2. Programmable Option Select 2-1
Description 2-3
POS Address Map 2-5
Card Selected Feedback Register (Hex 0091) 2-6
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-7
System Board Group 1 POS Register 2 (Hex 0102) 2-8
System Board Group 1 POS Register 3 (Hex 0103) 2-10
System Board Group 1 POS Register 4 (Hex 0104) 2-11
System Board Group 1 POS Register 5 (Hex 0105) 2-11
System Board Group 2 POS Register 2 (Hex 0102) 2-12
System Board Group 2 POS Register 3 (Hex 0103) 2-12
System Board Group 3 POS Register 4 (Hex 0104) 2-13
System Board SCSI Controller POS Register 2 (Hex 0102) . . 2-13
System Board SCSI Controller POS Register 3 (Hex 0103) . . 2-14
Adapter Enable/Setup Register (Hex 0096) 2-14

Section 3. System Board 3-1
Description 3-3
Microprocessor—Type 1 Systems 3-3
Microprocessor—Type 2 Systems 3-3
Programming Model 3-4
Instructions 3-4

© Copyright IBM Corp. 1991, 1992

| Microprocessor—Type 3 Systems 3-4
Cache Operation 3-5
Cacheable Address Space 3-6
Math Coprocessor 3-6
Micro Channel Implementation 3-6
Central Arbiter 3-6
Bus Adapter 3-9
| Diskette Drive Connector 3-10
System Board Memory Connectors 3-11
SCSI-Device Connector 3-12
Memory 3-13
ROM Subsystem 3-14
| RAM Subsystem 3-14
| Memory Interleaving Option 3-15
| Memory-Presence Detect Signals 3-15
| System Memory Map 3-16
Memory Controller Registers 3-16
RT/CMOS RAM 3-18
NVRAM 3-28
| Vital Product Data 3-28
Miscellaneous System Functions and Ports 3-28
| Nonmaskable Interrupt 3-28
System Control Port B (Hex 0061) 3-29
System Control Port A (Hex 0092) 3-30
| Power-On Password 3-31
| Privileged-Access Password 3-32
Keyboard Password 3-32
| Cover Lock and Tamper-Evident Switch 3-32
| Selectable Boot Sequence 3-33
Hardware Compatibility 3-33
| Error Codes 3-34

Appendix. 386SLC Instruction Cycle Times A-1

Index X-1

Figures

1-1.	Model and Submodel Bytes	1-3
1-2.	System Board Devices and System Features—57 SX Models	1-4
1-3.	System Board Devices and System Features—57 SLC and Ultimedia M57 SLC Models	1-6
1-4.	System Board Devices and System Features—57 486SLC2 and Ultimedia M57 486SLC2 Models	1-8
1-5.	System Board I/O Address Map	1-10
1-6.	Performance Specifications—57 SX, 57 SLC, and Ultimedia M57 SLC Models	1-13
1-7.	Performance Specifications—57 486SLC2 and Ultimedia M57 486SLC2 Models	1-14
1-8.	Physical Specifications—57 SX, 57 SLC, and Ultimedia M57 SLC Models	1-15
1-9.	Physical Specifications—57 486SLC2 and the Ultimedia M57 486SLC2 Models	1-16
1-10.	Acoustical Readings	1-17
1-11.	Component Maximum Current	1-18
1-12.	Channel Load Current	1-18
1-13.	Voltage Assignments for the Internal Power-Supply Connectors	1-19
2-1.	POS I/O Address Map	2-5
2-2.	Card Selected Feedback Register (Hex 0091)	2-6
2-3.	Devices Supported in Setup Mode	2-7
2-4.	System Board Enable/Setup Register (Hex 0094)	2-7
2-5.	System Board POS Register 2 (Hex 0102)	2-8
2-6.	Parallel Port Select Bits	2-9
2-7.	System Board Group 1 POS Register 3 (Hex 0103)—Write	2-10
2-8.	System Board POS Group 1 Register 3 (Hex 0103)—Read Index 00	2-10
2-9.	System Board POS Group 1 Register 3 (Hex 0103)—Read Index 04	2-11
2-10.	System Board Group 1 POS Register 4 (Hex 0104)	2-11
2-11.	System Board Group 1 POS Register 5 (Hex 0105)	2-11
2-12.	System Board Group 2 POS Register 2 (Hex 0102)	2-12
2-13.	System Board Group 2 POS Register 3 (Hex 0103)	2-12
2-14.	Serial Port Addresses	2-12
2-15.	System Board Group 3 POS Register 4 (Hex 0104)	2-13
2-16.	System Board SCSI Controller POS Register 2 (Hex 0102)	2-13

© Copyright IBM Corp. 1991, 1992

2-17. System Board SCSI Controller POS Register 3 (Hex 0103) 2-14
2-18. System Board SCSI Controller ID 2-14
2-19. Adapter Enable/Setup Register (Hex 0096) 2-14
3-1. Arbitration Bus Priority Assignments 3-7
3-2. Arbitration Register (Hex 0090)—Write 3-8
3-3. Arbitration Register (Hex 0090)—Read 3-8
| 3-4. Diskette Drive Connector 3-10
3-5. System Board Memory Connectors 3-11
3-6. SCSI Device Cable Internal Connector Pin Assignments 3-12
3-7. System Board SCSI Device External Connector 3-13
| 3-8. Memory Interleaving Configurations 3-15
| 3-9. Presence-Detect Bits 3-15
| 3-10. System Memory Map 3-16
3-11. Memory-Fault RAS Capture Register (I/O Port Hex 00E2) 3-17
3-12. Fixed RAS Signals 3-17
3-13. Memory-Controller-Fault Address Register (I/O Port Hex 00E4) 3-18
3-14. Memory-Controller-Fault Address Registers (I/O Port Hex 00E5) 3-18
3-15. RT/CMOS RAM Address Map 3-19
3-16. RT/CMOS Address and NMI Mask Register (Hex 0070) 3-19
3-17. RT/CMOS Data Register (Hex 0071) 3-20
3-18. Real-Time Clock Bytes (Hex 000−00D) 3-21
3-19. Status Register A (Hex 00A) 3-21
3-20. Status Register B (Hex 00B) 3-22
3-21. Status Register C (Hex 00C) 3-23
3-22. Status Register D (Hex 00D) 3-23
3-23. Diagnostic Status Byte (Hex 00E) 3-24
3-24. Diskette Drive Type Byte (Hex 010) 3-25
3-25. Diskette Drive Type Byte (Bits 7−4) 3-25
3-26. Diskette Drive Type Byte (Bits 3−0) 3-25
3-27. Equipment Byte (Hex 014) 3-26
3-28. Installed Diskette Drive Bits 3-26
3-29. Display Operating-Mode Bits 3-26
3-30. System Control Port B (Hex 0061)—Write 3-29
3-31. System Control Port B (Hex 0061)—Read 3-29
3-32. System Control Port A (Hex 0092) 3-30
3-33. POST Error Messages 3-35
A-1. Instruction Cycle Times A-1

Notices

References in this publication to IBM products, programs, or services do not imply that IBM intends to make these available in all countries in which IBM operates. Any reference to an IBM product, program or service is not intended to state or imply that only IBM's product, program, or service may be used. Any functionally equivalent product, program, or service that does not infringe any of IBM's intellectual property rights or other legally protectable rights may be used instead of the IBM product, program, or service. Evaluation and verification of operation in conjunction with other products, programs, or services, except those expressly designated by IBM, are the user's responsibility.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

Trademarks and Service Marks

The following terms, denoted by an asterisk (*) in this publication, are trademarks of the IBM Corporation in the United States and/or other countries:

IBM
Micro Channel
Personal Computer AT
Personal System/2
PS/2
Ultimedia
XGA

The following terms, denoted by a double asterisk (**) in this publication, are trademarks of other companies as follows:

Intel	Intel Corporation
Motorola	Motorola, Incorporated

© Copyright IBM Corp. 1991, 1992

Notes:

Preface

The Technical Reference library is intended for those who develop hardware and software products for IBM Personal Computers and IBM Personal System/2 products. Users should understand computer architecture and programming concepts.

Additions and changes have been made since the second edition of this manual. New or changed information is marked in the text with the same mark that is in the margin of this text.

This manual consists of the following sections:

Section 1, "System Overview," describes the system, features, and specifications.

Section 2, "Programmable Option Select," describes the registers used for configuration.

Section 3, "System Board," describes the system-specific hardware implementations of the Micro Channel architecture.

This technical reference should be used with the following publications. These publications contain additional information on many of the subjects discussed in this technical reference.

IBM Personal System/2 Hardware Interface Technical Reference—Architectures

IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces

IBM Personal System/2 Hardware Interface Technical Reference—Video Subsystems

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference

Information about diskette drives, fixed disk drives, adapters, and external options are in separate option technical references.

Warning: The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

© Copyright IBM Corp. 1991, 1992

Notes:

Section 1. System Overview

| Description 1-3
| System Board Devices and System Features 1-4
| System Board I/O Address Map 1-10
| Micro Channel Compatibility 1-12
| Specifications 1-13
Power Supply 1-17
Outputs 1-18
Output Protection 1-19
Voltage Sequencing 1-19
Power Supply Connectors 1-19

© Copyright IBM Corp. 1991, 1992

Notes:

Description

The IBM* Personal System/2* (PS/2*) Model 57 systems are Micro Channel* systems. They are self-contained desktop computer systems with a keyboard. The systems can support a maximum of four internal drives. Three of these drives can be either removable-media direct access storage devices (DASD) (diskette, tape, optical), or three can be nonremovable-media DASD devices.

Programs can identify the system board by reading the model and submodel bytes. Interrupt 15H, function code (AH) = C0H, returns the model byte, submodel byte, and BIOS revision code. The microprocessor on Type 2 and Type 3 systems contains an internal cache and cache controller.

The following figure lists the model names, model and submodel bytes, system board types, and system-clock speed for all Model 57 system boards.

Model Name	Model Byte (Hex)	Submodel Byte (Hex)	System Board Type	System Clock
57 SX	F8	26	Type 1	20 MHz
57 SLC	F8	25	Type 2	20 MHz
Ultimedia* M57 SLC	F8	25	Type 2	20 MHz
57 486SLC2	F8	38	Type 3	25 MHz/50 MHz
Ultimedia M57 486SLC2	F8	38	Type 3	25 MHz/50 MHz

Figure 1-1. Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems.

* Trademark of the IBM Corporation.

System Board Devices and System Features

The following figure lists the system board devices and system features for the 57 SX models. The *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* describes devices common to PS/2 products by type number.

Device	Type	Features
Microprocessor	—	Type 1 systems (57 SX models) - 80386SX - 24-bit address, 16-bit data interface
System Timers	1	Channel 0-System timer Channel 2-Tone generation for speaker Channel 3-Watchdog timer
ROM Subsystem	—	128KB logical ROM (KB equals 1024 bytes) 256KB physical ROM
RAM Subsystem	—	Three connectors (4MB to 16MB) (MB equals 1048576 bytes) Connectors will accommodate 2MB, 4MB, and 8MB memory modules.
CMOS RAM Subsystem	—	64-byte CMOS RAM with real-time clock/calendar 8KB CMOS RAM extension Battery backup
Audio Subsystem	1	Driven by - System-timer channel 2 - The 'audio sum node' signal
DMA Controller	1	Eight independent DMA channels Single or burst transfers with read verification
Video Subsystem	1	16-bit VGA - 132-column text mode - Mainframe interactive (MFI) support

Figure 1-2 (Part 1 of 2). System Board Devices and System Features—57 SX Models

Device	Type	Features
Interrupt Controller	1	16 levels of system interrupts Interrupts are level sensitive
Keyboard/Auxiliary Device Controller	2	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	2	Supports - 3.5-in. diskette drive (1.44MB and 2.88MB) - 5.25-in. diskette drive (360KB and 1.2MB)
Serial Controller Port	4	One RS-232C interface - One 25-pin connector Programmable as serial ports 1–16 DMA, FIFO, and character modes
Parallel Controller Port	3	Programmable as parallel port 1–4 Supports bidirectional input and output Supports DMA operation
SCSI Controller	1	Supports up to three internal SCSI devices Supports up to seven total SCSI devices
Micro Channel Bus Adapter	—	Five connectors for Type 3 adapters - One 16-bit connector with an auxiliary video extension (slot 2) - Four 16-bit connectors
Math Coprocessor Socket	—	Supports 80387SX math coprocessor option with the same clock speed as the system microprocessor

Figure 1-2 (Part 2 of 2). System Board Devices and System Features—57 SX Models

The following figure lists the system board devices and system features for the 57 SLC and the Ultimedia M57 SLC models. The *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* describes devices common to PS/2 products by type number.

Device	Type	Features
Microprocessor	—	Type 2 systems (57 SLC and Ultimedia M57 SLC models) - IBM 386SLC - 24-bit address, 16-bit data interface - 8KB instruction and data cache with parity
System Timers	1	Channel 0-System timer Channel 2-Tone generation for speaker Channel 3-Watchdog timer
ROM Subsystem	—	128KB logical ROM (KB equals 1024 bytes) 256KB physical ROM
RAM Subsystem	—	Three connectors (4MB to 16MB) (MB equals 1048576 bytes) Connectors will accommodate 2MB, 4MB, and 8MB memory modules.
CMOS RAM Subsystem	—	64-byte CMOS RAM with real-time clock/calendar 8KB CMOS RAM extension Battery backup
Audio Subsystem	1	Driven by - System-timer channel 2 - The 'audio sum node' signal **The following is for the Ultimedia M57 only:** M-Audio Capture and Playback Adapter† Multimedia front panel - Stereo headphone output - Mono microphone input - Enhanced speaker
DMA Controller	1	Eight independent DMA channels Single or burst transfers with read verification

† For information about the M-Audio Capture and Playback Adapter, see the *M-Audio Capture and Playback Adapter Installation and Technical Reference Manual.*

Figure 1-3 (Part 1 of 2). System Board Devices and System Features—57 SLC and Ultimedia M57 SLC Models

Device	Type	Features
Video Subsystem (57 SLC models only)	1	16-bit VGA - 132-column text mode - Mainframe interactive (MFI) support
Video Subsystem (Ultimedia M57 SLC model only)	2	16-bit Extended graphics array (XGA*) adapter - 132-column text mode
Interrupt Controller	1	16 levels of system interrupts Interrupts are level sensitive
Keyboard/Auxiliary Device Controller	2	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	2	Supports - 3.5-in. diskette drive (1.44MB and 2.88MB) - 5.25-in. diskette drive (360KB and 1.2MB)
CD-ROM (Ultimedia M57 SLC model only)	—	CD-ROM-II† - 600MB capacity - CD-XA capability - 330 ms average access time
Serial Controller Port	4	One RS-232C interface - One 25-pin connector Programmable as serial ports 1–16 DMA, FIFO, and character modes
Parallel Controller Port	3	Programmable as parallel port 1–4 Supports bidirectional input and output Supports DMA operation
SCSI Controller	1	Supports up to three internal SCSI devices Supports up to seven total SCSI devices
Micro Channel Bus Adapter	—	Five connectors for Type 3 adapters - One 16-bit connector with an auxiliary video extension (slot 2) - Four 16-bit connectors
Math Coprocessor Socket	—	Supports 80387SX math coprocessor option with the same clock speed as the system microprocessor

† For information about the IBM Personal System/2 CD-ROM-II, see the *IBM Personal System/2 CD-ROM-II Technical Reference.*

Figure 1-3 (Part 2 of 2). System Board Devices and System Features—57 SLC and Ultimedia M57 SLC Models

* Trademark of the IBM Corporation.

The following figure lists the system board devices and system features for the 57 486SLC2 and the Ultimedia M57 486SLC2 models. The *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* describes devices common to PS/2 products by type number.

Device	Type	Features
Microprocessor	—	Type 3 systems (57 486SLC2 and Ultimedia M57 486SLC2 models) - IBM 486SLC2 - 24-bit address, 16-bit data interface - 16KB instruction and data cache with parity
System Timers	1	Channel 0-System timer Channel 2-Tone generation for speaker Channel 3-Watchdog timer
ROM Subsystem	—	128KB logical ROM (KB equals 1024 bytes) 256KB physical ROM
RAM Subsystem	—	Three connectors (8MB to 16MB) (MB equals 1048576 bytes) Connectors will accommodate 2MB, 4MB, and 8MB memory modules.
CMOS RAM Subsystem	—	64-byte CMOS RAM with real-time clock/calendar 8KB CMOS RAM extension Battery backup
EEPROM Subsystem	—	128-byte electrically-erasable programmable read-only memory (EEPROM) Unique system board identifier
Audio Subsystem	1	Driven by - System-timer channel 2 - The 'audio sum node' signal **The following is for the Ultimedia M57 486SLC2 models only:** M-Audio Capture and Playback Adapter† Multimedia front panel - Stereo headphone output - Mono microphone input - Enhanced speaker
DMA Controller	1	Eight independent DMA channels Single or burst transfers with read verification

† For information on the M-Audio Capture and Playback Adapter, see the *M-Audio Capture and Playback Adapter Installation and Technical Reference Manual.*

Figure 1-4 (Part 1 of 2). System Board Devices and System Features—57 486SLC2 and Ultimedia M57 486SLC2 Models

Device	Type	Features
Video Subsystem	3	XGA-2 video - VGA mode - Updated XGA modes - 132-column text mode - 1MB of video memory
Interrupt Controller	1	16 levels of system interrupts Interrupts are level sensitive
Keyboard/Auxiliary Device Controller	2	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	3	Supports - 3.5-in. diskette drive (1.44MB and 2.88MB) - 3.5-in. diskette drive (2.88MB with electronic eject) - 5.25-in. diskette drive (360KB and 1.2MB)
CD-ROM (Ultimedia M57 486SLC2 models only)	—	CD-ROM-II† - 600MB capacity - CD-XA capability - 330 ms average access time
Serial Controller Port	4	RS-232C interface - Two 9-pin connectors Programmable as serial ports 1 – 16 DMA, FIFO, and character modes
Parallel Controller Port	3	Programmable as parallel port 1 – 4 Supports bidirectional input and output Supports DMA operation
SCSI Controller	1	Supports up to three internal SCSI devices Supports up to seven total SCSI devices
Micro Channel Bus Adapter	—	Five connectors for Type 3 adapters - One 16-bit connector with an auxiliary video extension (slot 2) - Four 16-bit connectors
Math Coprocessor Socket	—	Supports 80387SX math coprocessor option with the same clock speed as the system microprocessor

† For information about the IBM Personal System/2 CD-ROM-II, see the *IBM Personal System/2 CD-ROM-II Technical Reference*.

Figure 1-4 (Part 2 of 2). System Board Devices and System Features—57 486SLC2 and Ultimedia M57 486SLC2 Models

System Board I/O Address Map

The following figure is the Model 57 system board I/O address map.

Address (Hex)	Device
0000–001F	DMA controller (0–3)
0020, 0021	Interrupt controller
0040, 0042–0044, 0047	System timers
004B–004F	32-bit free running timer (Type 3 system board only)
0060	Keyboard, auxiliary device
0061	System Control Port B
0064	Keyboard, auxiliary device
0066–0067	Keyboard, auxiliary device
0070, 0071	RT/CMOS and NMI mask
0074, 0075, 0076	8K x8 NVRAM
0078–007C	Reserved
0081–0083, 0087	DMA Page registers (0–3)
0089–008B, 008F	DMA Page registers (4–7)
0090	Central arbitration control point
0091	Card Selected Feedback register
0092	System Control Port A
0094	System Board Enable/Setup register
0096	Adapter Enable/Setup register
00A0, 00A1	Interrupt controller
00C0–00DF	DMA controller (4–7)
00E0–00E5	Memory controller
00F0–00FF	Math coprocessor
0100–0107	Programmable option select
0278–027D	Parallel Port 3
02F8–02FF	Serial Port 2
0378–037D	Parallel Port 2
03B4, 03B5, 03BA	Video subsystem
03BC–03BF	Parallel Port 1
03C0–03C5	Video subsystem
03C6–03C9	Video DAC
03CA, 03CC, 03CE, 03CF	Video subsystem
03D4, 03D5, 03DA	Video subsystem
03F0–03F7	Diskette drive controller
03F8–03FF	Serial Port 1
1278–127D	Enhanced Parallel Port 1
1378–137D	Parallel Port 4

Figure 1-5 (Part 1 of 2). System Board I/O Address Map

Address (Hex)	Device
2100–210F	XGA video instance 0
2110–211F	XGA video instance 1
2120–212F	XGA video instance 2
2130–213F	XGA video instance 3
2140–214F	XGA video instance 4
2150–215F	XGA video instance 5
2160–216F	XGA video instance 6
2170–217F	XGA video instance 7
3220–3227	Serial Port 3
3228–322F	Serial Port 4
3540–3547	SCSI controller
3A20–3A27	Serial Port 9
3A28–3A2F	Serial Port 10
3A30–3A37	Serial Port 11
3A38–3A3F	Serial Port 12
3A80–3A87	Serial Port 13
3A88–3A8F	Serial Port 14
3A90–3A97	Serial Port 15
3A98–3A9F	Serial Port 16
4220–4227	Serial Port 5
4228–422F	Serial Port 6
4620–462F	Serial port arbitration-level control
5220–5227	Serial Port 7
5228–522F	Serial Port 8
82F8–82FF	Enhanced Serial Port 2
83F8–83FF	Enhanced Serial Port 1
B220–B227	Enhanced Serial Port 3
B228–B22F	Enhanced Serial Port 4
BA20–BA27	Enhanced Serial Port 9
BA28–BA2F	Enhanced Serial Port 10
BA30–BA37	Enhanced Serial Port 11
BA38–BA3F	Enhanced Serial Port 12
BA80–BA87	Enhanced Serial Port 13
BA88–BA8F	Enhanced Serial Port 14
BA90–BA97	Enhanced Serial Port 15
BA98–BA9F	Enhanced Serial Port 16
C220–C227	Enhanced Serial Port 5
C228–C22F	Enhanced Serial Port 6
D220–D227	Enhanced Serial Port 7
D228–D22F	Enhanced Serial Port 8

Figure 1-5 (Part 2 of 2). System Board I/O Address Map

Micro Channel Compatibility

The following terms describe system limitations supporting Micro Channel.

Streaming Data

The system board supports 10-MHz streaming-data procedures involving transfers between adapters; but the devices on the system board do not *use* the streaming-data procedures. Transfers default to the basic transfer procedure.

Data Parity

The system board supports data-parity procedures involving transfers between adapters; but the devices on the system board do not *use* the data-parity procedures. Transfers default to the basic transfer procedure.

Select Feedback Return Indicator (Port Hex 91)

The system board supports the 'selected feedback return' indicator except for the I/O devices at addresses below hex 0100. These devices are controlled by the system master only and should not be accessed by bus masters.

Synchronous Channel Check

Synchronous channel checks for errors other than Micro Channel data-parity errors are not supported in this system.

Synchronous channel checks for data-parity errors, typically issued by slaves, are the responsibility of the master that owned the channel and issued the access to the slave. However, in this system, these channel checks are detected by logic on the system board, resulting in a nonmaskable interrupt (NMI).

DMA

In this system, the DMA controller supports DMA slaves with 8-bit or 16-bit data widths.

Specifications

The following figure contains the performance specifications for the 57 SX, the 57 SLC, and the Ultimedia M57 SLC models.

Device	Cycle Time (ns)
Microprocessor (20 MHz—50 ns Clock)	
Pipelined access to system board RAM†	
Memory read/write (page hit)	100
Memory read/write (page miss/bank miss)	150
Memory read/write (page miss)	200
Nonpipelined access to system board RAM†	
Memory read/write (page hit)	150
Memory read/write (page miss/bank miss)	200
Memory read/write (page miss)	250
Access to Channel	
Default transfer cycle	250
Synchronous transfer cycle	350
Access to ROM	200
Refresh Rate (typically performed every 15.1 μs)	500 (min) 800 (typical)
Bus-Master Access to System Board RAM	
Page hit	320 (min)
Page miss	370 (min)
DMA Controller (10 MHz—100 ns Clock)	
Single transfer: 300 + (I/O access + memory access)	
Burst transfer: 300 + (I/O access + memory access)*n*‡	
System board memory access	200–350
Default transfer cycle	350 (min)
Synchronous transfer cycle	450 (min)

† Adapters installed in the channel should not rely on monitoring system board memory access, because channel-memory control signals might not be present during these accesses.

‡ *n* equals the number of transfers in the burst.

Note: The cycle times shown for access to system board RAM are based on 70-nanosecond memory.

Figure 1-6. Performance Specifications—57 SX, 57 SLC, and Ultimedia M57 SLC Models

The following figure contains the performance specifications for the 57 486SLC2 and the Ultimedia M57 486SLC2 models.

Device	Cycle Time (ns)
Microprocessor (25 MHz—40 ns Clock)	
Pipelined access to system board RAM†	
Memory read/write (page hit)	80
Memory read/write (page miss/bank miss)	120
Memory read/write (page miss)	160
Nonpipelined access to system board RAM†	
Memory read/write (page hit)	120
Memory read/write (page miss/bank miss)	160
Memory read/write (page miss)	200
Access to Channel	
Default transfer cycle	240
Synchronous transfer cycle	320
Access to ROM	200
Refresh Rate (typically performed every 15.1 μs)	400 (min) 640 (typical)
Bus-Master Access to System Board RAM	
Page hit	300 (min)
Page miss	320 (min)
DMA Controller (12.5 MHz—80 ns Clock)	
Single transfer: 240 + (I/O access + memory access)	
Burst transfer: 240 + (I/O access + memory access)*n*‡	
System board memory access	160–320
Default transfer cycle	305 (min)
Synchronous transfer cycle	405 (min)

† Adapters installed in the channel should not rely on monitoring system board memory access, because channel-memory control signals might not be present during these accesses.

‡ *n* equals the number of transfers in the burst.

Note: The cycle times shown for access to system board RAM are based on 70-nanosecond memory.

Figure 1-7. Performance Specifications—57 486SLC2 and Ultimedia M57 486SLC2 Models

| The following figure describes the physical specifications of the 57
| SX, the 57 SLC, and the Ultimedia M57 SLC models.

Specification	Measurements
Size	
Width	440 mm (17.3 in.)
Depth	394 mm (15.5 in.)
Height	168 mm (6.6 in.)
Weight	
Minimum configuration	12.0 kg (26 lb)
Maximum configuration	15.9 kg (35 lb)
Cables	
Power cable	1.8 m (6 ft)
Keyboard cable	1.8 m (6 ft)
Air Temperature	
System on	10.0 to 35.0°C (50 to 95°F) 0 – 7000 ft
System off	10.0 to 43.0°C (50 to 110°F)
Humidity	
System on	8% to 85%
System off	5% to 85%
Maximum Altitude	2133.6 m (7000 ft)
Heat Output	(300 watts) 1030 BTUs per hour
Acoustical Readings	See Figure 1-10 on page 1-17
Electrical	
Input voltage (range is switch selected; sinewave input is required)	
Low range	90 (min) – 137 (max) V ac
High range	180 (min) – 265 (max) V ac
Input frequency	50 ± 3 Hz or 60 ± 3 Hz
Maximum current draw	
Low range	4.6 A
High range	2.0 A
Input in kilovolt-ampere (kVA)	
Minimum configuration (as shipped by IBM)	0.07 kVA
Maximum configuration	0.50 kVA
Electromagnetic Compatibility	FCC Class B

Figure 1-8. Physical Specifications—57 SX, 57 SLC, and Ultimedia M57 SLC Models

The following figure describes the physical specifications of the 57 486SLC2 and the Ultimedia M57 486SLC2 models.

Specification	Measurements
Size	
Width	440 mm (17.3 in.)
Depth	394 mm (15.5 in.)
Height	168 mm (6.6 in.)
Weight	
Minimum configuration	11.8 kg (26 lb)
Maximum configuration	15.9 kg (35 lb)
Cables	
Power cable	1.8 m (6 ft)
Keyboard cable	2.7 m (9 ft)
Air Temperature	
System on	10.0 to 35.0°C (50 to 95°F) 0 – 3000 ft 10.0 to 32.2°C (50 to 90°F) 3000 – 7000 ft
System off	10.0 to 43.0°C (50 to 110°F)
Humidity	
System on	8% to 85%
System off	5% to 85%
Maximum Altitude	2133.6 m (7000 ft)
Heat Output as shipped	(35 watts) 123 BTUs per hour
Maximum configuration	(250 watts) 875 BTUs per hour
Acoustical Readings	See Figure 1-10 on page 1-17
Electrical	
Input voltage (range is switch selected; sinewave input is required)	
Low range	90 (min) – 137 (max) V ac
High range	180 (min) – 265 (max) V ac
Input frequency	50 ± 3 Hz or 60 ± 3 Hz
Power Supply	197 watts
Maximum current draw	
Low range	4.6 A
High range	2.0 A
Input in kilovolt-ampere (kVA)	
Minimum configuration (as shipped by IBM)	0.07 kVA
Maximum configuration	0.50 kVA
Electromagnetic Compatibility	FCC Class B

Figure 1-9. Physical Specifications—57 486SLC2 and the Ultimedia M57 486SLC2 Models

The following figure contains the acoustical readings for all Model 57 systems.

Description	L_{WAd} in bels Operate	Idle	L_{pAm} in dB Operate	Idle	$<L_{pA}>_m$ in dB Operate	Idle
Model 57	5.0	5.0	41	41	36	35

Notes

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

All measurements are made in accordance with ANSI standard 12.10 and reported in conformance with ISO DIS 9296.

The measurements are preliminary data and subject to change.

Figure 1-10. Acoustical Readings

Power Supply

The power supply converts the ac input voltage to three dc output voltages and provides power for the following:

- System board
- Micro Channel adapters
- Internal DASD drives
- Auxiliary devices
- Keyboard
- Multimedia control panel (for the Ultimedia M57 SLC and the Ultimedia M57 486SLC2 models only)

The power switch and two light-emitting diodes (LED) are on the front of the system unit. The power supply is operating properly when the green LED is lit. The amber LED is the fixed-disk-activity indicator.

Outputs

The power supply provides separate voltage sources for the system board and the drives. The system board voltages are +5 V dc, +12 V dc, and −12 V dc. The drive voltages are +5 V dc and +12 V dc.

The following figure shows the maximum current provided for system components.

System Component	Maximum Current	
	+12 V dc	+5 V dc
Internal fixed disk drives†	4.5 A	5.0 A
Auxiliary device	None	300 mA
Keyboard	None	275 mA
† Total for three power-supply connectors.		

Figure 1-11. Component Maximum Current

The following figure shows the maximum load currents allowed for each channel connector.

Supply Voltage	Maximum Load Current
+ 5.0 V dc	1.6 A
+12.0 V dc	0.175 A
−12.0 V dc	0.040 A

Figure 1-12. Channel Load Current

The formulas used to determine the power requirements and the voltage regulation tolerances are in the Micro Channel architecture information in the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures.*

Output Protection

A short circuit placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state, with no damage to the power supply.

If an overvoltage fault occurs in the power supply, the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of the nominal value of the power supply.

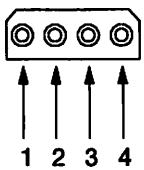
If either of these shutdown states occurs, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least ten seconds.

Voltage Sequencing

During power-on, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Power Supply Connectors

The power supply provides three 4-pin connectors for internal devices. The total power used by both connectors must not exceed the amount shown in Figure 1-11 on page 1-18.



Pin	Signal	Pin	Signal
1	+12 V dc	3	dc return
2	dc return	4	+5 V dc

Figure 1-13. Voltage Assignments for the Internal Power-Supply Connectors

Notes:

Section 2. Programmable Option Select

| Description 2-3
POS Address Map 2-5
Card Selected Feedback Register (Hex 0091) 2-6
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-7
System Board Group 1 POS Register 2 (Hex 0102) 2-8
| System Board Group 1 POS Register 3 (Hex 0103) 2-10
System Board Group 1 POS Register 4 (Hex 0104) 2-11
System Board Group 1 POS Register 5 (Hex 0105) 2-11
| System Board Group 2 POS Register 2 (Hex 0102) 2-12
| System Board Group 2 POS Register 3 (Hex 0103) 2-12
System Board Group 3 POS Register 4 (Hex 0104) 2-13
System Board SCSI Controller POS Register 2 (Hex 0102) . . 2-13
System Board SCSI Controller POS Register 3 (Hex 0103) . . 2-14
Adapter Enable/Setup Register (Hex 0096) 2-14

© Copyright IBM Corp. 1991, 1992

Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used on all Model 57 system boards. For additional POS information, refer to the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures.*

Note: For the Ultimedia M57 SLC and the Ultimedia M57 486SLC2 models, there is additional POS information for the M-Audio Capture and Playback Adapter. Refer to the *M-Audio Capture and Playback Adapter Installation and Technical Reference Manual* for more information.

Warning:

- IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignments of the same system resource, improper operation of the feature, loss of data, or damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention occurs, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- The channel-reset bit (bit 7) in the Adapter Enable/Setup register (hex 0096) must be set to 0 to program the adapters.
- The system board does not support 16-bit I/O operations to 8-bit POS registers. Using 16-bit I/O instructions on 8-bit POS registers causes incorrect data to be written to or read from the registers. Only 8-bit transfers are supported for setup operations.

Setup functions respond to I/O addresses hex 0100 through hex 0107 only when their unique setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

System Board Video Subsystem Setup:

- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 0 to place the system board video into the setup mode.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bits 7, 6, 4, and 3 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system board functions.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register must be set to 1 to allow adapter setup.
- Bits 7–3 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to system board or video subsystem functions.

System Board Setup Group 1:

- Bit 7 in the System Board Enable/Setup register must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bits 6–3 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem or other system board functions.

System Board Setup Group 2:

- Bit 6 in the System Board Enable/Setup register must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bits 7, 5, 4, and 3 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem or other system board functions.

System Board Setup Group 3:

- Bit 4 in the System Board Enable/Setup register must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bits 7, 6, 5, and 3 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem or other system board functions.

System Board SCSI Controller Setup:

- Bit 3 in the System Board Enable/Setup register must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bits 7–4 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem or other system board functions.

POS Address Map

The following figure shows the organization of the I/O address space used by POS. Bit 0 of POS Register 2 and bits 6 and 7 of POS Register 5 are fixed. All other bits in POS Registers 2 through 5 are free form.

Address (Hex)	Function
0094	System Board Enable/Setup register
0096	Adapter Enable/Setup register
0100	POS Register 0—Adapter Identification byte (low byte)
0101	POS Register 1—Adapter Identification byte (high byte)
0102	POS Register 2—Option Select Data byte 1 – Bit 0 is card enable
0103	POS Register 3—Option Select Data byte 2
0104	POS Register 4—Option Select Data byte 3
0105	POS Register 5—Option Select Data byte 4
0106	Reserved
0107	Reserved

Figure 2-1. POS I/O Address Map

Card Selected Feedback Register (Hex 0091)

Whenever an adapter is addressed, it responds by setting the '-card selected feedback' (-CD SFDBK) signal to active. -CD SFDBK is derived from the address decode, driven by a totem-pole driver, and latched by the system board. It can be read through the Card Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs can use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and determine if the video subsystem, system board I/O, or an adapter is addressed and functioning.

Bit	Function
7–1	Reserved
0	Card selected feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7–1 These bits are reserved.

Bit 0 This bit is set to 1 whenever -CD SFDBK was active on a previous cycle or whenever the system board I/O functions (diskette drive, serial, or parallel interfaces) are accessed by an I/O cycle. Reading this register resets the bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information during setup. The diskette drive controller, serial port, and parallel port are treated as a single device. The video subsystem also is an integrated part of the system board, but POS treats it as a separate device. The System Board Enable/Setup register is used to place the system board or the video subsystem in the setup mode.

Figure 2-3 indicates the group, POS register number, and I/O function supported.

Group	POS Register	Device
1	2	Diskette drive Parallel port controllers
1	3	Memory connectors
1	4	Diskette arbitration level
1	5	Parallel port arbitration level
2	2, 3	Serial port controller
3	4	SCSI controller arbitration level
SCSI Controller	2, 3	Enable SCSI controller

Figure 2-3. Devices Supported in Setup Mode

System Board Enable/Setup Register (Hex 0094)

This is a read/write register. All bits in this register default to 1 (enabled).

Bit	Function
7	Enable/setup system board group 1
6	Enable/setup system board group 2
5	Enable/setup video subsystem
4	Enable/setup system board group 3
3	Enable/setup SCSI controller
2–0	Reserved

Figure 2-4. System Board Enable/Setup Register (Hex 0094)

Bit 7 When this bit is set to 0, it places the diskette drive controller, parallel port controllers, memory connectors, diskette arbitration level, and parallel port arbitration level in setup mode.

When this bit is set to 1, it enables the system board functions.

Bit 6 When this bit is set to 0, it places the system board serial controller in setup mode. System Board Group 2 POS Register 2 (hex 0102) includes the serial port enable and interrupt-level selection. The serial port address selection is in System Board Group 2 POS Register 3 (hex 0103).

Bit 5 When this bit is set to 0, the video subsystem is placed in the setup mode and controlled through Group 1 POS Register 2 (hex 0102). When this bit is set to 1 and bit 0 in Group 1 POS Register 2 is set to 1, video is enabled.

Bit 0 of Group 1 POS Register 2 is the video-enable bit. When this bit is set to 0, the video subsystem does not respond to commands, addresses, or data. If video is being generated when the video-enable bit is set to 0, the output is still generated. For information on BIOS calls to enable or disable the video, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Note: When the video subsystem is disabled, access to the Digital-to-Analog Converter (DAC) registers is disabled.

Bit 4 When this bit is set to 0, the system board bus controller is placed in setup mode and controlled through POS Register 4 (hex 0104). POS Register 4 includes the system board SCSI-controller arbitration level. All other bits in POS Register 4 and POS Register 5 are reserved.

Bit 3 When this bit is set to 0, the system board SCSI controller is placed in setup mode and is controlled through POS Register 2 (hex 0102). When this bit is set to 1 and bit 0 in POS Register 2 is set to 1, the system board SCSI controller is enabled.

Bits 2–0 These bits are reserved.

System Board Group 1 POS Register 2 (Hex 0102)

When the system board is in the setup mode, this read/write register controls the diskette drive controller, serial port, and parallel port. Reading this register returns the current state of these system board functions.

Bit	Function
7	Disable parallel port extended mode
6, 5	Select parallel port
4	Enable parallel port
3	Reserved
2	Reserved
1	Enable diskette drive interface
0	Enable system board

Figure 2-5. System Board POS Register 2 (Hex 0102)

Bit 7 When this bit is set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional (extended mode) interface. When this bit is set to 1, this bit disables the bidirectional mode. This bit is set to 0 after power-on.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Hex Address	Interrupt Level
0 0	Parallel 1	03BC–03BF†	7
0 1	Parallel 2	0378–037D	7
1 0	Parallel 3	0278–027D	7
1 1	Parallel 4	1378–137D	7

† The addresses are hex 1278–127D for the DMA operations.

Figure 2-6. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bits 3, 2 These bits are reserved.

Bit 1 When this bit and bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When this bit is set to 1, bits 4 and 1 can enable and disable their respective devices. When this bit is set to 0, this bit disables the diskette drive interface and system board serial and parallel ports, regardless of the state of bits 4 and 1.

System Board Group 1 POS Register 3 (Hex 0103)

The system board has connectors that provide for installation of three single inline memory modules (memory modules) (for more information about these memory connectors, see "System Board Memory Connectors" on page 3-11). Information about each memory module is contained in four read-only data bits in POS Register 3. Each set of data bits is selected by writing the appropriate index to the write-only index register.

POS Register 3 provides access to the read-only data bits and a write-only index register. To determine the memory information for a particular connector, write the appropriate index to POS Register 3, then read POS Register 3. The following figure shows the relationship of the index value, the memory connector, and the available data register information.

Index Value (Hex)	Function
00	Presence detection information for memory connectors 2 and 1
04	Presence detection information for memory connector 3

Note: All values that are not shown are reserved.

Figure 2-7. System Board Group 1 POS Register 3 (Hex 0103)—Write

The following information is returned by reading POS Register 3 after the appropriate index value has been written to POS Register 3. For coding of the presence detection signals, see Figure 3-9 on page 3-15.

Index 00 Bit	Function
7	Presence detect 3, memory connector 2
6	Presence detect 2, memory connector 2
5	Presence detect 1, memory connector 2
4	Presence detect 0, memory connector 2
3	Presence detect 3, memory connector 1
2	Presence detect 2, memory connector 1
1	Presence detect 1, memory connector 1
0	Presence detect 0, memory connector 1

Figure 2-8. System Board POS Group 1 Register 3 (Hex 0103)—Read Index 00

Index 04 Bit	Function
7–4	Reserved
3	Presence detect 3, memory connector 3
2	Presence detect 2, memory connector 3
1	Presence detect 1, memory connector 3
0	Presence detect 0, memory connector 3

Figure 2-9. System Board POS Group 1 Register 3 (Hex 0103)—Read Index 04

System Board Group 1 POS Register 4 (Hex 0104)

This register is used to specify the diskette arbitration level.

Bit	Function
7–4	Reserved
3–0	Diskette arbitration level

Figure 2-10. System Board Group 1 POS Register 4 (Hex 0104)

Bits 7–4 These bits are reserved.

Bits 3–0 These bits select the diskette arbitration level.

System Board Group 1 POS Register 5 (Hex 0105)

This register is used to specify the arbitration level used by the parallel port controller.

Bit	Function
7–4	Reserved
3–0	Parallel port arbitration level

Figure 2-11. System Board Group 1 POS Register 5 (Hex 0105)

Bits 7–4 These bits are reserved.

Bits 3–0 These bits are used to select the arbitration level used by the parallel port controller.

System Board Group 2 POS Register 2 (Hex 0102)

This register is used to enable the system board serial ports.

Bit	Function
7–6	Reserved
5	Enable Serial Port B
4	Enable Serial Port A
3–2	Reserved
1	Select Serial Port B interrupt
0	Select Serial Port A interrupt

Figure 2-12. System Board Group 2 POS Register 2 (Hex 0102)

Bits 7–6 These bits are reserved.

Bit 5 When this bit is set to 1 and bit 0 in POS Register 2 (Group 1) is set to 1, Serial Port B is enabled.

Bit 4 When this bit is set to 1 and bit 0 in POS Register 2 (Group 1) is set to 1, Serial Port A is enabled.

Bits 3–2 These bits are reserved.

Bit 1 When this bit is set to 1, Serial Port B uses IRQ4. When this bit is set to 0, Serial Port B uses IRQ3.

Bit 0 When this bit is set to 1, Serial Port A uses IRQ4. When this bit is set to 0, Serial Port A uses IRQ3.

System Board Group 2 POS Register 3 (Hex 0103)

This register is used to select the address of the serial ports.

Bit	Function
7–4	Serial Port B address
3–0	Serial Port A address

Figure 2-13. System Board Group 2 POS Register 3 (Hex 0103)

Bits 7–4 These bits are used to determine the address of Serial Port B.

Bits 3–0 These bits are used to determine the address of Serial Port A.

Bits 7 6 5 4 3 2 1 0	Assignment	Hex Address	
		Compatible	Extended
0 0 0 0	Serial 1	03F8–03FF	83F8–83FF
0 0 0 1	Serial 2	02F8–02FF	82F8–82FF
0 0 1 0	Serial 3	3220–3227	B220–B227
0 0 1 1	Serial 4	3228–322F	B228–B22F
0 1 0 0	Serial 5	4220–4227	C220–C227
0 1 0 1	Serial 6	4228–422F	C228–C22F
0 1 1 0	Serial 7	5220–5227	D220–D227
0 1 1 1	Serial 8	5228–522F	D228–D22F
1 0 0 0	Serial 9	3A20–3A27	BA20–BA27
1 0 0 1	Serial 10	3A28–3A2F	BA28–BA2F
1 0 1 0	Serial 11	3A30–3A37	BA30–BA37
1 0 1 1	Serial 12	3A38–3A3F	BA38–BA3F
1 1 0 0	Serial 13	3A80–3A87	BA80–BA87
1 1 0 1	Serial 14	3A88–3A8F	BA88–BA8F
1 1 1 0	Serial 15	3A90–3A97	BA90–BA97
1 1 1 1	Serial 16	3A98–3A9F	BA98–BA9F

Figure 2-14. Serial Port Addresses

System Board Group 3 POS Register 4 (Hex 0104)

This register is used to select the arbitration level of the SCSI controller on the system board.

Bit	Function
7–4	SCSI arbitration level (system board)
3–0	Reserved

Figure 2-15. System Board Group 3 POS Register 4 (Hex 0104)

Bits 7–4 These bits select the SCSI arbitration level.

Bits 3–0 These bits are reserved.

System Board SCSI Controller POS Register 2 (Hex 0102)

This register is used to enable the system board SCSI controller.

Bit	Function
7–1	Reserved
0	Enable SCSI

Figure 2-16. System Board SCSI Controller POS Register 2 (Hex 0102)

Bits 7–1 These bits are reserved.

Bit 0 When this bit is set to 1, this bit enables the system board SCSI controller.

System Board SCSI Controller POS Register 3 (Hex 0103)

This register is used to select the SCSI ID for the system board SCSI controller.

Bit	Function
7–5	SCSI ID
4–0	Reserved

Figure 2-17. System Board SCSI Controller POS Register 3 (Hex 0103)

Bits 7–5 These bits determine the SCSI ID for the system board SCSI controller as follows:

Bits 7 6 5	System Board SCSI ID
0 0 0	0
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	4
1 0 1	5
1 1 0	6
1 1 1	7

Figure 2-18. System Board SCSI Controller ID

Bits 4–0 These bits are reserved.

Adapter Enable/Setup Register (Hex 0096)

This read/write register resets the channel, enables the '-card setup' signal, and configures the connectors.

Bit	Function
7	Channel reset
6–4	Reserved
3	Enable card setup
2–0	Channel select 2–0

Figure 2-19. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When this bit is set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6–4 These bits are reserved and must be set to 0.

Bit 3 When this bit is set to 1, this bit enables the '-card setup' signal selected by bits 2–0.

Bits 2–0 These bits are the address bits for the '-card setup' signal to the connectors. Connectors 1 through 5 are addressed as 0 through 4. When bit 3 is set to 1, these bits select the connector or function for setup cycles.

Each channel connector has a unique '-card setup' signal (-CD SETUP) associated with it. This signal is used to select the adapters for setup cycles, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Note: -CD SETUP goes active only when an operation is performed in the I/O address range hex 0100 through 0107.

Notes:

Section 3. System Board

| Description 3-3
Microprocessor—Type 1 Systems 3-3
Microprocessor—Type 2 Systems 3-3
Programming Model 3-4
Instructions 3-4
| Microprocessor—Type 3 Systems 3-4
Cache Operation 3-5
Cacheable Address Space 3-6
Math Coprocessor 3-6
Micro Channel Implementation 3-6
Central Arbiter 3-6
Arbitration Bus Priority Assignments 3-7
Central Arbiter Programming 3-8
Bus Adapter 3-9
| Diskette Drive Connector 3-10
System Board Memory Connectors 3-11
SCSI-Device Connector 3-12
Memory 3-13
ROM Subsystem 3-14
| RAM Subsystem 3-14
| Memory Interleaving Option 3-15
| Memory-Presence Detect Signals 3-15
| System Memory Map 3-16
Memory Controller Registers 3-16
Memory-Fault RAS Capture Register (I/O Port Hex 00E2) . 3-17
Memory-Controller-Fault Address Registers (I/O Ports Hex 00E4 and Hex 00E5) 3-17
RT/CMOS RAM 3-18
RT/CMOS Address and NMI Mask Register (Hex 0070) . . 3-19
RT/CMOS Data Register (Hex 0071) 3-20
RT/CMOS RAM I/O Operations 3-20
Real-Time Clock Bytes (Hex 000−00D) 3-21
CMOS RAM Configuration 3-24
NVRAM 3-28
| Vital Product Data 3-28
Miscellaneous System Functions and Ports 3-28
| Nonmaskable Interrupt 3-28
System Control Port B (Hex 0061) 3-29
System Control Port A (Hex 0092) 3-30
| Power-On Password 3-31
| Privileged-Access Password 3-32
Keyboard Password 3-32

© Copyright IBM Corp. 1991, 1992

| Cover Lock and Tamper-Evident Switch 3-32
| Selectable Boot Sequence 3-33
Hardware Compatibility 3-33
| Error Codes 3-34

Description

This section describes the microprocessors, math coprocessor, channel differences, memory subsystems, and miscellaneous system ports and connectors for the all Model 57 systems. Additional information on these topics can be found in the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces.*

Type 1 systems contain an 80386SX microprocessor, Type 2 systems contain a 386SLC microprocessor, and Type 3 systems contain a 486SLC2 microprocessor. To identify the microprocessor used in the system unit, use INT 15H, function code 0C9H. This returns the microprocessor type and stepping level.

Microprocessor—Type 1 Systems

The 80386SX microprocessor used in Type 1 systems runs at 20 MHz and has a 24-bit address and a 16-bit data interface. The 80386SX microprocessor is software compatible with the 80386DX microprocessor. The type for the 80386SX is hex 023.

Microprocessor—Type 2 Systems

The 386SLC microprocessor used in Type 2 systems runs at 20 MHz and has an 8KB, 2-way set-associative store-through instruction and data cache. It contains an internal 32-bit data path (including the path to the cache) with external 16-bit data and 24-bit address paths. The 386SLC maintains binary compatibility with programs written for the 80386SX. The type for the IBM 386SLC is hex 0A3.

Programming Model

The IBM 386SLC microprocessor implements the same registers and bit descriptions as the Intel** 80386SX with the following additions:

- The 386SLC implements the WP bit in the CR0 of the Intel486** microprocessor.
- The 386SLC implements the PCD bit in the Page Table Entry of the Intel486 microprocessor.

Instructions

The 386SLC microprocessor decodes the same instructions as the 80386SX. The 386SLC microprocessor also decodes the following 6 Intel486 instructions:

- BSWAP
- XADD
- CMPXCHG
- INVD
- WBINVD
- INVLPG

Microprocessor—Type 3 Systems

The 486SLC2 microprocessor used in Type 3 systems runs at 50 MHz internally and 25 MHz externally. It has a 24-bit address and a 16-bit data interface. The 486SLC2 microprocessor is software compatible with the 80486SX microprocessor, the 80386DX microprocessor, and the 80386SX microprocessor. The type for the 486SLC2 is hex 0A4.

** Trademark of Intel Corporation.

Cache Operation

The cache in the 386SLC microprocessor (8KB) and the 486SLC2 microprocessor (16KB) enables it to read instructions and data much faster than if the microprocessor had to access system memory. When instructions are first used or data is first read or written, they are transferred to the cache from main memory. This enables future accesses to the instructions or data to occur much faster.

The cache is disabled and empty when the microprocessor comes out of the reset state. The cache is tested and enabled during the power-on self-test (POST).

The cache is loaded from system memory in 16-byte increments. These increments are referred to as a cache line. A cache line is aligned on a paragraph boundary. A reference to any byte contained in the line results in the entire cache line being read into the cache (if the data was not already in the cache). When the microprocessor gives up control of the system bus, the cache enters a "snoop" mode and monitors all write operations. If a memory write occurs to a location that is in the cache, the corresponding cache line is invalidated.

When the microprocessor performs a memory read, the address is used to find the data in the cache. If the data is found (a hit), it is read from the cache and no external bus cycle occurs. If the data is not found (a miss), an external bus cycle is used to read the data from system memory. If the address of the missed data is in cacheable address space, the data is stored in the cache and the rest of the cache line is read.

When the microprocessor performs a memory write, the address is used to search the cache. If found, the data is written to the cache. Then (hit or miss), an external bus cycle is used to write the data to system memory. If the address of the write operation was not in the cache but was in cacheable address space, the data is read back into the cache and the rest of the cache line is read.

Cacheable Address Space

Cacheable address space is defined as system memory that resides on the system board (0 – 640KB and 1MB – 16MB). Nothing in the address range hex A0000 – DFFFF is cached, and no memory that is located in any Micro Channel slot is cached. Nothing in the I/O address space is cached.

ROM address space (hex E0000 – FFFFF) is cacheable for *read operations only*. If data in this address range is already in cache and the address range is written to, the cached line is invalidated and is read again from the ROM.

Math Coprocessor

The 80387SX math coprocessor is matched to the speed of the system microprocessor and operates in the synchronous mode. The 80387SX math coprocessor is software compatible with the 80387DX math coprocessor.

Micro Channel Implementation

This section describes the implementation of the Micro Channel architecture on Model 57 systems. For general Micro Channel architecture information, refer to the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures.*

Central Arbiter

The central arbitration control point gives programmable subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. The central arbiter supports up to 15 arbitrating devices (levels 0 through E) and the system microprocessor (level F).

Note: The system board SCSI controller performs cycles at arbitration level F if the Micro Channel arbitration level is F when the SCSI controller requests the bus.

Arbitration Bus Priority Assignments

The following figure shows the assignment of arbitration levels. The functions with the *lowest* arbitration level have the *highest* priority.

ARB Level	Primary Assignment
−2	Memory refresh
−1	NMI
0	DMA channel 0 (Programmable to any arbitration level)
1	DMA channel 1
2	DMA channel 2
3	DMA channel 3
4	DMA channel 4 (programmable to any arbitration level)
5	DMA channel 5
6	DMA channel 6
7	DMA channel 7
8−E	Available
F	System microprocessor

Figure 3-1. Arbitration Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so that diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, normally on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation, and by the previous controlling master. To prevent overrun, the diskette drive controller should not be held inactive for more than 12 microseconds.

Nonmaskable interrupt (NMI) service is executed at a priority level higher than 0, called −1. Memory refresh is prioritized at −2, two levels higher than 0. Levels −1 and −2 are reached on the system board only, while the 'arbitrate/-grant' signal (ARB/-GNT) is in the arbitration state.

When the central arbitration control point receives a level −1 request (NMI, a system board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level −1 request and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following figures.

Bit	Function
7	Enable system microprocessor cycle
6	Arbitration mask
5	Enable extended arbitration (not supported)
4–0	Reserved

Figure 3-2. Arbitration Register (Hex 0090)—Write

Bit	Function
7	Enable system microprocessor cycle
6	Arbitration masked by NMI
5	Bus time-out
4	Reserved
3–0	Value of arbitration bus during previous grant state

Figure 3-3. Arbitration Register (Hex 0090)—Read

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 1 by POST.

Reading this bit as a 1 indicates that the system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Note: On 57 models that have a Type 3 system board (all 486SLC2 models) reading this bit as a 1 indicates that a bus timeout has occurred, and has masked arbitration. This bit will not be set in response to a memory parity error or channel check.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 enables extended arbitration. The minimum arbitration cycle is 300 nanoseconds; this bit extends that minimum cycle to 600 nanoseconds. This bit is set to 0 during POST.

Reading this bit as a 1 indicates that a bus time-out has occurred and resets bit 6 in this register to 0.

Bit 4 This bit is reserved and must be set to 0.

Bits 3–0 These bits are undefined for a write operation and must be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Bus Adapter

The Model 57 systems use a direct bus attachment board to provide five channel connectors:

- Four 16-bit Micro Channel connectors
- One 16-bit Micro Channel connector with an auxiliary video extension.

The adapters are installed horizontally into the direct bus attachment board.

Diskette Drive Connector

The diskette drive cable connects to the system board and provides three 2- by 17-pin connectors for attaching internal diskette drives. Each connector passes control and data signals between the diskette drive controller on the system board and the drives. It also provides the power to each drive.

The following figure shows the signal assignments and pin numbers for the diskette drive connectors.

Pin	Signal	Pin	Signal
1	Ground	2	Data rate select 1
3	+5 V dc	4	Drive type ID 1/Drive status 1
5	Ground	6	+12 V dc
7	Ground	8	-Index
9	Drive type ID 0/Drive status 0	10	Reserved
11	Ground	12	-Drive select
13	Ground	14	-Security Command
15	Ground	16	-Motor enable
17	Media type ID 1/Drive status 3	18	-Direction in
19	Ground	20	-Step
21	Ground	22	-Write data
23	Ground	24	-Write enable
25	Ground	26	-Track 0
27	Media type ID 0/Drive status 2	28	-Write protect
29	Ground	30	-Read data
31	Ground	32	-Head 1 select
33	Data rate select 0	34	-Diskette change

Figure 3-4. Diskette Drive Connector

System Board Memory Connectors

The Model 57 system board has three 72-pin connectors for single inline memory modules (memory modules).

The following figure shows the pin assignments for the 1- by 72-pin memory connectors. Refer to "Memory-Presence Detect Signals" on page 3-15 for decoding of the presence-detect signals.

Pin	Signal	Pin	Signal
1	Ground	37	Parity data 1
2	Data 0	38	Parity data 3
3	Data 16	39	Ground
4	Data 1	40	Column address strobe 0
5	Data 17	41	Column address strobe 2
6	Data 2	42	Column address strobe 3
7	Data 18	43	Column address strobe 1
8	Data 3	44	Row address strobe 0
9	Data 19	45	Row address strobe 1
10	+5 V dc	46	Block select 1
11	-Column address strobe parity	47	Write enable
12	Address 0	48	Reserved
13	Address 1	49	Data 8
14	Address 2	50	Data 24
15	Address 3	51	Data 9
16	Address 4	52	Data 25
17	Address 5	53	Data 10
18	Address 6	54	Data 26
19	Reserved	55	Data 11
20	Data 4	56	Data 27
21	Data 20	57	Data 12
22	Data 5	58	Data 28
23	Data 21	59	+5 V dc
24	Data 6	60	Data 29
25	Data 22	61	Data 13
26	Data 7	62	Data 30
27	Data 23	63	Data 14
28	Address 7	64	Data 31
29	Block select 0	65	Data 15
30	+5 V dc	66	Block select 2
31	Address 8	67	Presence detect 0
32	Address 9	68	Presence detect 1
33	Row address strobe 3	69	Presence detect 2
34	Row address strobe 2	70	Presence detect 3
35	Parity data 2	71	Block select 3
36	Parity data 0	72	Ground

Figure 3-5. System Board Memory Connectors

SCSI-Device Connector

The SCSI-device cable connects to the system board and provides three 2- by 25-pin connectors for attaching internal SCSI devices. The Model 57 system board has one 2- by 30-pin connector for attaching external SCSI devices.

The following figure shows the pin assignments for the 2- by 25-pin internal SCSI connector.

Pin	Signal	Pin	Signal
1	Ground	26	+Terminal power
2	Data 0	27	Ground
3	Ground	28	Ground
4	Data 1	29	Ground
5	Ground	30	Ground
6	Data 2	31	Ground
7	Ground	32	-Attention
8	Data 3	33	Ground
9	Ground	34	Ground
10	Data 4	35	Ground
11	Ground	36	-Busy
12	Data 5	37	Ground
13	Ground	38	-Acknowledge
14	Data 6	39	Ground
15	Ground	40	-Reset
16	Data 7	41	Ground
17	Ground	42	-Message
18	Data P	43	Ground
19	Ground	44	-Select
20	Ground	45	Ground
21	Ground	46	-Control/data
22	Ground	47	Ground
23	Ground	48	-Request
24	Ground	49	Ground
25	Not connected	50	-Input/output

Figure 3-6. SCSI Device Cable Internal Connector Pin Assignments

The following figure shows the pin assignments for the 2- by 30-pin external SCSI connector.

Pin	Signal	Pin	Signal
1	Ground	31	Ground
2	Data 0	32	-Attention
3	Ground	33	Ground
4	Data 1	34	Ground
5	Ground	35	Ground
6	Data 2	36	-Busy
7	Ground	37	Ground
8	Data 3	38	-Acknowledge
9	Ground	39	Ground
10	Data 4	40	-Reset
11	Ground	41	Ground
12	Data 5	42	-Message
13	Ground	43	Ground
14	Data 6	44	-Select
15	Ground	45	Ground
16	Data 7	46	-Control/data
17	Ground	47	Ground
18	Data P	48	-Request
19	Ground	49	Ground
20	Ground	50	-Input/output
21	Ground	51	Ground
22	Ground	52	Reserved
23	Ground	53	Reserved
24	Ground	54	Reserved
25	Not connected	55	Reserved
26	+Terminal power	56	Reserved
27	Ground	57	Reserved
28	Ground	58	Reserved
29	Ground	59	Reserved
30	Ground	60	Reserved

Figure 3-7. System Board SCSI Device External Connector

Memory

The Model 57 systems use the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- Real-time clock and CMOS RAM (RT/CMOS RAM)
- Nonvolatile random access memory (NVRAM)

ROM Subsystem

The ROM subsystem consists of 256KB of physical memory in two 128KB pages. Mapped ROM is active at power-on time and is assigned to the top of the first and last 1MB of address space (hex 0E0000–0FFFFF and hex FE0000–FFFFFF). After POST ensures that system memory is operating properly, the ROM code is copied to RAM at the same address space, and ROM is disabled.

Access to ROM or RAM at address space hex 0E0000–0FFFFF is controlled by the ROM enable bit in the Memory-Controller Configuration register. When ROM is enabled, it is not parity-checked, and operates with two 50-nanosecond wait states.

RAM Subsystem

The RAM subsystem on the system board starts at address hex 000000 of the address space. The RAM subsystem is 18 bits wide: 16 data bits and 2 parity bits. One parity bit is generated for each byte of data written. During a read operation, one parity bit is checked for each byte of data that is read by the device controlling the bus.

Three memory connectors are provided on the system board. Each connector can support 2MB, 4MB, or 8MB memory.

The system enables and disables memory in 1MB blocks. Each 1MB block must start on a 1MB boundary. Because 128KB of I/O ROM, 128KB of system board ROM, and 128KB of video memory are mapped within the first 1MB of address space, the first physical 1MB of RAM cannot be mapped to contiguous addresses and is split at the 640KB boundary, creating a 384KB overflow. The high 128KB of the overflow is mapped to the system board ROM address space; the remaining 256KB, called the *split memory block*, is either reserved for system use or mapped to the first available address following the last full 1MB of activated system board memory. Split-memory-block remapping and disabling are controlled by the Memory-Controller Configuration register. The presence of the split memory block in the memory address space, might be affected by nonsystem memory.

Memory Interleaving Option

The system board memory controller supports interleaving for specific memory configurations. The following figure lists the interleaving configurations for the three memory connectors for Type 1 and Type 2 system boards only. The Type 3 system board (57 486SLC2 models) does not support memory interleaving.

Memory Connector 1	Memory Connector 2	Memory Connector 3
2MB	Empty	Empty
2MB	2MB	Empty
2MB	2MB	2MB
4MB	4MB	Empty
4MB	4MB	4MB

Figure 3-8. Memory Interleaving Configurations

Memory-Presence Detect Signals

The memory-presence detect signals are used by the system to determine the size and speed of memory on the memory module. The pins are either not connected (1) or connected to ground (0).

A set of 4 bits shows the state of all memory-presence detect signals for a specific memory connector; the bit is set to 0 when the signal is connected to ground. The following figure shows the information indicated by these bits as well as the bank size of the memory module. All combinations that are not shown are reserved.

Presence Detect 3 2 1 0	Single Inline Memory Module Definition	Bank Size
1 1 0 0	2MB 70-ns memory	1MB
0 1 0 0	4MB 70-ns memory	4MB
1 0 1 1	8MB 70-ns memory	4MB

Figure 3-9. Presence-Detect Bits

System Memory Map

Memory is mapped by Memory Controller registers.

The first 640KB of system board RAM is mapped starting at address hex 000000. A 256-byte area and a 1KB area of this RAM are reserved as BIOS data areas. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for details.

The following figure shows the memory map for a properly functioning system. Memory can be mapped differently if POST detects an error in system board memory or RT/CMOS RAM. In the following figure, the variable *x* represents the number of 1MB blocks of system board memory starting at or above the hex 100000 boundary.

Hex Address Range	Function
000000 to 09FFFF†	640KB system board RAM
0A0000 to 0BFFFF	128KB video RAM
0C0000 to 0DFFFF	Feature adapter ROM
0E0000 to 0FFFFF†	128K system board ROM mapped to RAM
100000 to (100000 + xMB) − 1†	xMB system board RAM
(100000 + xMB) to (100000 + xMB + 256KB) − 1†	256KB system board RAM (split memory block)
FE0000 to FFFFFF	128KB system board ROM (same as 0E0000 to 0FFFFF)

† These address ranges are cacheable on Type 2 and Type 3 systems.

Figure 3-10. System Memory Map

Memory Controller Registers

The memory controller, which is located on the system board, has several internal registers that are used to control the memory installed in the memory connectors on the system board. The memory controller manages this memory in banks of 1MB or 4MB. Memory is enabled in 1MB increments.

Memory-parity error information is provided through the following internal registers:

- Memory-Fault Row Address Strobe (RAS) Capture register
- Two Memory-Controller Fault Address registers.

Memory-Fault RAS Capture Register (I/O Port Hex 00E2)

Bits in this register are set by a system board parity check. The RAS signal that is active at the time of the parity check is held until the system microprocessor reads this register.

Bit	Function
7, 6	Reserved
5	RAS5
4	RAS4
3	RAS3
2	RAS2
1	RAS1
0	RAS0

Figure 3-11. Memory-Fault RAS Capture Register (I/O Port Hex 00E2)

Bits 7, 6 These bits are reserved.

Bits 5–0 The system board memory connectors are wired with fixed RAS signals as follows:

Memory Connector	RAS Signals
Memory connector 1	RAS0, RAS1
Memory connector 2	RAS2, RAS3
Memory connector 3	RAS4, RAS5

Figure 3-12. Fixed RAS Signals

Memory-Controller-Fault Address Registers (I/O Ports Hex 00E4 and Hex 00E5)

These registers capture the high-order memory address when a system board parity check occurs. The address remains in the registers until the registers are read by the system microprocessor.

The following figure shows the failing memory-address space address bits for the Memory-Controller-Fault Address register (I/O Port Hex 00E4).

I/O Port Hex 00E4	Failing-Address Bit
7	15
6	14
5	13
4	12
3	11
2	10
1	09
0	08

Figure 3-13. Memory-Controller-Fault Address Register (I/O Port Hex 00E4)

The following figure shows the failing memory-address space address bits for the Memory-Controller-Fault Address register (I/O Port Hex 00E5).

I/O Port Hex 00E5	Failing-Address Bit
7	23
6	22
5	21
4	20
3	19
2	18
1	17
0	16

Figure 3-14. Memory-Controller-Fault Address Registers (I/O Port Hex 00E5)

RT/CMOS RAM

The RT/CMOS RAM (real-time clock/complementary metal-oxide semiconductor RAM) module contains the real-time clock and 64 bytes of CMOS RAM. The clock uses 14 bytes of this memory, and the rest is allocated to configuration and system status information. A battery, which is located on the bus adapter, keeps the RT/CMOS RAM active when the power supply is off.

The system board has an additional 8KB CMOS RAM extension that is used to store configuration and other system information. This RAM extension is kept active by the battery on the bus adapter.

The following figure shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000–00D	Real-Time Clock bytes
00E	Diagnostic Status byte
00F	Shutdown Status byte
010	Diskette Drive Type byte
011	Fixed Disk Drive Type byte
012	Reserved
013	Reserved
014	Equipment byte
015, 016	Low and High Base-Memory bytes
017, 018	Low and High Expansion-Memory bytes
019–031	Reserved
032, 033	Configuration CRC bytes
034	Reserved
035, 036	Low and high usable memory above 1MB
037	Date-Century byte
038–03F	Reserved

Figure 3-15. RT/CMOS RAM Address Map

RT/CMOS Address and NMI Mask Register (Hex 0070)

This register is used with the RT/CMOS Data register (hex 0071) to read from and write to the RT/CMOS RAM bytes.

Warning: The operation following a write operation to this register should access the RT/CMOS Data register; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Bit	Function
7	NMI mask
6	Reserved
5–0	RT/CMOS RAM address

Figure 3-16. RT/CMOS Address and NMI Mask Register (Hex 0070)

Bit 7 When this write-only bit is set to 1, the NMI is masked (disabled). This bit is set to 1 by a power-on reset.

Bit 6 This bit is reserved.

Bits 5–0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This register is used with the RT/CMOS Address and NMI Mask register to read from and write to the RT/CMOS RAM bytes.

Bit	Function
7–0	RT/CMOS data

Figure 3-17. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts must be masked to prevent other interrupt routines from changing the CMOS Address register before data is read from or written to.

Warning: The operation following a write operation to hex 0070 must access hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Writing to RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Write the data to address hex 0071.
3. Write the address, hex 0F, to the RT/CMOS and NMI Mask register; this leaves hex 0070 pointing to the Shutdown Status byte (hex 0F).
4. Read address hex 0071 to restore the RT/CMOS (see the warning above).

Reading from RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Read the data from address hex 0071.
3. Write the address, hex 0F, to the RT/CMOS and NMI Mask register; this leaves hex 0070 pointing to the Shutdown Status byte (hex 0F).
4. Read address hex 0071 to restore the RT/CMOS.

Real-Time Clock Bytes (Hex 000 – 00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following figure.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second alarm	1
002	Minutes	2
003	Minute alarm	3
004	Hours	4
005	Hour alarm	5
006	Day of week	6
007	Date of month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-18. Real-Time Clock Bytes (Hex 000 – 00D)

Note: The system initializes Status Registers A and B when the time and date are set. Interrupt 1AH is the BIOS interface to read and set the time and date, and it initializes the registers in the same way as the system does.

Status Register A (Hex 00A)

Bit	Function
7	Update in progress
6 – 4	22-stage divider
3 – 0	Rate-selection bits

Figure 3-19. Status Register A (Hex 00A)

Bit 7 When this bit is set to 1, this bit indicates that the time-update cycle is in progress. When this bit is set to 0, it indicates that the current date and time can be read.

Bits 6 – 4 These bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768-kHz time base. This is the only value supported by the system for proper timekeeping.

Bits 3 – 0 These bits allow the selection of a divider-output frequency. The system initializes the rate-selection bits to binary 0110, which selects a 1.024-kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Enable periodic-interrupt
5	Enable alarm-interrupt
4	Enable update-ended interrupt
3	Enable square wave
2	Date mode
1	24-hour mode
0	Enable daylight saving time mode

Figure 3-20. Status Register B (Hex 00B)

Bit 7 When this bit is set to 0, it updates the cycle by advancing the counts at a rate of one per second. When this bit is set to 1, it immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This bit is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status register A. When this bit is set to 1, it enables the interrupt. The system initializes this bit to 0.

Bit 5 When this bit is set to 1, it enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When this bit is set to 1, it enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When this bit is set to 1, it enables the square-wave frequency as set by the rate-selection bits in Status register A. The system initializes this bit to 0.

Bit 2 This bit indicates whether the binary-coded-decimal (BCD) or binary format is used for time-and-date calendar updates. When this bit is set to 1, it indicates the binary format. The system initializes this bit to 0.

Bit 1 This bit indicates if the hours byte is in 12-hour or 24-hour mode. When this bit is set to 1, it indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When this bit is set to 1, it enables the daylight-saving-time mode. When this bit is set to 0, it disables the modes and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt-request flag
6	Periodic-interrupt flag
5	Alarm-interrupt flag
4	Update-ended interrupt flag
3–0	Reserved

Figure 3-21. Status Register C (Hex 00C)

Note: Interrupts are enabled by bits 6, 5, and 4 in Status register B.

Bit 7 When this bit is set to 1, it indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When this bit is set to 1, it indicates that a periodic interrupt occurred.

Bit 5 When this bit is set to 1, it indicates that an alarm interrupt occurred.

Bit 4 When this bit is set to 1, it indicates that an update-ended interrupt occurred.

Bits 3–0 These bits are reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6–0	Reserved

Figure 3-22. Status Register D (Hex 00D)

Bit 7 This read-only bit monitors the internal battery. When this bit is set to 1, it indicates that the real-time clock has power. When this bit is set to 0, it indicates that the real-time clock has lost power.

Bits 6–0 These bits are reserved.

CMOS RAM Configuration

The following shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-time clock power
6	Configuration record and checksum status
5	Incorrect configuration
4	Memory-size mismatch
3	Fixed disk controller/drive C initialization status
2	Time status indicator
1	Adapter configuration miscompare
0	Adapter ID time-out

Figure 3-23. Diagnostic Status Byte (Hex 00E)

Bit 7 When this bit is set to 1, it indicates that the real-time clock lost power.

Bit 6 When this bit is set to 1, it indicates that a checksum is incorrect.

Bit 5 When this bit is set to 1, it indicates that the configuration information is incorrect.

Bit 4 When this bit is set to 1, it indicates that the memory size does not match the configuration information.

Bit 3 When this bit is set to 1, it indicates that the controller or fixed disk drive failed initialization.

Bit 2 When this bit is set to 1, it indicates that the time and date are invalid.

Bit 1 When this bit is set to 1, it indicates that the adapters do not match the configuration information.

Bit 0 When this bit is set to 1, it indicates that a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is used by POST and BIOS.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7–4	First diskette drive type
3–0	Second diskette drive type

Figure 3-24. Diskette Drive Type Byte (Hex 010)

Bits 7–4 These bits indicate the first diskette drive type, as shown in the following figure.

Bits 7 6 5 4	Function
0 0 0 0	No drive present
0 0 0 1	5.25-inch, 360KB diskette drive
0 0 1 0	5.25-inch, 1.2MB diskette drive
0 0 1 1	3.5-inch, 720KB diskette drive
0 1 0 0	3.5-inch, 1.44MB diskette drive
0 1 1 0	3.5-inch, 2.88MB diskette drive

Note: All combinations that are not shown are reserved.

Figure 3-25. Diskette Drive Type Byte (Bits 7–4)

Bits 3–0 These bits indicate the second diskette drive type, as shown in the following figure.

Bits 3 2 1 0	Function
0 0 0 0	No drive present
0 0 0 1	5.25-inch, 360KB diskette drive
0 0 1 0	5.25-inch, 1.2MB diskette drive
0 0 1 1	3.5-inch, 720KB diskette drive
0 1 0 0	3.5-inch, 1.44MB diskette drive
0 1 1 0	3.5-inch, 2.88MB diskette drive

Note: All combinations that are not shown are reserved.

Figure 3-26. Diskette Drive Type Byte (Bits 3–0)

Fixed Disk Drive Type Byte (Hex 011): This byte defines the type of fixed disk drive installed. Hex 000 indicates that a fixed disk drive is *not* installed. This byte is not used for SCSI fixed disk drives.

Note: For more information about fixed disk drives, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Reserved Bytes (Hex 012, 013): These bytes are reserved.

Equipment Byte (Hex 014): This byte defines the basic equipment in the system for the power-on diagnostic tests.

Bit	Function
7, 6	Number of diskette drives other than physical drive 0
5, 4	Display operating mode
3, 2	Reserved
1	Math coprocessor presence
0	Diskette drive 0 presence

Figure 3-27. Equipment Byte (Hex 014)

Bits 7, 6 These bits indicate the number of diskette drives other than drive 0 installed, as shown in the following figure.

Bits 7 6	Number of Diskette Drives
0 0	No other drive
0 1	One other drive
1 0	Two other drives
1 1	Reserved

Figure 3-28. Installed Diskette Drive Bits

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port, as shown in the following figure.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-column mode
1 0	80-column mode
1 1	Monochrome mode

Figure 3-29. Display Operating-Mode Bits

Bits 3, 2 These bits are reserved.

Bit 1 When this bit is set to 1, it indicates that a math coprocessor is installed.

Bit 0 When this bit is set to 1, it indicates that physical diskette drive 0 is installed.

Low and High Base-Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The hexadecimal value in these bytes represents the number of 1KB blocks of *base memory*. For example, hex 0280 indicates 640KB. The low byte is hex 015; the high byte is hex 016.

Low and High Expansion-Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The hexadecimal value in these bytes represent the number of 1KB blocks of *expansion memory*. For example, hex 0800 indicates 2048KB. The low byte is hex 017; the high byte is hex 018.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check (CRC) data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 033; the high byte is hex 032.

Reserved Byte (Hex 034): This byte is reserved.

Low and High Usable Memory Bytes (Hex 035 and 036): These bytes define the total amount of contiguous memory from 1MB to 16MB.

The hexadecimal value in these bytes represent the number of 1KB blocks of usable memory. For example, hex 0800 indicates 2408KB. The low byte is hex 035; the high byte is hex 036.

Date Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 – 03F): These bytes are reserved.

NVRAM

The NVRAM contains, among other things, the system configuration information. The entire RAM is reserved for system use.

Vital Product Data

On 57 models with a Type 3 system board (486SLC2 models), the system board has a unique vital product data (VPD) code. This code is stored in NVRAM and contains various system identification information. Interrupt 15H, function code (AH) = D2H, returns the system identification information. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for more information.

Miscellaneous System Functions and Ports

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system watchdog time-out has occurred. The NMI (except cache parity error) stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. (On the 57 486SLC2 and the Ultimedia 57 486SLC2 models, only the channel time-out NMI stops arbitration on the bus.) This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts, and the IRET instruction restores the interrupt flag to the state it was in before the interrupt. A system reset causes a reset of the NMI.

The NMI requests from system board parity and channel check are subject to mask control with the NMI mask bit in the RT/CMOS Address register. The watchdog timer, system channel time-out, and cache parity error are not masked by this bit. See "RT/CMOS Address and NMI Mask Register (Hex 0070)" on page 3-19. The power-on default of the NMI mask is 1 (NMI disabled). Before the NMI is enabled after a power-on reset, the parity-check and channel-check states are initialized by POST.

Warning: The operation following a write operation to this register must access the RT/CMOS Data register; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the write and read functions of this port are shown in the following figures.

Bit	Function
7	Reset timer 0 output latch (IRQ0)
6–4	Reserved
3	Enable channel check
2	Enable parity check
1	Enable speaker data
0	Timer 2 gate to speaker

Figure 3-30. System Control Port B (Hex 0061)—Write

Bit	Function
7	Parity check
6	Channel check
5	Timer 2 output
4	Toggles with each refresh request
3	Enable channel check
2	Enable parity check
1	Enable speaker data
0	Timer 2 gate to speaker

Figure 3-31. System Control Port B (Hex 0061)—Read

Bit 7 When this bit is set to 1 during a write operation, IRQ0 is reset. When read as a 1, this bit indicates that a parity check has occurred.

Bit 6 When read as a 1, this bit indicates that a channel check has occurred.

Bit 5 When read, this bit indicates the condition of the timer/counter 2 'output' signal.

Bit 4 When read, this bit toggles for each refresh request.

Bit 3 When this bit is set to 0, it enables a channel check. This bit is set to 1 during a power-on reset.

Bit 2 When this bit is set to 0, it enables a parity check. This bit is set to 1 during a power-on reset.

Bit 1 When this bit is set to 1, it enables speaker data.

Bit 0 When this bit is set to 1, it enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7–5	Reserved
4	Watchdog timer status
3	Security lock latch
2	Reserved
1	Alternate gate A20
0	Alternate hot reset

Figure 3-32. System Control Port A (Hex 0092)

Bits 7–5 These bits are reserved.

Bit 4 This read-only bit indicates the watchdog-timer status. When this bit is set to 1, a watchdog time-out has occurred. For more information about the watchdog timer, refer to the System Timers section of the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces.*

Bit 3 This bit provides the security lock for the secured area of RT/CMOS. When this bit is set to 1, the 8-byte, power-on password is electronically locked. After this bit is set by POST, it can be cleared only by turning the system off.

Bit 2 This bit is reserved.

Bit 1 This bit is ORed with bit 1 in the Keyboard Output port to enable the 'address 20' signal (A20). When both bits are set to 0, A20 is disabled and set to 0. This bit is set to 0 during POST. See the Keyboard and Auxiliary Device Controller section of the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces.*

Bit 0 This bit provides an alternative method of resetting the system microprocessor. This alternative method supports operating systems that require faster operation than was provided on the IBM Personal Computer AT®. Resetting

the system microprocessor switches the microprocessor from protected mode to real-address mode. The alternative reset takes 13.4 microseconds.

This bit is set to 0 by either a system reset or a write operation. When a write operation changes this bit from 0 to 1, the alternative reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is set to 0, POST assumes that the system was just powered-on. If the bit is set to 1, POST assumes that a switch from the protected mode to the real mode has taken place.

When bit 0 is used to reset the system microprocessor to the real mode, the following procedure *must* be used:

1. Disable all maskable and nonmaskable interrupts.
2. Reset the system microprocessor by writing a 1 to bit 0.
3. Issue a Halt instruction to the system microprocessor.
4. Reenable all maskable and nonmaskable interrupts.

If this procedure is not followed, the results will be unpredictable.

Note: Whenever possible, BIOS or ABIOS should be used as an interface to reset the system microprocessor to the real mode. See *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for more information about BIOS.

Power-On Password

RT/CMOS RAM has 8 bytes reserved for the power-on password and its check character. The 8 bytes are initialized to hex 00. The microprocessor can access these bytes only during power-on self-test (POST). After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by a program. During power-on password installation, the password (1 to 7 characters), is stored in the security space.

Installing the password is a function of a program on the Reference Diskette. The power-on password does not appear on the screen

---

* Trademark of the IBM Corporation.

when it is installed, changed, or removed. After the power-on password has been installed, it can be changed or removed only during POST.

Privileged-Access Password

The privileged-access password (on 57 486SLC2 and Ultimedia M57 486SLC2 models only) is also a function of the Reference Diskette. This password, when set and entered correctly, will give the owner access to the entire system, overriding the power-on password. It is stored in electrically-erasable programmable read-only memory (EEPROM), and is only accessible by the processor during power-on self-test (POST) and during system configuration. Afterwards, the locations are locked from further access.

Warning: If the owner forgets the privileged-access password after it has been set, the system board must be replaced to make the system operational.

Keyboard Password

The Model 57 systems also can have a keyboard password. See the Keyboard and Auxiliary Device Controller section of the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* for more information.

Cover Lock and Tamper-Evident Switch

All 57 486SLC2 models have an electro-mechanical cover lock. In the locked position, it mechanically prevents the cover from being removed. If the covers are forced open, the tamper-evident cover switch detects the intrusion. The next time the system is powered-on, POST displays a message informing the user that the system covers have been tampered with.

Note: When the cover is removed, power is removed from the system. If you want to run the system with the cover off, you must move the security switch to the "up" or "on" position.

Selectable Boot Sequence

The selectable boot sequence allows the user to specify the order in which 1 to 4 bootable devices are searched when looking for the boot startup record of an operating system. Diskette drives, fixed disk drives, and remote initial program load (RIPL) can be part of the search sequence. Changing the sequence for selectable boot affects the drive-letter assignment each time the system is reset, either as a power-on reset or a soft reset.

The user selects the boot sequence by using the Select startup sequence menu on the System Reference Diskette, and selecting from a list of possible devices. After the sequence is selected, it is stored in nonvolatile RAM (NVRAM). On the 57 486SLC2 and the Ultimedia 57 486SLC2, the startup sequence is stored in electrically-erasable programmable read-only memory (EEPROM). When the system is booted, it searches for a device that contains a bootable record, using the specified sequence.

After the operating system is booted, the drive lettering is determined by the sequence and by which device contained the bootable source.

Note: Selectable boot affects adapters that use initialization programs. See the Setup section of *IBM Personal System/2 Hardware Interface Technical Reference—Architectures* for more details.

Hardware Compatibility

The Model 57 systems maintain many of the interfaces used by previous PS/2 products. In most cases, command and status organization of these interfaces is maintained.

The functional interfaces for the Model 57 systems are compatible with the following:

- The Intel 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller-address/transfer counters, page registers and status fields only. The Command and Request registers are not supported. The Rotate and Mask functions are not supported. The Mode register is partially supported.
- The NS16450 serial port.

- The Intel 8088, 8086, 80286, and 80386 microprocessors.
- The Intel 8272 diskette drive controller.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The keyboard interface at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in DOS mode.
- Generally compatible with the Intel 80387, 80287, and 8087 math coprocessors.

Error Codes

POST returns a message in the form of a multiple-character code to indicate the type of test that failed. Two formats are used for these error messages:

- A 12-character code for all errors *that are* related to SCSI devices:
  - The first four characters identify the device type.
  - The next eight characters identify specifics of the error.
- An 8-character error code for all errors *that are not* related to SCSI devices.

The 8-character error code consists of two 4-character elements; the major error code and the minor error code. The following figure lists the failure and the associated error code.

** Trademark of Motorola, Incorporated.

Major Code	Minor Code	Description
0001		System bus error - system board
	0100	Unexpected interrupt
	0200	Timer failure
	0300	Timer interrupt failure
	0400	Protected mode failure
	0500	Last keyboard command not accepted
	0600	Converting logic test
	0700	NMI test failed
	0800	Timer bus-test failed
	0900	Low MB chip select test failed
	10xx	System board memory parity error
	11xx	I/O channel-check error
	1200	Watchdog time-out
	1300	DMA arbitration time-out
	1400	Channel feature card ROM checksum error
	1500	ROM checksum error or DMA error
	1600	System board port read/write failure
	1800	System board parity
	2000	Microprocessor test error
	6000	System board ID not recognized
	6100	Dead battery
	6300	Clock not updating
	6400	Memory-configuration error
	6500	Adapter ID mismatch
	6600	Adapter-busy error
	6700	Clock not updating
	6900	System board and processor card configuration mismatch
	7100	Rolling-bit-test failure on CMOS shutdown address byte
	7200	Rolling-bit-test failure on NVRAM diagnostic byte
	7300	Bad CMOS/NVRAM checksum
	7400	Bad configuration
	7500	Bad EEPROM
	7600	Tamper evident
	7700	Bad EEPROM
	7800	Bad EEPROM
	7900	NVRAM error log full
	8100	Unsupported configurations
	8200	Privileged-access switch (JMP2) is not in the write-enable position
	8300	Privileged-access password required
	8400	Bad power-on password
	8500	Bad startup sequence
	8600	Password protection hardware
	8700	Serial number error
	8800	Bad EEPROM checksum
	8900	Excessive incorrect password attempts

Figure 3-33 (Part 1 of 2). POST Error Messages

Major Code	Minor Code	Description
0002		Memory errors
	0xxx	Memory error
	1xxx	Unrecoverable error in first 1MB
	2100	ROM-to-RAM remapping error
	25xx	Unsupported memory-type installed
0003		Keyboard
	0100	Keyboard error
	0200	Keyboard locked
	0300	Keyboard-to-system board interface error
	0400	Keyboard clock high
	0500	No keyboard +5 V dc
0006		Diskette
	0100	Diskette drive or controller error
	0200	Diskette IPL boot record not valid
	0400	Non-media sense
	0500	Diskette drive locked
0011	0100	Serial port A error
0012	0100	Serial port B error
0017		Fixed disk error
	8000	Fixed disk 0 failed
	8100	Fixed disk 1 failed
	8200	Disk-controller error
	9000	Fixed disk 0 error
	9100	Fixed disk 1 error
0024	0100	System board video error
0037	xxxx	System board SCSI controller error
0086		Mouse
	0100	System-bus error - keyboard/pointing device interface
	0200	Pointing-device error
	0300	Pointing-device or system-bus error
0096	xxxx	SCSI adapter with cache error
0112	xxxx	SCSI adapter error
0129	0200	Cache error
0208 to 0241	xxxx	SCSI device test failure
1999		Special instruction codes
	00xx	Initial microcode load (IML) error
	03xx	No bootable device
	04xx	IML-to-system mismatch

Figure 3-33 (Part 2 of 2). POST Error Messages

Appendix. 386SLC Instruction Cycle Times

The following are the instruction timings for the IBM 386SLC. All cache-off timings are considered cache-miss situations. Any instructions not listed are the same as for the Intel 80386SX.

Mnemonic	16-Bit Real Mode Cache-Miss Cycles	16-Bit Real Mode Cache-Hit Cycles	16-Bit Protected Mode Cache-Miss Cycles	16-Bit Protected Mode Cache-Hit Cycles
adc mb,ib	7	5	7	5
adc mb,rb	7	5	7	5
adc mw,iw	7	5	7	5
adc mw,rw	7	5	7	5
adc rb,ib	2	2	2	2
adc rb,mb	6	4	6	4
adc rb,rb	2	2	2	2
adc rw,iw	2	2	2	2
adc rw,mw	6	4	6	4
adc rw,rw	2	2	2	2
add mb,ib	7	5	7	5
add mb,rb	7	5	7	5
add mw,iw	7	5	7	5
add mw,rw	7	5	7	5
add rb,ib	2	2	2	2
add rb,mb	5	3	5	3
add rb,rb	2	2	2	2
add rw,iw	2	2	2	2
add rw,mw	5	3	5	3
add rw,rw	2	2	2	2
and mb,ib	7	5	7	5
and mb,rb	7	5	7	5
and mw,iw	7	5	7	5
and mw,rw	7	5	7	5
and rb,ib	2	2	2	2
and rb,mb	5	3	5	3
and rb,rb	2	2	2	2
and rw,iw	2	2	2	2
and rw,mw	5	3	5	3
and rw,rw	2	2	2	2
bound rdw,mqw	15	10	15	10
bound rw,mdw	11	10	11	10
bsf rdw,mdw	40	37	40	37
bsf rdw,rdw	35	35	35	35
bsf rw,mw	26	25	26	25
bsf rw,rw	23	23	23	23

Figure A-1 (Part 1 of 8). Instruction Cycle Times

© Copyright IBM Corp. 1991, 1992

Mnemonic	16-Bit Real Mode Cache-Miss Cycles	16-Bit Real Mode Cache-Hit Cycles	16-Bit Protected Mode Cache-Miss Cycles	16-Bit Protected Mode Cache-Hit Cycles
bsr rdw,mdw	38	35	38	35
bsr rdw,rdw	33	33	33	33
bsr rw,mw	24	23	24	23
bsr rw,rw	21	21	21	21
bt mdw,ib	8	5	8	5
bt mdw,rdw	14	11	14	11
bt mw,ib	6	5	6	5
bt mw,rw	12	11	12	11
bt rdw,ib	3	3	3	3
bt rdw,rdw	3	3	3	3
bt rw,ib	3	3	3	3
bt rw,rw	3	3	3	3
btc mdw,ib	9	8	9	8
btc mdw,rdw	15	13	15	13
btc mw,ib	8	8	8	8
btc mw,rw	13	13	13	13
btc rdw,ib	6	6	6	6
btc rdw,rdw	6	6	6	6
btc rw,ib	6	6	6	6
btc rw,rw	6	6	6	6
btr mdw,ib	9	8	9	8
btr mdw,rdw	15	13	15	13
btr mw,ib	8	8	8	8
btr mw,rw	13	13	13	13
btr rdw,ib	6	6	6	6
btr rdw,rdw	6	6	6	6
btr rw,ib	6	6	6	6
btr rw,rw	6	6	6	6
bts mdw,ib	9	8	9	8
bts mdw,rdw	15	13	15	13
bts mw,ib	8	8	8	8
bts mw,rw	13	13	13	13
bts rdw,ib	6	6	6	6
bts rdw,rdw	6	6	6	6
bts rw,ib	6	6	6	6
bts rw,rw	6	6	6	6
call cs:ip	20	14	32	19
call disp	9	5	9	5
call far m	27	17	39	22
call m	14	10	14	10
call rw	11	7	11	7
cli	5	5	5	5
cmc	2	2	2	2

Figure A-1 (Part 2 of 8). Instruction Cycle Times

Mnemonic	16-Bit Real Mode Cache-Miss Cycles	16-Bit Real Mode Cache-Hit Cycles	16-Bit Protected Mode Cache-Miss Cycles	16-Bit Protected Mode Cache-Hit Cycles
cmp mb,ib	5	3	5	3
cmp mb,rb	5	3	5	3
cmp mw,iw	5	3	5	3
cmp mw,rw	5	3	5	3
cmp rb,ib	2	2	2	2
cmp rb,mb	6	4	6	4
cmp rb,rb	2	2	2	2
cmp rw,iw	2	2	2	2
cmp rw,mw	6	4	6	4
cmp rw,rw	2	2	2	2
cmpsb	12	10	12	10
cmpsw	12	10	12	10
cmpsd	16	10	16	10
dec mb	6	4	6	4
dec mw	6	4	6	4
dec rb	2	2	2	2
dec rw	2	2	2	2
enter	7	7	7	7
imul mb	6	4	6	4
imul mw	6	4	6	4
imul rb	2	2	2	2
imul rw	2	2	2	2
imul rw,rw,iw	19	19	19	19
in rb,dx	14	14	7	7
in rb,ib	12	12	6	6
in rw,dx	14	14	7	7
in rw,ib	12	12	6	6
inc mb	6	4	6	4
inc mw	6	4	6	4
inc rb	2	2	2	2
inc rw	2	2	2	2
int ib	43	35	76	64
iret	31	26	42	30
jcond not taken	3	3	3	3
jcond taken	9	5	9	5
jcxz not taken	3	3	3	3
jcxz taken	9	5	9	5
jmp cs:ip	16	12	27	16
jmp disp	9	5	9	5
jmp far m	23	15	34	19
jmp m	13	8	13	8
jmp rw	10	6	10	6
lds rw,mw	7	6	23	12

Figure A-1 (Part 3 of 8). Instruction Cycle Times

Mnemonic	16-Bit Real Mode Cache-Miss Cycles	16-Bit Real Mode Cache-Hit Cycles	16-Bit Protected Mode Cache-Miss Cycles	16-Bit Protected Mode Cache-Hit Cycles
leave	5	4	5	4
les rw,mw	7	6	23	12
lodsb	5	5	5	5
lodsd	7	5	7	5
lodsw	5	5	5	5
loop not taken	11	9	11	9
loop taken	9	5	9	5
loopc not taken	14	12	14	12
loopc taken	12	8	12	8
mov m,s	2	2	2	2
mov mb,ib	2	2	2	2
mov mb,rb	2	2	2	2
mov mw,iw	2	2	2	2
mov mw,rw	2	2	2	2
mov rb,ib	2	2	2	2
mov rb,mb	4	2	4	2
mov rb,rb	2	2	2	2
mov rw,iw	2	2	2	2
mov rw,mw	4	2	4	2
mov rw,rw	2	2	2	2
mov rw,s	2	2	2	2
mov s,m	5	4	18	9
mov s,rw	2	2	15	8
movsb	9	8	9	8
movsd	11	8	11	8
movsw	9	8	9	8
movsx rdw,mb	6	5	6	5
movsx rdw,mw	6	5	6	5
movsx rw,mb	6	5	6	5
movzx rdw,mb	6	5	6	5
movzx rdw,mw	6	5	6	5
movzx rw,mb	6	5	6	5
mul mb	16	15	16	15
mul mw	16	15	16	15
mul rb	13	13	13	13
mul rw	13	13	13	13
neg mb	6	4	6	4
neg mw	6	4	6	4
neg rb	2	2	2	2
neg rw	2	2	2	2
not mb	6	4	6	4
not mw	6	4	6	4
not rb	2	2	2	2
not rw	2	2	2	2

Figure A-1 (Part 4 of 8). Instruction Cycle Times

Mnemonic	16-Bit Real Mode Cache-Miss Cycles	16-Bit Real Mode Cache-Hit Cycles	16-Bit Protected Mode Cache-Miss Cycles	16-Bit Protected Mode Cache-Hit Cycles
or mb,ib	7	5	7	5
or mb,rb	7	5	7	5
or mw,iw	7	5	7	5
or mw,rw	7	5	7	5
or rb,ib	2	2	2	2
or rb,mb	5	3	5	3
or rb,rb	2	2	2	2
or rw,iw	2	2	2	2
or rw,mw	5	3	5	3
or rw,rw	2	2	2	2
out dx,rb	12	12	6	6
out dx,rw	12	12	6	6
out ib,rb	11	11	5	5
out	11	11	5	5
pop m	6	5	6	5
pop rw	4	2	4	2
pop s	5	4	18	9
popa	25	24	25	24
popad	33	24	66	65
popf	8	7	6	5
push m	6	5	6	5
push rw	2	2	2	2
push s	2	2	2	2
push iw	2	2	2	2
pusha	24	24	24	24
pushad	32	25	66	66
pushf	7	7	5	5
rep:cmpsb	10+4*n*†	9+2*n*	10+4*n*	9+2*n*
rep:cmpsw	10+4*n*	9+2*n*	10+4*n*	9+2*n*
rep:cmpsd	10+8*n*	9+2*n*	10+8*n*	9+2*n*
rep:lodsb	5+6*n*	5+6*n*	5+6*n*	5+6*n*
rep:lodsd	5+8*n*	5+6*n*	5+8*n*	5+6*n*
rep:lodsw	5+6*n*	5+6*n*	5+6*n*	5+6*n*
rep:movsb	8+5*n*	8+2*n*	8+5*n*	8+2*n*
rep:movsw	8+5*n*	8+2*n*	8+5*n*	8+2*n*
rep:movsd	8+8*n*	8+2*n*	8+8*n*	8+2*n*
rep:scasb	8+4*n*	8+2*n*	8+4*n*	8+2*n*
rep:scasw	8+4*n*	8+2*n*	8+4*n*	8+2*n*
rep:scasd	8+6*n*	8+2*n*	8+6*n*	8+2*n*

† *n* represents the number of additional cycles.

Figure A-1 (Part 5 of 8). Instruction Cycle Times

Mnemonic	16-Bit Real Mode Cache-Miss Cycles	16-Bit Real Mode Cache-Hit Cycles	16-Bit Protected Mode Cache-Miss Cycles	16-Bit Protected Mode Cache-Hit Cycles
rep:stosb	5+2*n*	5+2*n*	5+2*n*	5+2*n*
rep:stosw	5+2*n*	5+2*n*	5+2*n*	5+2*n*
rep:stosd	5+4*n*	5+2*n*	5+4*n*	5+2*n*
ret	11	7	11	7
ret iw	11	7	11	7
retf	21	13	33	19
retf iw	21	13	33	19
rol mb,cl	7	6	7	6
rol mb,ib	7	6	7	6
rol mw,cl	7	6	7	6
rol mw,ib	7	6	7	6
rol rb,cl	3	3	3	3
rol rb,ib	3	3	3	3
rol rw,cl	3	3	3	3
rol rw,ib	3	3	3	3
ror mb,cl	7	6	7	6
ror mb,ib	7	6	7	6
ror mw,cl	7	6	7	6
ror mw,ib	7	6	7	6
ror rb,cl	3	3	3	3
ror rb,ib	3	3	3	3
ror rw,cl	3	3	3	3
ror rw,ib	3	3	3	3
sahf	3	3	3	3
sal mb,cl	7	6	7	6
sal mb,ib	7	6	7	6
sal mw,cl	7	6	7	6
sal mw,ib	7	6	7	6
sal rb,cl	3	3	3	3
sal rb,ib	3	3	3	3
sal rw,cl	3	3	3	3
sal rw,ib	3	3	3	3
sar mb,cl	7	6	7	6
sar mb,ib	7	6	7	6
sar mw,cl	7	6	7	6
sar mw,ib	7	6	7	6
sar rb,cl	3	3	3	3
sar rb,ib	3	3	3	3
sar rw,cl	3	3	3	3
sar rw,ib	3	3	3	3

Figure A-1 (Part 6 of 8). Instruction Cycle Times

Mnemonic	16-Bit Real Mode Cache-Miss Cycles	16-Bit Real Mode Cache-Hit Cycles	16-Bit Protected Mode Cache-Miss Cycles	16-Bit Protected Mode Cache-Hit Cycles
sbb mb,ib	7	5	7	5
sbb mb,rb	7	5	7	5
sbb mw,iw	7	5	7	5
sbb mw,rw	7	5	7	5
sbb rb,ib	2	2	2	2
sbb rb,mb	6	4	6	4
sbb rb,rb	2	2	2	2
sbb rw,iw	2	2	2	2
sbb rw,mw	6	4	6	4
sbb rw,rw	2	2	2	2
scasb	8	7	8	7
scasd	10	7	10	7
scasw	8	7	8	7
shl mb,cl	7	6	7	6
shl mb,ib	7	6	7	6
shl mw,cl	7	6	7	6
shl mw,ib	7	6	7	6
shl rb,cl	3	3	3	3
shl rb,ib	3	3	3	3
shl rw,cl	3	3	3	3
shl rw,ib	3	3	3	3
shld mw,rw,cl	7	6	7	6
shld mw,rw,ib	7	6	7	6
shld rw,rw,cl	3	3	3	3
shld rw,rw,ib	3	3	3	3
shld mdw,rdw,cl	9	6	9	6
shld mdw,rdw,ib	9	6	9	6
shld rdw,rdw,cl	3	3	3	3
shld rdw,rdw,ib	3	3	3	3
shr mb,cl	7	6	7	6
shr mb,ib	7	6	7	6
shr mw,cl	7	6	7	6
shr mw,ib	7	6	7	6
shr rb,cl	3	3	3	3
shr rb,ib	3	3	3	3
shr rw,cl	3	3	3	3
shr rw,ib	3	3	3	3
shrd mw,rw,cl	7	6	7	6
shrd mw,rw,ib	7	6	7	6
shrd rw,rw,cl	3	3	3	3
shrd rw,rw,ib	3	3	3	3
shrd mdw,rdw,cl	9	6	9	6
shrd mdw,rdw,ib	9	6	9	6
shrd rdw,rdw,cl	3	3	3	3
shrd rdw,rdw,ib	3	3	3	3
stc	2	2	2	2

Figure A-1 (Part 7 of 8). Instruction Cycle Times

Mnemonic	16-Bit Real Mode Cache-Miss Cycles	16-Bit Real Mode Cache-Hit Cycles	16-Bit Protected Mode Cache-Miss Cycles	16-Bit Protected Mode Cache-Hit Cycles
std	2	2	2	2
sti	5	5	5	5
stosb	5	5	5	5
stosd	5	5	5	5
stosw	5	5	5	5
sub mb,ib	7	5	7	5
sub mb,rb	7	5	7	5
sub mw,iw	7	5	7	5
sub mw,rw	7	5	7	5
sub rb,ib	2	2	2	2
sub rb,mb	6	4	6	4
sub rb,rb	2	2	2	2
sub rw,iw	2	2	2	2
sub rw,mw	6	4	6	4
sub rw,rw	2	2	2	2
test mb,ib	5	3	5	3
test mw,iw	5	3	5	3
test rb,ib	2	2	2	2
test rb,mb	5	3	5	3
test rb,rb	2	2	2	2
test rw,iw	2	2	2	2
test rw,mw	5	3	5	3
test rw,rw	2	2	2	2
xlat	5	4	5	4
xor mb,ib	7	5	7	5
xor mb,rb	7	5	7	5
xor mw,iw	7	5	7	5
xor mw,rw	7	5	7	5
xor rb,ib	2	2	2	2
xor rb,mb	5	3	5	3
xor rb,rb	2	2	2	2
xor rw,iw	2	2	2	2
xor rw,mw	5	3	5	3
xor rw,rw	2	2	2	2

Figure A-1 (Part 8 of 8). Instruction Cycle Times

Index

Numerics

386SLC microprocessor 1-13, 3-3
486SLC2 microprocessor 1-14, 3-4
80386SX microprocessor 1-13, 3-3
80387SX math coprocessor 3-6

A

adapter
  setup 2-4
adapter setup register 2-14
address 20 gate 3-30
address and NMI mask register, RT/CMOS 3-19
address map
  memory 3-16
  POS I/O 2-5
  system board I/O 1-10
alternate reset 3-31
altitude 1-15, 1-16
anticipated page miss 1-13, 1-14
arbiter programming 3-8
arbitration control point 3-6
arbitration level 3-7
arbitration register 3-8
arbitration, central control point 3-8

B

base memory bytes 3-27
battery 3-23
boot sequence 3-33
bus adapter 3-9
bus contention 2-3
bus priority assignments 3-7

C

cables 1-15, 1-16
cache
  address space 3-6
cache *(continued)*
  operation 3-5
card selected feedback register 2-6
-CD SFDBK 2-6
central arbitration control point 3-6
channel 1-4, 3-6
  check enable 3-29
  check latch 3-29
  connector 3-9
  DMA 3-7
clock, real-time 3-18, 3-21
CMOS RAM 3-18—3-27
codes, POST error 3-34
compatibility 3-33
configuration
  CRC bytes 3-27
  RT/CMOS 3-24
connector
  channel 3-9
  drives 3-10
  memory 3-11, 3-12
contention, bus 2-3
control ports, system 3-29—3-31
controller
coprocessor, math 3-6
cover lock 3-32
current, electrical 1-15, 1-16

D

data register, RT/CMOS 3-20
date century byte 3-27
date status indicator 3-24
depth, system unit 1-15, 1-16
description, power supply 1-17
diagnostic status byte (RT/CMOS) 3-24
diskette drive
diskette drive connector 3-10
diskette drive information, POS 2-11

© Copyright IBM Corp. 1991, 1992

diskette drive type byte 3-24
diskette overruns 3-7
display operating mode 3-26
DMA
  channels 3-7
  performance 1-13, 1-14

E

enable NMI 3-19
equipment byte 3-26
error codes, POST 3-34
extended arbitration 3-9

F

failures and messages, POST 3-34
fault, overvoltage 1-19
feedback, card selected 2-6
fixed disk drive
  initialization 3-24
  type byte 3-25

G

gate A20 3-30

H

height, system unit 1-15, 1-16
humidity 1-15, 1-16

I

I/O
  address map 1-10
  RT/CMOS RAM operations 3-20
instruction cycle times A-1
interleaving, memory 3-15
  mem.interleaving 3-15
interrupt
  IRQ0 reset 3-29
  NMI reset 3-28

K

keyboard
  cable 1-15, 1-16
  password 3-32

L

low and high usable memory
  byte 3-27

M

math coprocessor 3-6
measurements, system unit 1-15, 1-16
memory
  bytes 3-27
  connectors 3-11, 3-12
  description 3-13
  performance 1-13, 1-14
  RAM 3-14
  read 1-13, 1-14
  refresh 3-7
  ROM 3-14
  RT/CMOS RAM 3-18
  size miscompare 3-24
  system memory map 3-16
  write 1-13, 1-14
memory information, POS 2-10
memory-presence detect
  signals 3-15
messages, POST error 3-34
Micro Channel 1-4
Micro Channel architecture
  arbitration control point 3-6
  bus adapter 3-9
  general information 3-6
microprocessor
  386SLC 3-3
  386SLC instructions 3-4
  386SLC programming
    considerations 3-4
  486SLC2 3-4
  80386SX 3-3
  alternate reset 3-31
  mode switch compatibility 3-31

microprocessor *(continued)*
performance 1-13, 1-14
mode switch, protected 3-31

N

NMI mask register 3-19
NMI service 3-7
NMI signal 3-7
nonmaskable interrupt (NMI) 3-28
nonvolatile RAM (NVRAM) 3-28

O

operating system boot sequence 3-33
output voltage sequencing 1-19
outputs, power supply 1-18
overvoltage fault 1-19

P

page hit 1-13, 1-14
page miss 1-13, 1-14
parallel port select 2-9
parity check enable 3-30
password
keyboard 3-32
power-on 3-30, 3-31
privileged-access 3-32
performance, system 1-13, 1-14
port
system 3-29
POS
See programmable option select (POS)
POS address map 2-5
POS register 3 2-10
POS register, diskette drive 2-11
POST (power-on self-test) 3-14, 3-31
POST error codes 3-34
power
cable 1-15, 1-16
loss 3-23
specifications 1-15, 1-16
power supply 1-4
power supply description 1-17
power supply output protection 1-19
power supply outputs 1-18
power-on password 3-30, 3-31
power-on self-test (POST) 3-14, 3-31
privileged-access password 3-32
programmable option select (POS)
address map 2-5
card selected feedback register 2-6
description 2-3
setup procedures 2-4
system board enable/setup register 2-7
system board setup 2-6
system configuration utilities 2-3
system memory map 3-16
video 2-7
warning 2-3
programming, arbiter 3-8
protected mode switch 3-31
protection, power supply 1-19

R

RAM (random access memory) 3-14
random access memory (RAM) 3-14
read-only memory (ROM) 3-14
real mode switch 3-31
real-time clock 3-18, 3-21
refresh 3-7
refresh request 1-13, 1-14, 3-29
register
adapter setup 2-14
card selected feedback 2-6
miscellaneous system 3-29
RT/CMOS address and NMI mask 3-19
RT/CMOS data 3-20
RT/CMOS status 3-21—3-23
system board enable/setup 2-7
system board POS 2-5

register *(continued)*
system control 3-29
reset, alternate 3-31
ROM (read-only memory) 3-14
RT/CMOS RAM
address and NMI mask register 3-19
address map 3-19
configuration bytes 3-24
data register 3-20
description 3-18
diagnostic status byte 3-24
I/O operations 3-20
power-on password 3-31
secured area 3-30
status registers 3-21—3-23

S

selectable boot 3-33
sequencing, output voltage 1-19
set configuration 3-33
setup
bus contention 2-3
system board 2-6
system board group 1 2-4
system board group 2 2-4
system board group 3 2-5
system board SCSI controller setup 2-5
system memory map 3-16
video 2-7
shutdown status byte 3-24
signal
card selected feedback 2-6
size, system unit 1-15, 1-16
speaker data enable 3-30
specifications
performance 1-13, 1-14
physical 1-15, 1-16
startup sequence 3-33
status registers (RT/CMOS) 3-21—3-23
switch to real mode 3-31
system
configuration utilities 2-3
control ports 3-29—3-31
system *(continued)*
functions, miscellaneous 3-29
performance 1-13, 1-14
reset 3-28
specifications 1-15, 1-16
system board
address map 1-10
description 3-3
enable/setup register 2-7
memory connector 3-11, 3-12
microprocessors 3-3
POS I/O address map 2-5
setup 2-4, 2-5, 2-6
system description 1-3

T

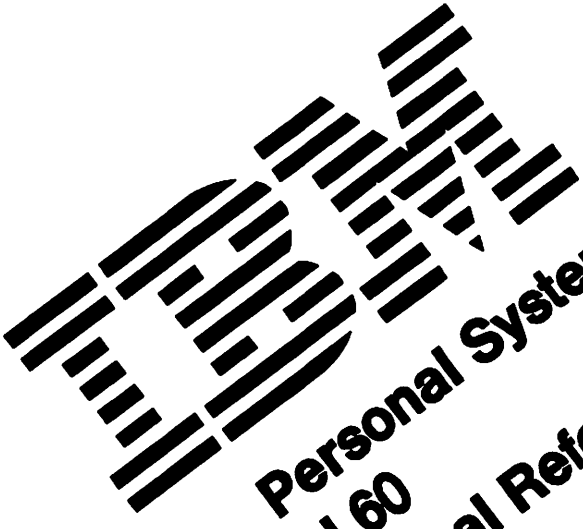
tamper-evident switch 3-32
temperature 1-15, 1-16
time status indicator 3-24

V

video
setup 2-7
subsystem 2-4
vital product data (VPD) 3-28
VPD 3-28

W

warning
arbitration 3-7
central arbiter 3-9
NMI mask 3-28
POS 2-3
RT/CMOS 3-19
watchdog status 3-30
weight, system unit 1-15, 1-16
width, system unit 1-15, 1-16



Personal System/2
Model 60
Technical Reference

Second Edition (October 1990)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer of express or implied warranties in certain transactions, therefore, this statement may not apply to you.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Requests for technical information about IBM products should be made to your IBM Authorized Dealer or your IBM Marketing Representative.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

© Copyright International Business Machines Corporation 1989, 1990. All rights reserved.

Note to U.S. Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Special Notices

References in this publication to IBM products, programs, or services do not imply that IBM intends to make these available in all countries in which IBM operates. Any reference to an IBM product, program or service is not intended to state or imply that only IBM's product, program, or service may be used. Any functionally equivalent product, program, or service that does not infringe any of IBM's intellectual property rights or other legally protectible rights may be used instead of the IBM product, program, or service. Evaluation and verification of operation in conjunction with other products, programs, or services, except those expressly designated by IBM, are the user's responsibility.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

The following terms, denoted by an asterisk (*) in this publication, are trademarks of the IBM Corporation in the United States and/or other countries:

IBM
Micro Channel
Personal Computer AT
Personal System/2
PS/2

The following terms, denoted by a double asterisk (**) in this publication, are trademarks of other companies as follows:

Hitachi	Hitachi Corporation
Intel	Intel Corporation
Motorola	Motorola, Incorporated

Preface

This technical reference contains hardware and software interface information specific to the IBM Personal System/2 Model 60 computer. It is intended for those who develop hardware and software products for these systems. Users should understand computer architecture and programming concepts.

This publication consists of the following sections:

Section 1, "System Overview," describes the system, features and specifications.

Section 2, "Programmable Option Select," describes registers used for configuration.

Section 3, "System Board," describes the system specific hardware implementations.

This technical reference should be used with the following publications:

IBM Personal System/2 Hardware Interface Technical Reference — Architectures

IBM Personal System/2 Hardware Interface Technical Reference — Common Interfaces

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference

These publications contain additional information on many of the subjects discussed in this technical reference.

Warning: The term "Reserved" describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

© Copyright IBM Corp. 1989, 1990

Contents

Section 1. System Overview 1-1
Description 1-3
System Board Features 1-3
System Board Block Diagram 1-5
System Board I/O Address Map 1-6
Specifications 1-7
| Power Supply 1-10
| Outputs 1-10
| Output Protection 1-11
| Voltage Sequencing 1-11
| Power Supply Connectors 1-11

Section 2. Programmable Option Select 2-1
Description 2-3
POS Address Map 2-5
Card Selected Feedback 2-6
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-7
System Board POS Register 2 (Hex 0102) 2-8
System Board POS Register 3 (Hex 0103) 2-9
Adapter Enable/Setup Register (Hex 0096) 2-10

Section 3. System Board 3-1
Description 3-3
| Micro Channel Implementation 3-3
| Exception Reporting 3-3
Adapter Identification 3-3
Central Arbiter 3-3
Memory 3-7
Read-Only Memory Subsystem 3-7
Random Access Memory Subsystem 3-7
Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM 3-10
Miscellaneous System Functions 3-20
Nonmaskable Interrupt 3-20
System Control Port B (Hex 0061) 3-20
System Control Port A (Hex 0092) 3-21
Power-On Password 3-23
Hardware Compatibility 3-24

Index X-1

© Copyright IBM Corp. 1989, 1990

Figures

1-1. System Board Devices and Features 1-4
1-2. System Board 1-5
1-3. System Board I/O Address Map 1-6
1-4. Performance Specifications — System Board 1-7
1-5. Physical Specifications 1-8
1-6. Acoustical Readings 1-9
1-7. Component Maximum Current 1-10
1-8. Channel Load Current 1-10
1-9. Voltage Assignments for the Internal Drive Power-Supply Connectors 1-11
2-1. POS I/O Address Map 2-5
2-2. Card Selected Feedback Register (Hex 0091) 2-6
2-3. System Board Enable/Setup Register (Hex 0094) 2-7
2-4. System Board POS Register 2 (Hex 0102) 2-8
2-5. Parallel Port Select Bits 2-8
2-6. System Board POS Register (Hex 0103) 2-9
2-7. Adapter Enable/Setup Register (Hex 0096) 2-10
3-1. Arbitration Bus Priority Assignments 3-4
3-2. Arbitration Register, Write to Hex 0090 3-5
3-3. Arbitration Register, Read Hex 0090 3-5
3-4. System Memory Map 3-8
3-5. System Board Memory Connector 3-9
3-6. RT/CMOS RAM Address Map 3-10
3-7. RT/CMOS Address Register and NMI Mask (Hex 0070) 3-11
3-8. RT/CMOS Data Register (Hex 0071) 3-11
3-9. Real-Time Clock Bytes 3-13
3-10. Status Register A 3-13
3-11. Status Register B 3-14
3-12. Status Register C 3-15
3-13. Status Register D 3-15
3-14. Diagnostic Status Byte 3-16
3-15. Diskette Drive Type Byte 3-17
3-16. Diskette Drive Type Byte (Bits 7 - 4) 3-17
3-17. Diskette Drive Type Byte (Bits 3 - 0) 3-17
3-18. Equipment Byte 3-18
3-19. Equipment Byte (Bits 7, 6) 3-18
3-20. Equipment Byte (Bits 5, 4) 3-18
3-21. System Control Port B (Write) 3-20
3-22. System Control Port B (Read) 3-21
3-23. System Control Port A (Hex 0092) 3-21

© Copyright IBM Corp. 1989, 1990

Section 1. System Overview

Description 1-3
System Board Features 1-3
System Board Block Diagram 1-5
System Board I/O Address Map 1-6
Specifications 1-7
| Power Supply 1-10
| Outputs 1-10
| Output Protection 1-11
| Voltage Sequencing 1-11
| Power Supply Connectors 1-11

© Copyright IBM Corp. 1989, 1990

Notes:

Description

The IBM* Personal System/2* Model 60 computer is a self-contained, floor-standing system that features the Micro Channel* architecture. It comes with a keyboard, and can support two diskette drives and two internal fixed disk drives.

Programs can identify the system by reading the model and submodel bytes. The model and submodel byte for this system is hex FC and 05, respectively. Interrupt hex 15, function code (AH)= hex C0, returns the model and submodel bytes and BIOS revision code.

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems, and check the supplements section for updates to that listing.

System Board Features

The following figure lists the system board devices and features. The Hardware Interface Technical Reference manuals describe all devices common to PS/2* products by type number.

* IBM, Personal System/2, PS/2, and Micro Channel are trademarks of the International Business Machines Corporation.

Device	Type	Features
Microprocessor	—	80286 24-bit address and 16-bit data interface
System Timers	1	Channel 0 – System timer Channel 2 – Tone generation for speaker Channel 3 – Watchdog timer
ROM Subsystem	—	128KB (KB = 1024 bytes)
RAM Subsystem	—	1MB (MB = 1,048,576 bytes) Expandable on the channel
CMOS RAM Subsystem	—	64-byte CMOS RAM with real-time clock/calendar 2KB CMOS RAM extension Battery backup
Video Subsystem	1	Auxiliary connector on the channel Analog output 256KB video memory
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal.
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	1	Supports: - 720KB formatted diskette density - 1.44MB formatted diskette density.
Serial Controller	1, 2	RS-232C interface Programmable as serial port 1 or 2 FIFO mode* and character mode
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output
Micro Channel	—	Eight channel connectors for Type 3 adapters - 8- or 16-bit device support - One with an auxiliary video extension - One occupied by the fixed disk drive adapter
Math Coprocessor Socket	—	Supports 80287 math coprocessors Same clock speed as the system microprocessor

* The FIFO mode is supported by the Type 2 serial controller.

Figure 1-1. System Board Devices and Features

System Board Block Diagram

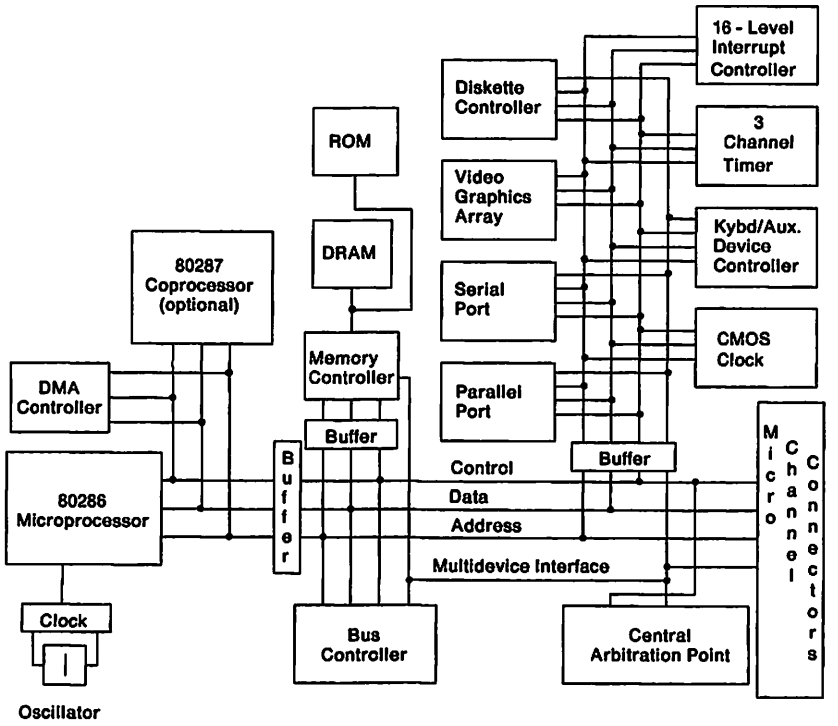


Figure 1-2. System Board

System Board I/O Address Map

Hex Addresses	Device
0000 - 001F	DMA Controller (0 – 3)
0020, 0021	Interrupt Controller (Master)
0040, 0042 - 0044, 0047	System Timers
0060	Keyboard, Auxiliary Device
0061	System Control Port B
0064	Keyboard, Auxiliary Device
0070, 0071	RT/CMOS and NMI Mask
0081 - 0083, 0087	DMA Page Registers (0 – 3)
0089, 008A, 008B, 008F	DMA Page Registers (4 – 7)
0090	Central Arbitration Control Point
0091	Card Selected Feedback Register
0092	System Control Port A
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
00A0 - 00A1	Interrupt Controller (Slave)
00C0 - 00DF	DMA Controller (4 – 7)
00F0 - 00FF	Math Coprocessor
0100 - 0107	Programmable Option Select
01F0 - 01F8	Fixed Disk Drive Controller
0278 - 027B	Parallel Port 3
02F8 - 02FF	Serial Port 2 (RS-232C)
0378 - 037B	Parallel Port 2
03B4, 03B5, 03BA	Video Subsystem
03BC - 03BF	Parallel Port 1
03C0 - 03C5	Video Subsystem
03C6 - 03C9	Video DAC
03CA, 03CC, 03CE, 03CF	Video Subsystem
03D4, 03D5, 03DA	Video Subsystem
03F0 - 03F7	Diskette Drive Controller
03F8 - 03FF	Serial Port 1 (RS-232C)

Figure 1-3. System Board I/O Address Map

Specifications

The following figure describes system board performance.

Device	Number of Waits	Cycle Time (ns)
Microprocessor (10 MHz – 100 ns Clock):		
Access to System Board RAM	1	300
Access to System Board ROM	1	300
Access to Channel:		
Default Transfer Cycle:		
I/O Access	1	300
Memory Access	0	200
Synchronous Extended Transfer Cycle	1	300
Refresh Rate (Typically performed every 15.1 μs)		500 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer: 300 + I/O Access + Memory Access		
Burst Transfers: 300 + (I/O Access + Memory Access)N *		
System Board Memory Access		300
Default Transfer Cycle:		
I/O Access		300
Memory Access		200
Synchronous Extended Transfer Cycle		300

* N is the number of transfers in the burst.

Figure 1-4. Performance Specifications – System Board

The following figure describes physical specifications of the system.

Size:	
Width	165 mm (6.5 in)
Width (Feet extended)	318 mm (12.5 in)
Depth	483 mm (19.0 in)
Height	597 mm (23.5 in)
Weight	20 kg (44 lb) with one fixed disk drive
Cables:	
Power Cable	1.8 m (6 ft)
Keyboard Cable	3.05 m (10 ft)
Air Temperature:	
System On	15.6 to 32.2°C (60 to 90°F)
System Off	10.0 to 43.0°C (50 to 110°F)
Humidity:	
System On	8% to 80%
System Off	8% to 80%
Maximum Altitude	2133.6 m (7000 ft)
Heat Output:	
207 Watt Power Supply	320 Watts (1100 BTUs/hour)
225 Watt Power Supply	350 Watts (1200 BTUs/hour)
250 Watt Power Supply	390 Watts (1330 BTUs/hour)
Acoustical Readings	(See Figure 1-6 on page 1-9)
Electrical Input:	
Input Voltage (Range is automatically selected; sinewave input is required):	
Low Range	90 (min) – 137 (max) Vac
High Range	180 (min) – 265 (max)Vac
Frequency:	
Low Range	47 (min) – 53 (max) Hz
High Range	57 (min) – 63 (max) Hz
Input in Kilovolt-Ampere (kVA):	
Minimum configuration (as shipped by IBM)	0.10 kVA
Maximum configuration:	
207 Watt Power Supply	0.53 kVA
225 Watt Power Supply	0.58 kVA
250 Watt Power Supply	0.65 kVA
Electromagnetic Compatibility	FCC Class B

Figure 1-5. Physical Specifications

The following figure describes the acoustical readings of the system.

Description	L_{WAd} in bels Operate	Idle	L_{pAm} in dB Operate	Idle	$<L_{pA}>_m$ in dB Operate	Idle
Model 60	5.1	5.1	41	40	38	37

Notes:

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

All measurements made in accordance with ANSI S12.10, and reported in conformance with ISO DIS 9296.

The measurements are preliminary data and subject to change.

Figure 1-6. Acoustical Readings

Power Supply

The power supply requires a sinewave input and converts the ac input voltage to three dc output voltages. The power supply provides power for the following:

- System board
- Channel adapters
- Internal diskette drives
- Internal fixed disk drives
- Auxiliary device
- Keyboard.

The power switch and one light-emitting diode (LED) is on the front of the system unit. The power supply is operating when the LED is lit.

Outputs

The power supply provides separate voltage sources for the system board and the drives. The system-board voltages are +5 Vdc, +12 Vdc, and −12 Vdc. The drive voltages are +5 Vdc and +12 Vdc. The following is a list of the approximate power provided for system components.

System Component	Maximim Current	
	+12 Vdc	+5 Vdc
Internal Fixed Disk Drives (per power supply connector)	2.5 A	1.5 A
Auxiliary Device	None	300 mA
Keyboard	None	275 mA

Figure 1-7. Component Maximum Current

The following are the load currents allowed for each Micro Channel connector.

Supply Voltage	Maximum Current
+ 5.0 Vdc	1.6 A
+12.0 Vdc	0.175 A
−12.0 Vdc	0.040 A

Figure 1-8. Channel Load Current

The formulas used to determine the power requirements and the voltage regulation tolerances are in the Micro Channel adapter

| design information in the *Hardware Interface Technical Reference - Architectures* manual.

Output Protection

A short circuit placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state with no damage to the power supply.

If an overvoltage fault occurs (internal to the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of its nominal value.

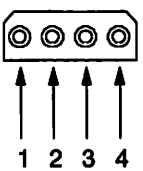
If either of these shutdown states is actuated, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least ten seconds.

Voltage Sequencing

At power-on time, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Power Supply Connectors

The power supply provides two 4-pin connectors for internal fixed disk drives. These connectors can be extended to provide power to more than one internal drive as long as the total power does not exceed the specifications shown in Figure 1-7 on page 1-10.



Pin	Signal
1	+12 Vdc
2	DC Return
3	DC Return
4	+5 Vdc

Figure 1-9. Voltage Assignments for the Internal Drive Power-Supply Connectors

Notes:

Section 2. Programmable Option Select

Description 2-3
POS Address Map 2-5
Card Selected Feedback 2-6
System Board Setup 2-6
  System Board Enable/Setup Register (Hex 0094) 2-7
  System Board POS Register 2 (Hex 0102) 2-8
  System Board POS Register 3 (Hex 0103) 2-9
  Adapter Enable/Setup Register (Hex 0096) 2-10

© Copyright IBM Corp. 1989, 1990

Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used specifically by the Model 60 system board. For additional POS information, refer to the Hardware Interface Technical Reference Micro Channel architecture information.

Warning:

- IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can cause multiple assignment of the same system resource, improper operation of the feature, loss of data, or possible damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention will occur, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- The channel reset bit (bit 7) in the Adapter Enable/Setup register must be 0 to program the adapters.
- The system board does not support 16-bit I/O operations to 8-bit POS registers. Using 16-bit I/O instructions on 8-bit POS registers will cause erroneous data to be written to or read from the registers. Only 8-bit transfers are supported for setup operations.

Setup functions respond to I/O addresses hex 0100 through 0107 only when their unique setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

System Board Video Subsystem Setup:

- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 0 to place the system board video into the setup mode.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 7 in the System Board Enable/Setup register (hex 0094) must be set to 1 to avoid driving a 'setup' signal to other system board functions.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 1 to allow adapter setup.
- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 1 to avoid driving a 'setup' signal to the Video Subsystem.
- Bit 7 in the System Board Enable/Setup register (hex 0094) must be set to 1 to avoid driving a 'setup' signal to a system board function.

Other System Board Setup:

- Bit 7 in the System Board Enable/Setup register (hex 0094) must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 1 to avoid driving a 'setup' signal to the Video Subsystem.

POS Address Map

The following figure shows the organization of the I/O address space used by POS. The POS registers are 8-bit registers. Bit 0 of POS Register 2 and bits 6 and 7 of POS Register 5 are defined. All other bits in POS Registers 2 through 5 are free-form.

Address (Hex)	Function
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
0100	POS Register 0—Adapter Identification Byte (Low Byte)
0101	POS Register 1—Adapter Identification Byte (High Byte)
0102	POS Register 2—Option Select Data Byte 1 Bit 0 is Card Enable.
0103	POS Register 3—Option Select Data Byte 2
0104	POS Register 4—Option Select Data Byte 3
0105	POS Register 5—Option Select Data Byte 4 Bit 7 is the channel check active indicator. Bit 6 is the channel check status-available indicator.
0106	Reserved
0107	Reserved

Figure 2-1. POS I/O Address Map

Card Selected Feedback

When the adapter is addressed, it responds by setting the '-card selected feedback' signal (-CD SFDBK) to active. -CD SFDBK is derived from the address decode and driven by a totem pole driver. It is latched by the system board and can be read through the Card Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and thereby determine if the video subsystem, system board I/O, or an adapter is addressed and functioning.

Bit	Function
7 - 1	Reserved
0	-Card Selected Feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7 - 1 Reserved.

Bit 0 This bit is set to 1 whenever -CD SFDBK was active on a previous cycle or whenever the system board I/O functions (diskette drive, serial, or parallel interfaces) are accessed by an I/O cycle. Reading this register resets the bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information during setup. The diskette drive controller, serial port, and parallel port are treated as a single device. The video subsystem is also an integrated part of the system board; however, POS treats it as a separate device. The System Board Enable/Setup register is used to place the system board or video subsystem into the setup mode.

System Board Enable/Setup Register (Hex 0094)

This is a read/write register; all bits in this register default to 1 (enabled).

Bit	Function
7	Enable/-Setup System Board Functions
6	Reserved
5	Enable/-Setup Video Subsystem
4 - 0	Reserved

Figure 2-3. System Board Enable/Setup Register (Hex 0094)

Bit 7 When this bit is set to 0, various system board I/O functions are placed in the setup mode. The diskette drive controller, serial port, and parallel port are controlled through System Board POS Register 2 (hex 0102). The memory is controlled through System Board POS Register 3 (hex 0103).

When this bit is set to 1, the system board functions are enabled.

Bit 6 Reserved.

Bit 5 When this bit is set to 0, the video subsystem is placed in the setup mode and controlled through POS Register 2 (hex 0102). When set to 1, and bit 0 in hex 0102 is set to 1, video is enabled.

Bit 0 of POS Register 2 is the video enable bit. When this bit is set to 0, the video subsystem does not respond to commands, addresses, or data. If video is being generated when the video enable bit is set to 0, the output is still generated. For information on BIOS calls to enable or disable the video, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Note: When the video is disabled, access to the video DAC registers is disabled.

Bits 4 - 0 Reserved.

System Board POS Register 2 (Hex 0102)

When the system board is in the setup mode, the diskette drive controller, serial port, and parallel port are controlled by this read/write register. Reading this register returns the current state of these system board functions.

Bit	Function
7	Disable Parallel Port Extended Mode
6, 5	Parallel Port Select
4	Enable Parallel Port
3	Serial Port Select
2	Enable Serial Port
1	Enable Diskette Drive Interface
0	Enable System Board

Figure 2-4. System Board POS Register 2 (Hex 0102)

Bit 7 When set to 0, this bit allows the parallel port to be configured as an 8-bit parallel bidirectional interface. When set to 1, this bit disables the bidirectional mode. This bit is set to 0 at power-on, and POST sets it to 1.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Hex Address	Interrupt Level
0 0	Parallel 1	03BC - 03BF	7
0 1	Parallel 2	0378 - 037B	7
1 0	Parallel 3	0278 - 027B	7
1 1	Reserved	----------	-

Figure 2-5. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bit 3 When set to 1, this bit sets the system board serial port as Serial 1 (addresses hex 03F8 through 03FF), which uses interrupt level 4. When set to 0, this bit sets the serial port as Serial 2 (addresses hex 02F8 through 02FF), which uses interrupt level 3.

Bit 2 When this bit and bit 0 are set to 1, the system board serial port is enabled.

Bit 1 When this bit and bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When set to 1, this bit allows bits 4, 2, and 1 to enable and disable their respective devices. When set to 0, this bit disables the diskette drive interface, system board serial port, and system board parallel port, regardless of the state of bits 4, 2, and 1.

System Board POS Register 3 (Hex 0103)

With the system board in setup, this register controls the system board memory.

Bit	Function
7 - 1	Reserved
0	Enable System Board RAM

Figure 2-6. System Board POS Register (Hex 0103)

Bit 7 - 1 Reserved.

Bit 0 When set to 1, this bit enables the system board memory. When set to 0, this bit disables the memory. All system board memory is enabled or disabled by this operation.

Adapter Enable/Setup Register (Hex 0096)

The Adapter Enable/Setup register selects the connector to be configured.

Bit	Symbol
7	Channel Reset
6 - 4	Reserved
3	Card Setup Enable
2 - 0	Channel Select 2 - 0

Figure 2-7. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6 - 4 These bits are reserved.

Bit 3 When set to 1, this bit enables the '-card setup' signal selected by bits 2 through 0.

Bits 2 - 0 These bits are the address bits for the '-card setup' signal Connectors 1 through 8 are addressed as 0 through 7, respectively. When bit 3 is set to 1, these bits select the connector that is put into setup.

Each channel connector has a unique '-card setup' signal (-CD SETUP) associated with it. This signal is used to put the adapters in the setup mode, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Notes:

1. -CD SETUP only goes active when an operation is performed in the I/O address range hex 0100 through 0107.
2. The status of port hex 0096 can be read by software. However, when the port is read, bits 6, 5, and 4 are set to 1.

Section 3. System Board

Description 3-3
Micro Channel Implementation 3-3
Exception Reporting 3-3
Adapter Identification 3-3
Central Arbiter 3-3
Arbitration Bus Priority Assignments 3-4
Central Arbiter Programming 3-5
Memory 3-7
Read-Only Memory Subsystem 3-7
Random Access Memory Subsystem 3-7
System Memory Maps 3-8
System Board Memory Connector 3-9
Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM 3-10
RT/CMOS Address Register and NMI Mask (Hex 0070) . . 3-11
RT/CMOS Data Register (Hex 0071) 3-11
RT/CMOS RAM I/O Operations 3-12
Real-Time Clock Bytes (Hex 000-00D) 3-13
CMOS RAM Configuration 3-16
Miscellaneous System Functions 3-20
Nonmaskable Interrupt 3-20
System Control Port B (Hex 0061) 3-20
System Control Port A (Hex 0092) 3-21
Power-On Password 3-23
Hardware Compatibility 3-24

© Copyright IBM Corp. 1989, 1990

Notes:

Description

This section provides information about the Model 60 implementation of the Micro Channel architecture, memory subsystem, and miscellaneous system ports. Additional information on these topics can be found in the *Hardware Interface Technical Reference* listed in the preface of this manual.

Micro Channel Implementation

The POST routines and registers used to implement programmable features of the Micro Channel architecture may vary from system to system. This section provides information about the Model 60 implementation of the Micro Channel architecture.

Exception Reporting

Exceptions should be reported using the asynchronous channel check procedure. The synchronous channel check procedure is not supported.

Adapter Identification

When the system is powered on, an adapter can issue an ID of hex 0000 for up to 1 second after channel reset to indicate it is not ready. Any adapter that continues to issue an adapter ID of hex 0000 (not ready) for more than 1 second is considered defective. On the Model 60, if the channel reset was caused by a keyboard sequence or a program routine, this time is reduced to 740 milliseconds.

Central Arbiter

The central arbitration control point gives intelligent subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. This arbiter supports up to 16 arbitrating devices.

Arbitration Bus Priority Assignments

The following figure shows the assignment of arbitration levels. The functions with the lowest arbitration level have the highest priority.

ARB Level	Primary Assignment
-2	Memory Refresh
-1	NMI
0	DMA Channel 0 (Programmable to any arbitration level)
1	DMA Channel 1
2	DMA Channel 2
3	DMA Channel 3
4	DMA Channel 4 (Programmable to any arbitration level)
5	DMA Channel 5
6	DMA Channel 6
7	DMA Channel 7
8-E	Available
F	System Microprocessor

Figure 3-1. Arbitration Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation, and by the previous controlling master. The diskette drive controller should not be held inactive for more than 12 microseconds to prevent overrun.

NMI service is executed at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal (ARB/-GNT)) is in the arbitrate state.

When the central arbitration control point receives a level -1 request (NMI, a system-board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level -1 request, and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following figures.

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Mask
5	Enable Extended Arbitration
4 - 0	Reserved

Figure 3-2. Arbitration Register, Write to Hex 0090

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Masked by NMI
5	Bus Time-out
4	Reserved
3 - 0	Value of Arbitration Bus During Previous Grant State

Figure 3-3. Arbitration Register, Read Hex 0090

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 enables extended arbitration. The minimum arbitration cycle is 300 nanoseconds; this bit extends that minimum cycle to 600 nanoseconds. This bit is set to 0 during a system reset.

Reading this bit as a 1 indicates that a bus time-out has occurred, and resets bit 6 in this register to 0.

Bit 4 This bit is reserved and should be 0.

Bits 3 - 0 These bits are undefined for a write operation and should be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Memory

The Model 60 system uses the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- Real-time Clock and CMOS RAM.

Read-Only Memory Subsystem

The ROM subsystem system board consists of four 32Kb by 8-bit modules in a 64Kb by 16-bit arrangement (Kb equals 1024 bits).

ROM is not parity-checked and is assigned addresses at the top of the first and last 1MB of address space (hex 0E0000 and FE0000).

Random Access Memory Subsystem

The RAM subsystem on the system board starts at address hex 000000 of the 16MB address space. It consists of 1MB of RAM modules.

The system board uses four memory module packages that operate with one wait state. Memory-refresh typically occurs once every 15 microseconds.

The timing of the memory signals on the system board is similar to the Hitachi** HB61009BR-15, 150-nanosecond DRAM or equivalent.

** Hitachi is a trademark of the Hitachi Corporation.

System Memory Maps

The following figure shows the mapping of the memory locations on the Model 60. A 256-byte portion of this RAM is reserved as a BIOS data area. A 1KB portion of this RAM is reserved as an extended BIOS data area. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for details.

Hex Range	Function
000000 to 09FFFF	640KB System Board RAM *
0A0000 to 0BFFFF	128KB Video RAM
0C0000 to 0DFFFF	128KB I/O Expansion ROM
0E0000 to 0FFFFF	128KB System Board ROM
100000 to 15FFFF	384KB System Board RAM
160000 to FDFFFF	Channel Expansion Memory Addresses
FE0000 to FFFFFF	128KB System Board ROM

* With the system board in the setup mode, the system board memory can be disabled through System Board POS Register 3 (see page 2-9).

Figure 3-4. System Memory Map

System Board Memory Connector

The system board has four 30-pin connectors and comes with four 256KB memory module packages installed. The following figure shows the pin assignments and signal definitions for these connectors.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	+ 5 Vdc	2	I	-Column Address Strobe
3	I/O	Data Bit 1	4	I	Address Bit 1
5	I	Address Bit 2	6	I/O	Data Bit 2
7	I	Address Bit 3	8	I	Address Bit 4
9	N/A	Ground	10	I/O	Data Bit 3
11	I	Address Bit 5	12	I	Address Bit 6
13	I/O	Data Bit 4	14	I	Address Bit 7
15	I	Address Bit 8	16	I/O	Data Bit 5
17	I	Address Bit 9	18	N/A	No Connection
19	I	Reserved	20	I/O	Data Bit 6
21	I	-Write Strobe	22	N/A	Ground
23	I/O	Data Bit 7	24	O	Presence Detect
25	I/O	Data Bit 8	26	O	Presence Detect
27	I	Reserved	28	N/A	No Connection
29	I/O	Data Bit 9 (Parity)	30	N/A	+5 Vdc

Figure 3-5. System Board Memory Connector

Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM

The real-time clock/complementary metal-oxide semiconductor RAM (RT/CMOS) chip contains the real-time clock and 64 bytes of CMOS RAM. The internal clock circuitry uses 14 bytes of this memory, and the rest is allocated to configuration and system status information.

In addition to the 64 bytes of CMOS RAM, a 2KB CMOS RAM extension is provided for configuration and other system information.

A 6-Vdc lithium battery maintains voltage to the RT/CMOS RAM and 2KB CMOS RAM extension when the power supply is not in operation.

The system cover can be locked to prevent battery removal and loss of password and configuration information.

The following figure shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000 - 00D	Real-Time Clock Bytes
00E	Diagnostic Status Byte
00F	Shutdown Status Byte
010	Diskette Drive Type Byte
011	First Fixed Disk Drive Type Byte
012	Second Fixed Disk Drive Type Byte
013	Reserved
014	Equipment Byte
015 - 016	Low and High Base Memory Bytes
017 - 018	Low and High Expansion Memory Bytes
019 - 031	Reserved
032 - 033	Configuration CRC Bytes
034	Reserved
035 - 036	Low and High Useable Memory Bytes
037	Date Century Byte
038 - 03F	Reserved

Figure 3-6. RT/CMOS RAM Address Map

RT/CMOS Address Register and NMI Mask (Hex 0070)

This register is used in conjunction with the port at hex 0071 to read and write the RT/CMOS RAM bytes.

Bit	Function
7	NMI Mask
6	Reserved
5 - 0	RT/CMOS RAM Address

Figure 3-7. RT/CMOS Address Register and NMI Mask (Hex 0070)

Warning: The operation following a write to hex 0070 should access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Bit 7 When this bit is set to 1, the NMI is masked off (the NMI is disabled). This bit is set to 1 by a power-on reset and is a write-only bit.

Bit 6 Reserved.

Bits 5 - 0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This port is used in conjunction with the address register at hex 0070 to read and write the RT/CMOS RAM bytes.

Bit	Function
7 - 0	RT/CMOS Data

Figure 3-8. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts should be masked to prevent other interrupt service routines from changing the CMOS address register before data is read or written. After I/O operations, the RT/CMOS and NMI Mask register (hex 0070) should be left pointing to Status Register D (hex 00D).

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

The following steps are required to perform I/O operations to the RT/CMOS RAM addresses:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Write the data to address hex 0071.

Reading RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Read the data from address hex 0071.

Real-Time Clock Bytes (Hex 000-00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following figure.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second Alarm	1
002	Minutes	2
003	Minute Alarm	3
004	Hours	4
005	Hour Alarm	5
006	Day of Week	6
007	Date of Month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-9. Real-Time Clock Bytes

Note: The Setup program initializes status registers A, B, C, and D when the time and date are set. Interrupt hex 1A is the BIOS interface to read and set the time and date and it initializes the register the same way as the Setup program.

Status Register A (Hex 00A)

Bit	Function
7	Update in Progress
6 - 4	22-Stage Divider
3 - 0	Rate Selection Bits

Figure 3-10. Status Register A

Bit 7 When set to 1, this bit indicates the time-update cycle is in progress. When set to 0, it indicates the current date and time can be read.

Bits 6 - 4 These three divider-selection bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768 kHz time-base. This is the only value supported by the system for proper time-keeping.

Bits 3 - 0 These bits allow the selection of a divider output frequency. The system initializes the rate selection bits to a binary 0110, which selects a 1.024 kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Periodic Interrupt Enable
5	Alarm Interrupt Enable
4	Update-Ended Interrupt Enabled
3	Square Wave Enabled
2	Date Mode
1	24-Hour Mode
0	Daylight Savings Enabled

Figure 3-11. Status Register B

Bit 7 When set to 0, this bit updates the cycle, normally by advancing the counts at a rate of one per second. When set to 1, this bit immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This bit is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

Bit 5 When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit indicates if the time-and-date calendar updates use binary or binary-coded-decimal (BCD) formats. When set to 1, this bit indicates a binary format. The system initializes this bit to 0.

Bit 1 This bit establishes if the hours byte is in the 24-hour or 12-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When set to 1, this bit enables the daylight savings time mode. When set to 0, it disables the mode, and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt Request Flag
6	Periodic Interrupt Flag
5	Alarm Interrupt Flag
4	Update-Ended Interrupt Flag
3 - 0	Reserved

Figure 3-12. Status Register C

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 This bit is used in conjunction with bits 6, 5, and 4. When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When set to 1, this bit indicates that a periodic interrupt occurred.

Bit 5 When set to 1, this bit indicates that an alarm interrupt occurred.

Bit 4 When set to 1, this bit indicates that an update-ended interrupt occurred.

Bits 3 - 0 Reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6 - 0	Reserved

Figure 3-13. Status Register D

Bit 7 This read-only bit monitors the power-sense pin. A low state of this pin indicates a loss of power to the real-time clock (dead battery). When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power.

Bits 6 - 0 Reserved.

CMOS RAM Configuration

The following shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-Time Clock Chip Power
6	Configuration Record and Checksum Status
5	Incorrect Configuration
4	Memory Size Miscompare
3	Fixed Disk Controller/Drive C Initialization Status
2	Time Status Indicator
1	Adapter Configuration Miscompare
0	Adapter ID Time-Out

Figure 3-14. Diagnostic Status Byte

Bit 7 When set to 1, this bit indicates the real-time clock chip lost power.

Bit 6 When this bit is set to 1, the checksum is incorrect.

Bit 5 This is a check, at power-on time, of the Equipment byte. When set to 1, the configuration information is incorrect. Power-on checks require that at least one diskette drive be installed (bit 0 of the Equipment byte, hex 014, is set to 1).

Bit 4 When set to 1, this bit indicates the power-on check determined that the memory size is not the same as in the configuration record.

Bit 3 When set to 1, this bit indicates that the controller or drive C failed initialization, which prevents the system from attempting a power-on reset.

Bit 2 When set to 0, this bit indicates the time is valid. When set to 1, this bit indicates the time is invalid.

Bit 1 This bit indicates if the installed adapters match the configuration information. When this bit is set to 1, the adapters do not match the configuration information.

Bit 0 When set to 1, this bit indicates a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7 - 4	First Diskette Drive Type
3 - 0	Second Diskette Drive Type

Figure 3-15. Diskette Drive Type Byte

Bits 7 - 4 These bits indicate the first diskette drive type, as shown in the following figure.

Bits 7 6 5 4	Function
0 0 0 0	No drive present
0 0 0 1	Double-sided diskette drive (48 tracks per inch, 360KB)
0 0 1 1	High-capacity diskette drive (720KB)
0 1 0 0	High-density diskette drive (1.44MB)
All combinations that are not shown are reserved.	

Figure 3-16. Diskette Drive Type Byte (Bits 7 - 4)

Bits 3 - 0 These bits indicate the second diskette drive type, as shown in the following figure.

Bits 3 2 1 0	Function
0 0 0 0	No drive present
0 0 0 1	Double-sided diskette drive (48 tracks per inch, 360KB)
0 0 1 1	High-capacity diskette drive (720KB)
0 1 0 0	High-density diskette drive (1.44MB)
All combinations that are not shown are reserved.	

Figure 3-17. Diskette Drive Type Byte (Bits 3 - 0)

First Fixed Disk Drive Type Byte (Hex 011): This byte defines the type of the first fixed disk drive (drive C). Hex 00 indicates that a fixed disk drive is *not* installed.

Second Fixed Disk Drive Type Byte (Hex 012): This byte defines the type of the second fixed disk drive (drive D). Hex 00 indicates that a fixed disk drive is *not* installed.

Note: For more information about fixed disk drive types, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Reserved Byte (Hex 013): This byte is reserved.

Equipment Byte (Hex 014): The equipment byte defines the basic equipment in the system for the power-on diagnostic tests.

Bit	Function
7, 6	Number of Diskette Drives
5, 4	Display Operating Mode
3, 2	Reserved
1	Math Coprocessor Presence
0	Diskette Drive Presence

Figure 3-18. Equipment Byte

Bits 7, 6 These bits indicate the number of diskette drives installed, as shown in the following figure.

Bits 7 6	Number of Diskette Drives
0 0	One Drive
0 1	Two Drives
1 0	Reserved
1 1	Reserved

Figure 3-19. Equipment Byte (Bits 7, 6)

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port, as shown in the following figure.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-Column Mode
1 0	80-Column Mode
1 1	Monochrome Mode

Figure 3-20. Equipment Byte (Bits 5, 4)

Bits 3, 2 Reserved.

Bit 1 When set to 1, this bit indicates that a math coprocessor is installed.

Bit 0 When set to 1, this bit indicates that a diskette drive is installed.

Low and High Base Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 is equal to 640KB. The low byte is hex 15; the high byte is hex 16.

Low and High Expansion Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The hexadecimal values in these bytes represent the number of 1KB blocks of expansion memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 17; the high byte is hex 18.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 33; the high byte is hex 32.

| ***Reserved Byte (Hex 034):*** This byte is reserved.

| ***Low and High Useable Memory Bytes (Hex 035 and 036):*** These
| bytes define the total amount of useable memory above the 1MB
| address space.

| The hexadecimal values in these bytes represent the number of 1KB
| blocks of useable memory. For example, hex 0800 is equal to
| 2048KB. The low byte is hex 35; the high byte is hex 36.

Date Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 through 03F): These bytes are reserved.

Miscellaneous System Functions

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system Watchdog time-out has occurred. The NMI stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts and the IRET instruction restores the interrupt flag to the state it was in prior to the interrupt. A system reset causes a reset of the NMI.

Nonmaskable interrupt requests from system board parity and channel check are subject to mask control with the NMI mask bit in the RT/CMOS Address register. The Watchdog Timer and system channel time-out are not masked by this bit. (See "RT/CMOS RAM I/O Operations" on page 3-12). The power-on default of the NMI mask is 1 (NMI disabled). Prior to enabling the NMI after a power-on reset, the parity check and channel check state are initialized by the POST.

Warning: The operation following a write to hex 0070 should access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the read and write functions of this port are shown in the following figures.

Bit	Function
7	Reset Timer 0 Output Latch (IRQ0)
6 - 4	Reserved
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-21. System Control Port B (Write)

Bit	Function
7	Parity Check
6	Channel Check
5	Timer 2 Output
4	Toggle with Each Refresh Request
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-22. System Control Port B (Read)

Bit 7 Setting this bit to 1 during a write operation, resets IRQ 0. When this port is read and this bit is set to 1, a parity check has occurred.

Bit 6 When this port is read and this bit is set to 1, a channel check has occurred.

Bit 5 When this port is read, this bit indicates the condition of the timer/counter 2 'output' signal.

Bit 4 When this port is being read, this bit toggles for each refresh request.

Bit 3 Setting this bit to 0 enables channel check. It is set to 1 during a power-on reset.

Bit 2 Setting this bit to 0 enables parity checking. This bit is set to 1 during a power-on reset.

Bit 1 Setting this bit to 1 enables speaker data. This bit is set to 0 during a power-on reset.

Bit 0 Setting this bit to 1 enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7, 6	Fixed Disk Activity Light
5	Reserved
4	Watchdog Timer Status
3	Security Lock Latch
2	Reserved
1	Alternate Gate A20
0	Alternate Hot Reset

Figure 3-23. System Control Port A (Hex 0092)

Bits 7, 6 These bits control the fixed-disk activity light. Setting either bit to 1 turns the fixed-disk activity light on. Setting both bits to 0 turns the light off. The power-on reset condition of each bit is 0.

Bit 5 Reserved.

Bit 4 This read-only bit indicates the Watchdog Timer status. When this bit is set to 1, a Watchdog time-out has occurred. For more information about the Watchdog Timer, refer to the *Hardware Interface Technical Reference.*

Bit 3 This bit provides the security lock for the secured area of RT/CMOS. Setting this bit to 1 electrically locks the 8-byte, power-on password. Once this bit is set by POST, it can only be cleared by turning the system off.

Bit 2 Reserved.

Bit 1 This bit is used to enable the 'address 20' signal (A20) when the microprocessor is in the real address mode. When this bit is set to 0, A20 cannot be used in real mode addressing. This bit is set to 0 during a system reset.

Bit 0 This bit provides an alternate method of resetting the system microprocessor. This alternate method supports operating systems requiring faster operation than was provided on the IBM Personal Computer AT* Resetting the system microprocessor is used to switch the microprocessor from the protected mode to the real address mode. The alternate reset takes 13.4 microseconds.

This bit is set to 0 either by a system reset or a Write operation. When a Write operation changes this bit from 0 to 1, the alternate reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is 0, POST assumes the system was just powered on. If the bit is 1, POST assumes a switch from the protected mode to the real mode has taken place.

---

* Personal Computer AT is a trademark of the International Business Machines Corporation.

Power-On Password

RT/CMOS RAM has 8 bytes reserved for the power-on password and its check character. The 8 bytes are initialized to hex 00. The microprocessor can only access these bytes during power-on self-test (POST). After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by a program. A power-on password can be from 1 to 7 characters.

During power-on password installation, the password (1 to 7 keyboard scan codes), is stored in the security space.

Power-on password installation is a function of a program contained on the Reference diskette. Once the power-on password utility has been installed, the password can be changed only during the POST. When the new power-on password is installed, changed, or removed, the password is not visible on the display.

The system unit cover can be physically locked to prevent unauthorized access to the battery. This helps prevent unauthorized battery removal and loss of power-on password and configuration information.

For information about the keyboard password, see the keyboard/auxiliary device controller information in the *Hardware Interface Technical Reference — Common Interfaces* manual.

Hardware Compatibility

The Model 60 maintains many of the interfaces used by the IBM Personal Computer AT. In most cases command and status organization of these interfaces is maintained.

The functional interfaces for the Personal System/2 products are compatible with the following interfaces:

- The Intel** 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller-address/transfer counters, page registers and status fields only. The Command and Request registers are not supported. The rotate and mask functions are not supported. The Mode register is partially supported.
- The NS16450 serial port.
- The Intel 8088, 8086, and 80286 microprocessors.
- The Intel 8272 diskette drive controller.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The Intel 8042 keyboard port at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.
- Generally compatible with the Intel 80287 and 8087 math coprocessors.

** Intel is a trademark of the Intel Corporation.

** Motorola is a trademark of Motorola, Incorporated.

Index

A

acoustic readings 1-9
activity light, fixed disk 3-22
adapter ID (0000) 3-3
adapter setup 2-4
address maps
  memory 3-8
  POS 2-5
  system 1-6
address space, POS 2-5
alternate reset 3-22
arbiter programming 3-5
arbiter refresh 3-4
arbitration level 3-4
arbitration register 3-5
arbitration, central control point 3-5
A20 gate 3-22

B

base memory bytes 3-19
battery 3-10
block diagram, system board 1-5
bus contention 2-3
bus priority assignments 3-4

C

card selected feedback 2-6
-CD SFDBK 2-6
central arbitration control point 3-5
channel check latch 3-21
CMOS RAM 3-10
configuration CRC bytes 3-19
configuration, RT/CMOS 3-16
connectors, memory 3-9
control ports, system 3-20

D

date century byte 3-19
description, power supply 1-10
diagnostic status byte (RT/CMOS) 3-16
diskette drive enable 2-8
diskette drive type byte 3-17
DMA channels 3-4

E

electrical requirements 1-7
enable I/O functions 2-8
enable NMI 3-11
enable/setup register 2-7
enable, channel check 3-21
equipment byte 3-18
extended arbitration 3-5

F

fault, overvoltage 1-11
features, system 1-4
feedback, card selected 2-6
first fixed disk type byte 3-17
fixed disk drive activity light 1-10
fixed disk drive initialization 3-16
fixed-disk activity light 3-22

G

gate A20 3-22

H

heat output 1-7

I

identification, adapter 3-3
interrupt 0 reset 3-21
interrupts

© Copyright IBM Corp. 1989, 1990

I/O address map 1-6
I/O function byte 2-8

K

keyboard (electrical) 1-7

L

light, fixed disk drive activity 1-10
light, power 1-10

M

map, memory 3-8
math coprocessor 1-4
memory
  connectors 3-9
  control register 2-9
  map 3-8
  memory module packages 3-7
  performance 1-7
  random access 3-7
  read only 3-7
  refresh 1-7
memory refresh 3-4
memory size miscompare 3-16
microprocessor
  alternate reset 3-22
  real address mode 3-22
miscellaneous ports 3-20
mode switch compatibility 3-22
model byte 1-3
modules, memory 3-7

N

NMI mask 3-11
NMI service 3-4
NMI signal 3-4
noise readings 1-9
nonmaskable interrupt (NMI) 3-20

O

output voltage sequencing 1-11
outputs, power supply 1-10
overvoltage fault 1-11

P

parallel port 2-8
parity check enable 3-21
password, power-on 3-23
performance, system 1-7
pointing device (electrical) 1-7
port, system control 3-20, 3-21
POS
  See programmable option select
power specifications (POS) 1-7
power supply description 1-10
power supply LED 1-10
power supply output
  protection 1-11
power supply outputs 1-10
programmable option select 2-3
  enable/setup register 2-7
  registers 2-5
  system board I/O byte 2-8
  system board setup 2-6
  system configuration
    utilities 2-3
programming, arbiter 3-5
protection, power supply 1-11

R

RAM enable 2-9
random access memory (RAM) 3-7
read-only memory 3-7
real mode addressing 3-22
real-time clock bytes 3-13
refresh 3-4, 3-7
refresh request 3-21
registers
  card selected feedback 2-6
  enable/setup 2-7
  memory control 2-9
  miscellaneous system 3-20
  port A 3-21
  port B 3-20
  POS 2-5, 2-8
  RT/CMOS and NMI mask 3-11
  RT/CMOS status registers 3-13

reset, alternate 3-22
RT/CMOS address register 3-11
RT/CMOS RAM 3-10
  password 3-22, 3-23
  secured area 3-22

S

second fixed disk type byte 3-17
sequencing, output voltage 1-11
serial port 2-8
setup
  system board 2-6
  system board I/O byte 2-8
  warning 2-3
shutdown status byte 3-17
size 1-7
sound specifications 1-9
speaker data enable 3-21
specifications 1-7
status registers (RT/CMOS) 3-13
status, watchdog 3-22
switch to real mode 3-22
system address map 1-6
system board
  block diagram 1-5
  features 1-4
  I/O address map 1-6
  I/O byte 2-8
  memory 3-7
  memory connectors 3-9
  memory enable 2-9
  memory map 3-8
  setup 2-4, 2-6
system configuration utilities 2-3
system ports, miscellaneous 3-20
system reset 3-20
system unit specifications 1-7

T

time status indicator 3-16
timer status, watchdog 3-22
type 1 memory connector 3-9

U

utilities, configuration 2-3

V

valid RAM bit 3-15
video subsystem enable/setup 2-7
video subsystem setup 2-4

W

warning, POS 2-3
watchdog status 3-22
weight 1-7

Notes:

Personal System/2
Model 65 SX
Technical Reference

Second Edition (October 1990)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer of express or implied warranties in certain transactions, therefore, this statement may not apply to you.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Requests for technical information about IBM products should be made to your IBM Authorized Dealer or your IBM Marketing Representative.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

© Copyright International Business Machines Corporation 1989, 1990. All rights reserved.

Note to U.S. Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Special Notices

References in this publication to IBM products, programs, or services do not imply that IBM intends to make these available in all countries in which IBM operates. Any reference to an IBM product, program or service is not intended to state or imply that only IBM's product, program, or service may be used. Any functionally equivalent product, program, or service that does not infringe any of IBM's intellectual property rights or other legally protectible rights may be used instead of the IBM product, program, or service. Evaluation and verification of operation in conjunction with other products, programs, or services, except those expressly designated by IBM, are the user's responsibility.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

The following terms, denoted by an asterisk (*) in this publication, are trademarks of the IBM Corporation in the United States and/or other countries:

IBM
Micro Channel
Personal Computer AT
Personal System/2
PS/2

The following terms, denoted by a double asterisk (**) in this publication, are trademarks of other companies as follows:

Intel	Intel Corporation
Motorola	Motorola, Incorporated
National Semiconductor	National Semiconductor Corporation

Preface

This technical reference contains hardware and software interface information specific to the IBM Personal System/2 Model 65 computer. It is intended for those who develop hardware and software products for these systems. Users should understand computer architecture and programming concepts.

This publication consists of the following sections:

Section 1, "System Overview," describes the system, features and specifications.

Section 2, "Programmable Option Select," describes registers used for configuration.

Section 3, "System Board," describes the system specific hardware implementations.

This technical reference should be used with the following publications:

IBM Personal System/2 Hardware Interface Technical Reference — Architectures

IBM Personal System/2 Hardware Interface Technical Reference — Common Interfaces

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference

These publications contain additional information on many of the subjects discussed in this technical reference.

Warning: The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

© Copyright IBM Corp. 1989, 1990

Contents

Section 1. System Overview 1-1
Description 1-3
System-Board Features 1-3
System-Board I/O Address Map 1-5
Specifications 1-6
| Power Supply 1-9
| Outputs 1-9
| Output Protection 1-10
| Power Supply Connectors 1-10

Section 2. Programmable Option Select 2-1
Description 2-3
System-Board POS Address Map 2-5
Card-Selected Feedback 2-5
System-Board Setup 2-6
System-Board Enable/Setup Register (Hex 0094) 2-7
System-Board POS Register 2 (Hex 0102) 2-8
System-Board POS Register 3 (Hex 0103) 2-9
System-Board POS Register 4 (Hex 0104) 2-9
System-Board POS Register 5 (Hex 0105) 2-10
Adapter Setup 2-12

Section 3. System Board 3-1
Description 3-3
Microprocessor and Math Coprocessor 3-3
| Micro Channel Implementation 3-3
| Exception Reporting 3-3
Central Arbiter 3-3
Micro Channel Connectors 3-6
Diskette-Drive Controller 3-6
Memory 3-7
ROM Subsystem 3-7
RAM Subsystem 3-8
Error Recovery 3-9
System-Memory Map 3-9
System-Board Memory Connectors 3-11
RT/CMOS RAM 3-12
Miscellaneous System Functions and Ports 3-22
Nonmaskable Interrupt 3-22
System-Control Port B (Hex 0061) 3-23
System-Control Port A (Hex 0092) 3-24
Power-On Password 3-25

© Copyright IBM Corp. 1989, 1990

Type 2 Serial-Port Controller 3-26
Hardware Compatibility 3-26

Index X-1

Figures

1-1. System-Board Devices and Features 1-4
1-2. System-Board I/O Address Map 1-5
1-3. Performance Specifications 1-6
1-4. Physical Specifications 1-7
1-5. Declared Acoustical Noise Emission Values 1-8
1-6. Component Maximum Current 1-9
1-7. Channel Load Current 1-9
1-8. Voltage Assignments for the Internal Drive Power-Supply Connectors 1-10
2-1. System-Board POS I/O Address Map 2-5
2-2. Card-Selected Feedback Register (Hex 0091) 2-6
2-3. System-Board Enable/Setup Register (Hex 0094) 2-7
2-4. System-Board POS Register 2 (Hex 0102) 2-8
2-5. Parallel-Port Select Bits 2-8
2-6. System-Board POS Register 3 (Hex 0103) 2-9
2-7. System-Board POS Register 4 (Hex 0104) 2-9
2-8. Memory Card ID Bits 2-10
2-9. System-Board POS Register 5 (Hex 0105) 2-10
2-10. Memory-Connector Select for POS Register 4 2-11
2-11. Adapter Enable/Setup Register (Hex 0096) 2-12
3-1. Arbitration-Bus Priority Assignments 3-4
3-2. Arbitration Register, Write to Hex 0090 3-5
3-3. Arbitration Register, Read Hex 0090 3-5
3-4. Diskette-Drive Connector 3-7
3-5. System-Memory Map 3-10
3-6. System-Board Memory Connectors 3-11
3-7. RT/CMOS RAM Address Map 3-12
3-8. RT/CMOS Address and NMI Mask Register (Hex 0070) 3-12
3-9. RT/CMOS Data Register (Hex 0071) 3-13
3-10. Real-Time Clock Bytes 3-14
3-11. Status Register A 3-15
3-12. Status Register B 3-15
3-13. Status Register C 3-16
3-14. Status Register D 3-17
3-15. Diagnostic-Status Byte 3-17
3-16. Diskette-Drive-Type Byte 3-18
3-17. Diskette-Drive-Type Bits (Bits 7-4) 3-18
3-18. Diskette-Drive-Type Bits (Bits 3-0) 3-19
3-19. Equipment Byte 3-19
3-20. Number of Diskette-Drive Bits 3-19
3-21. Display-Operating-Mode Bits 3-20
3-22. System-Control Port B (Write) 3-23

© Copyright IBM Corp. 1989, 1990

3-23. System-Control Port B (Read) 3-23
3-24. System-Control Port A 3-24

Section 1. System Overview

Description 1-3
System-Board Features 1-3
System-Board I/O Address Map 1-5
Specifications 1-6
| Power Supply 1-9
| Outputs 1-9
| Output Protection 1-10
| Voltage Sequencing 1-10
| Power Supply Connectors 1-10

© Copyright IBM Corp. 1989, 1990

Notes:

Description

The IBM* Personal System/2* Model 65 SX computer is a self-contained, floor-standing computer that features the Micro Channel* architecture. The system comes with a keyboard, and can accommodate up to five internal drives, such as two internal diskette drives, two internal fixed disk drives, and a tape drive or CD-ROM.

Programs can identify the system by reading the model and submodel bytes. The model and submodel bytes for the Model 65 SX are:

Byte	Value
Model	F8
Submodel	1C

Interrupt hex 15, function code (AH) = hex C0, returns the model byte, submodel byte, and BIOS revision code.

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* manual for a listing of the model and submodel bytes for other systems, and check the "Supplements" section for updates to that listing.

System-Board Features

The following table lists the system-board devices and features of the Model 65 SX. The Hardware Interface Technical Reference manuals describe devices common to PS/2* products by type number.

* IBM, Personal System/2, PS/2, and Micro Channel are trademarks of the International Business Machines Corporation.

Device	Type	Features
Microprocessor	—	80386SX** 24-bit address and 16-bit data interface
System Timers	1	Channel 0 – System timer Channel 2 – Tone generation for speaker Channel 3 – Watchdog timer
ROM Subsystem	—	128KB (KB = 1024 bytes)
RAM Subsystem	—	1 to 8MB (MB = 1,048,576 bytes) Expandable on the channel
CMOS RAM Subsystem	—	64-byte CMOS RAM with real-time clock/calendar 2KB CMOS RAM extension Battery backup
Video Subsystem	1	Auxiliary connector on the channel Analog output 256KB video memory
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1	Keyboard connector Auxiliary-device connector Password security
Diskette-Drive Controller	1	Supports: - 1.44MB formatted-diskette density - 720KB formatted-diskette density
Serial Controller	2	RS-232C interface Programmable as serial port 1 or 2 FIFO mode* and character mode
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output
Micro Channel	—	Eight channel connectors for Type 3 adpaters: - Seven 16-bit connectors - One 16-bit connector with an auxiliary-video extension
Math Coprocessor Socket	—	Supports 80387SX** math-coprocessor option Same clock speed as the system microprocessor

* The Model 65 SX supports FIFO through ABIOS calls only.

Figure 1-1. System-Board Devices and Features

Additional memory can be added in any available Micro Channel connector; however, the total amount of memory installed must not exceed the 16MB addressing limit.

** 80386SX and 80387SX are trademarks of the Intel Corporation.

System-Board I/O Address Map

Figure 1-2 shows the address map for the various system-board I/O functions.

Address (Hex)	Device
0000 - 001F	DMA Controller (0–3)
0020, 0021	Interrupt Controller (Master)
0040, 0042 - 0044, 0047	System Timers
0060	Keyboard, Auxiliary-Device
0061	System-Control Port B
0064	Keyboard, Auxiliary-Device
0070, 0071	RT/CMOS and NMI Mask
074 - 076	2KB CMOS RAM extension
0081 - 0083, 0087	DMA Page Registers (0–3)
0089 - 008B, 008F	DMA Page Registers (4–7)
0080	Central Arbitration Control Point
0091	Card-Selected Feedback Register
0092	System-Control Port A
0094	System-Board Enable/Setup Register
0096	Adapter Enable/Setup Register
00A0, 00A1	Interrupt Controller (Slave)
00C0 - 00DF	DMA Controller (4–7)
00F0 - 00FF	Math Coprocessor
0100 - 0107	Programmable Option Select
0278 - 027B	Parallel Port 3
02F8 - 02FF	Serial Port 2 (RS-232C)
0378 - 037B	Parallel Port 2
03B4, 03B5, 03BA	Video Subsystem
03BC - 03BF	Parallel Port 1
03C0 - 03C5	Video Subsystem
03C6 - 03C9	Video DAC
03CE, 03CF	Video Subsystem
03D4, 03D5, 03DA	Video Subsystem
03F0 - 03F7	Diskette-Drive Controller
03F8 - 03FF	Serial Port 1 (RS-232C)

Figure 1-2. System-Board I/O Address Map

Specifications

Device	Number of Waits	Cycle Time (ns)
Microprocessor (16 MHz, 62.5 ns Clock)		
Access to System-Board RAM: *		
Memory Read (Page Hit)	0	125
Memory Read (Anticipated Page Miss)	1	187.5
Memory Read (Page Miss)	2	250
Memory Write (Page Hit)	1	187.5
Memory Write (Anticipated Page Miss)	1	187.5
Memory Write (Page Miss)	2	250
Access to Channel:		
Default Transfer Cycle	2	250
Synchronous Transfer Cycle	4	375
Access to ROM	3	312.5
Refresh Rate (typically performed every 15.1 μs)		625 (min)
Bus-Master Access to System Board RAM		300 (min)
DMA Controller (8 MHz, 125 ns Clock):		
Single Transfer: 375 + (I/O Access + Memory Access)		
Burst Transfer: 375 + (I/O Access + Memory Access)N **		
System-Board Memory Access		375
Default Transfer Cycle		250
Synchronous Transfer Cycle		375

* Adapters installed in the channel should not rely on monitoring system board memory access, because channel-memory control signals may not be present during these accesses.
** N is the number of transfers in the burst.

Figure 1-3. Performance Specifications

Note: The cycle times shown for access to system board RAM is based on 85- or 100-nanosecond memory.

Size	
Width	165 mm (6.5 in.)
Depth	483 mm (19.0 in.)
Height	597 mm (23.5 in.)
Weight (with one fixed disk drive)	20.6 kg (45.3 lb)
Cables	
Power Cable	1.8 m (6 ft)
Keyboard Cable	3.05 m (10 ft)
Air Temperature	
System On	10.0 to 35.0°C (50 to 95°F)
System Off	10.0 to 43.0°C (50 to 110°F)
Humidity	
System On	8% to 80%
System Off	8% to 80%
Maximum Altitude	2133.6 m (7000 ft)
Heat Output	390 Watts (1330 BTUs/hour)
Acoustical Readings	(See Figure 1-5 on page 1-8)
Electrical Input:	
Input Voltage (Range is automatically selected; sinewave input is required):	
Low Range	90 (min) – 137 (max) Vac
High Range	180 (min) – 265 (max)Vac
Frequency:	
Low Range	47 (min) – 53 (max) Hz
High Range	57 (min) – 63 (max) Hz
Input in Kilovolt-Ampere (kVA):	
Minimum configuration (as shipped by IBM)	0.10 kVA
Maximum configuration	0.65 kVA
Electromagnetic Compatibility	FCC Class B

Figure 1-4. Physical Specifications

Description	L_{WAd} in bels		L_{pAm} in dB		$<L_{pA}>_m$ in dB	
	Operate	Idle	Operate	Idle	Operate	Idle
Model 65 SX	5.3	5.3	41	40	36	36

Notes:

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

All measurements are made in accordance with ANSI S12.10, and reported in conformance with ISO DIS 9296.

The measurements are preliminary data and subject to change.

Figure 1-5. Declared Acoustical Noise Emission Values

Power Supply

The power supply requires a sinewave input and converts the ac input voltage to three dc output voltages. The power supply provides power for the following:

- System board
- Channel adapters
- Internal DASD drives
- Auxiliary device
- Keyboard.

The power switch and two light-emitting diodes (LEDs) are on the front of the system unit. The green LED indicates that the power supply is operating. The yellow LED indicates fixed disk drive activity.

Outputs

The power supply provides separate voltage sources for the system board and the drives. The system-board voltages are +5 Vdc, +12 Vdc, and −12 Vdc. The drive voltages are +5 Vdc and +12 Vdc. The following is a list of the power provided for each of the components.

System Component	Maximum Current	
	+12 Vdc	+5 Vdc
Internal Fixed Disk Drives (per power supply connector)	2.5 A	1.5 A
Auxiliary Device	None	300 mA
Keyboard	None	275 mA

Figure 1-6. Component Maximum Current

The following are the load currents allowed for each channel connector.

Supply Voltage	Maximum Current
+ 5.0 Vdc	1.6 A
+12.0 Vdc	0.175 A
−12.0 Vdc	0.040 A

Figure 1-7. Channel Load Current

The formulas used to determine the power requirements and the voltage regulation tolerances are in the Micro Channel adapter

| design information in the *Hardware Interface Technical Reference - Architectures* manual.

Output Protection

A short circuit placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state with no damage to the power supply.

If an overvoltage fault occurs (internal to the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of its nominal value.

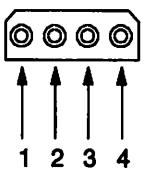
If either of these shutdown states is actuated, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least ten seconds.

Voltage Sequencing

At power-on time, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Power Supply Connectors

The power supply provides two 4-pin connectors for internal fixed disk drives. These connectors can be extended to provide power to more than one internal drive as long as the total power does not exceed the specifications shown in Figure 1-6 on page 1-9.



Pin	Signal
1	+12 Vdc
2	DC Return
3	DC Return
4	+5 Vdc

Figure 1-8. Voltage Assignments for the Internal Drive Power-Supply Connectors

Section 2. Programmable Option Select

Description 2-3
System-Board POS Address Map 2-5
Card-Selected Feedback 2-5
System-Board Setup 2-6
System-Board Enable/Setup Register (Hex 0094) 2-7
System-Board POS Register 2 (Hex 0102) 2-8
System-Board POS Register 3 (Hex 0103) 2-9
System-Board POS Register 4 (Hex 0104) 2-9
4MB Memory Cards 2-10
1MB and 2MB Memory Cards 2-10
System-Board POS Register 5 (Hex 0105) 2-10
Adapter Setup 2-12

© Copyright IBM Corp. 1989, 1990

Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used specifically by the the Model 65 SX system board. For additional POS information, refer to the Hardware Interface Technical Reference Micro Channel architecture information.

Warning:

- IBM recommends that programmable options be set only through the System-Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignments of the same system resource, improper operation of the feature, loss of data, or damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention occurs. When this happens, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System-Board Enable/Setup register (hex 0094) should be set to hex FF.
- The channel-reset bit (bit 7) in the Adapter Enable/Setup register (hex 0096) must be set to 0 to program the adapters.
- The system board does not support 16-bit I/O operations to 8-bit POS registers. Using 16-bit I/O instructions on 8-bit POS registers causes incorrect data to be written to or read from the registers. The system board supports only 8-bit transfers for setup operations.

Setup functions respond to I/O addresses hex 0100 through 0107 only when the setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

System-Board Video Subsystem Setup:

- Bit 5 in the System-Board Enable/Setup register (hex 0094) must be set to 0 to place the system-board video into the setup mode.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 7 in the System-Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system-board functions.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register must be set to 1 to allow adapter setup.
- Bit 5 in the System-Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem.
- Bit 7 in the System-Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to a system-board function.

Other System-Board Setup Requirements:

- Bit 7 in the System-Board Enable/Setup register must be set to 0 to allow setup of other system-board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 5 in the System-Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem.

System-Board POS Address Map

The following table shows the organization of the I/O address space used by system-board POS.

Address (Hex)	Function
0094	System-Board Enable/Setup Register
0096	Adapter Enable/Setup Register
0100	POS Register 0—Reserved
0101	POS Register 1—Reserved
0102	POS Register 2—System-Board I/O Register
0103	POS Register 3—Memory-Enable Register
0104	POS Register 4—Memory-Presence Register
0105	POS Register 5—Memory-Control Register
0106	Reserved
0107	Reserved

Figure 2-1. System-Board POS I/O Address Map

Card-Selected Feedback

Whenever the system addresses an adapter, the adapter responds by setting the '-card-selected feedback' signal (-CD SFDBK) to active. -CD SFDBK is derived from the address decode, driven by a totem-pole driver, and latched by the system board. It can be read through the Card-Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card-Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and determine if the video subsystem, system-board I/O, or an adapter is addressed and functioning.

Bit	Function
7 - 1	Reserved
0	Card-Selected Feedback

Figure 2-2. Card-Selected Feedback Register (Hex 0091)

Bits 7 - 1 Reserved.

Bit 0 This bit is set to 1 whenever -CD SFDBK was active on a previous cycle or whenever the system-board I/O functions (diskette drive, serial, or parallel interfaces) are accessed by an I/O cycle. Reading this register resets the bit to 0.

System-Board Setup

The integrated I/O functions on the system board use POS information during setup. POS treats the diskette-drive controller, serial port, and parallel port as a single device. The video subsystem also is an integrated part of the system board, but POS treats it as a separate device. The System-Board Enable/Setup register is used to place the system board or the video subsystem in the setup mode.

System-Board Enable/Setup Register (Hex 0094)

This is a read/write register. All bits in this register default to 1 (enabled).

Bit	Function
7	Enable/-Setup System-Board Functions
6	Reserved
5	Enable/-Setup Video Subsystem
4 - 0	Reserved

Figure 2-3. System-Board Enable/Setup Register (Hex 0094)

Bit 7 When set to 0, this bit places various system-board I/O functions in the setup mode. The diskette-drive controller, serial port, and parallel port are controlled through System-Board POS Register 2 (hex 0102). The POS information for memory is in System-Board POS Register 3 (hex 0103), POS Register 4 (hex 0104), and POS Register 5 (hex 0105).

When set to 1, this bit enables the system-board functions.

Bit 6 This bit is reserved.

Bit 5 When set to 0, this bit places the video subsystem in the setup mode, and control is through POS Register 2 (hex 0102). When this bit is set to 1 and bit 0 in POS Register 2 is set to 1, video is enabled.

Bit 0 of POS Register 2 is the video-enable bit. When this bit is set to 0, the video subsystem does not respond to commands, addresses, or data. If video is being generated when the video-enable bit is set to 0, the output is still generated. For information on BIOS calls to enable or disable the video, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* manual.

Note: When video is disabled, access to the digital-to-analog converter (DAC) registers is disabled.

Bits 4 - 0 These bits are reserved.

System-Board POS Register 2 (Hex 0102)

When the system board is in the setup mode, this read/write register controls the diskette-drive controller, serial port, and parallel port. Reading this register returns the current state of the following system-board functions.

Bit	Function
7	Disable Parallel-Port Extended Mode
6, 5	Parallel-Port Select
4	Enable Parallel Port
3	Serial-Port Select
2	Enable Serial Port
1	Enable Diskette-Drive Interface
0	Enable System Board

Figure 2-4. System-Board POS Register 2 (Hex 0102)

Bit 7 When set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional interface. When set to 1, this bit disables the bidirectional mode. This bit is set to 0 at power-on time, and the power-on self-test (POST) sets it to 1.

Bits 6, 5 These bits select the configuration of the system-board parallel port.

Bits 6 5	Assignment	Address (Hex)	Interrupt Level
0 0	Parallel 1	03BC - 03BE	7
0 1	Parallel 2	0378 - 037A	7
1 0	Parallel 3	0278 - 027A	7
1 1	Reserved	----------	-

Figure 2-5. Parallel-Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system-board parallel port is enabled.

Bit 3 When set to 1, this bit sets the system-board serial port as Serial 1 (addresses hex 03F8 through 03FF), which uses interrupt level 4. When set to 0, this bit sets the serial port as Serial 2 (addresses hex 02F8 through 02FF), which uses interrupt level 3.

Bit 2 When this bit and bit 0 are set to 1, the system-board serial port is enabled.

Bit 1 When this bit and bit 0 are set to 1, the diskette-drive interface is enabled.

Bit 0 When set to 1, this bit allows bits 4, 2, and 1 to enable and disable their respective devices. When set to 0, this bit disables the system-board parallel port, the system-board serial port, and the diskette-drive interface, regardless of the state of bits 4, 2, and 1.

System-Board POS Register 3 (Hex 0103)

When the system board is in setup mode, this read/write register controls the system-board memory.

Bit	Function
7 - 1	Reserved
0	Enable System-Board RAM

Figure 2-6. System-Board POS Register 3 (Hex 0103)

Bits 7 - 1 These bits are reserved.

Bit 0 When set to 1, this bit enables system-board memory. When set to 0, this bit disables system-board memory. All RAM installed on the system board is enabled or disabled by this operation.

System-Board POS Register 4 (Hex 0104)

The system board has two memory connectors that support 1MB, 2MB, and 4MB memory cards. This read/write register contains information about the memory cards installed. POS Register 5 defines the connector.

Bit	Function
7 - 4	Memory Card ID
3 - 0	Enable Memory Card

Figure 2-7. System-Board POS Register 4 (Hex 0104)

Bits 7 - 4 Bits 7 through 4 provide the memory card ID.

Bits 7654	Size	Speed
0000	4MB	80 ns
0001	2MB	100 ns
0010	1MB	100 ns
0011-0100	Reserved	--
0101	2MB	80 ns
0110	1MB	80 ns
0111-1100	Reserved	--
1101	2MB	120 ns
1110	1MB	120 ns
1111	No memory card installed	--

Figure 2-8. Memory Card ID Bits

4MB Memory Cards

Bits 3 - 0 When set to 1, a 4MB memory card is enabled

1MB and 2MB Memory Cards

Bits 3, 2 Reserved

Bit 1 When set to 1, this bit enables the second 1MB on a 2MB memory card.

Bit 0 When set to 1, this bit enables a 1MB memory card or the first 1MB on a 2MB memory card.

System-Board POS Register 5 (Hex 0105)

This is the memory-control register.

Bit	Function
7, 6	Reserved
5	640KB - 1MB Split Enable
4	ROM Enable
3	Memory-Access Speed
2 - 0	Memory-Connector Select Bit for POS Register 4

Figure 2-9. System-Board POS Register 5 (Hex 0105)

Bits 7, 6 These bits are reserved.

Bit 5 When set to 0, this bit enables the system-board RAM between 640KB and 1MB. Typically, 128KB of this memory is mapped to the system-board ROM address space, and the remaining 256KB is mapped to the first

available address following the last full 1MB block of activated system-board memory. When set to 1, this bit disables system-board RAM between 640KB and 1MB.

Bit 4 This bit determines how addresses hex 0E0000 to 0FFFFF are assigned.

When set to 1, this bit enables ROM; the system assigns the read-access addresses to ROM and the write-access addresses to RAM. When set to 0, this bit disables ROM; the system assigns the read-access addresses to RAM and disables the write-access addresses. Bit 5 of this register must be set to 0 before ROM can be disabled.

Bit 3 When set to 0, this bit sets the memory-access speed to 1, 2, or 3 wait states. When set to 1, this bit sets the memory-access speed to 0, 1, or 2 wait states. This bit is set to 0 by a power-on reset. For more information on memory-access speed, see Figure 1-3 on page 1-6.

Bits 2 - 0 These bits select the memory connector to be used by POS Register 4.

Bits 2 1 0	Function
0 0 0	Memory Connector 1
0 0 1	Memory Connector 2
0 1 0 - 1 1 1	Reserved

Figure 2-10. Memory-Connector Select for POS Register 4

Adapter Setup

The Adapter Enable/Setup register (hex 0096) selects the channel connector to be configured.

Bit	Function
7	Channel Reset
6 - 4	Reserved
3	Card-Setup Enable
2 - 0	Channel Select 2 - 0

Figure 2-11. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6 - 4 These bits are reserved.

Bit 3 When set to 1, this bit enables the '-card setup' signal (-CD SETUP) selected by bits 2 through 0.

Bits 2 - 0 These bits are the address bits for -CD SETUP. Connectors 1 through 8 are addressed as 0 through 8, respectively. When bit 3 is set to 1, these bits select the connector that is put into setup mode.

Associated with each channel connector is a unique '-card setup' signal used to put the adapters in the setup mode, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Notes:

1. -CD SETUP goes active only when an operation is performed in the I/O address range of hex 0100 through 0107.
2. The status of the Adapter Enable/Setup register (hex 0096) can be read by a program. however, when the register is read, bits 6 through 4 are set to 1.

Section 3. System Board

Description 3-3
Microprocessor and Math Coprocessor 3-3
| Micro Channel Implementation 3-3
| Exception Reporting 3-3
Central Arbiter 3-3
Arbitration-Bus Priority Assignments 3-4
Central-Arbiter Programming 3-5
Micro Channel Connectors 3-6
Diskette-Drive Controller 3-6
Memory 3-7
ROM Subsystem 3-7
RAM Subsystem 3-8
Error Recovery 3-9
System-Memory Map 3-9
System-Board Memory Connectors 3-11
RT/CMOS RAM 3-12
RT/CMOS Address and NMI Mask Register (Hex 0070) . . 3-12
RT/CMOS Data Register (Hex 0071) 3-13
RT/CMOS RAM I/O Operations 3-13
Real-Time-Clock Bytes (Hex 000-00D) 3-14
CMOS RAM Configuration 3-17
Miscellaneous System Functions and Ports 3-22
Nonmaskable Interrupt 3-22
System-Control Port B (Hex 0061) 3-23
System-Control Port A (Hex 0092) 3-24
Power-On Password 3-25
Type 2 Serial-Port Controller 3-26
Hardware Compatibility 3-26

© Copyright IBM Corp. 1989, 1990

Notes:

Description

This section describes the microprocessor, math coprocessor, channel differences, memory subsystems, and miscellaneous system ports and connectors for the Model 65 SX. Additional information on these topics can be found in the *Hardware Interface Technical Reference* listed in the preface of this manual.

Microprocessor and Math Coprocessor

The Model 65 SX uses an 80386SX Microprocessor that runs at 16 MHz and has a 24-bit address and a 16-bit data interface. The 80386SX Microprocessor is software compatible with the 80386 Microprocessor.

The 80387SX Math Coprocessor matches the speed of the system microprocessor and operates in the synchronous mode. The 80387SX Math Coprocessor is software compatible with the 80387 Math Coprocessor.

Micro Channel Implementation

This section describes the implementation of the Micro Channel architecture on the Model 65 SX system. For more information, refer to the Hardware Interface Technical Reference Micro Channel architecture information.

Exception Reporting

Exceptions should be reported using the asynchronous channel check procedure. The synchronous channel check procedure is not supported.

Central Arbiter

The central-arbitration control point gives intelligent subsystems on the channel the ability to share and control the system. It allows burst-data transfers and prioritization of control between devices. The central arbiter supports up to 15 arbitrating devices (levels 0 through E) and the system microprocessor (level F).

Arbitration-Bus Priority Assignments

The following figure shows the assignment of arbitration levels. The functions with the lowest arbitration level have the highest priority.

ARB Level	Primary Assignment
-2	Memory Refresh
-1	NMI
0	DMA Channel 0 (Programmable to any arbitration level)
1	DMA Channel 1
2	DMA Channel 2
3	DMA Channel 3
4	DMA Channel 4 (Programmable to any arbitration level)
5	DMA Channel 5
6	DMA Channel 6
7	DMA Channel 7
8 - E	Available
F	System Microprocessor

Figure 3-1. Arbitration-Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so diskette overruns can be prevented or recovered by retry operations. The diskette-drive controller on arbitration level 2 can be held inactive by devices on levels 0 and 1 by a refresh operation, and by the previous controlling master. The diskette-drive controller should not be held inactive for more than 12 microseconds to prevent data overruns.

Nonmaskable-interrupt (NMI) service executes at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal (ARB/-GNT) is in the arbitrate state.

When the central-arbitration control point receives a level -1 request (NMI, a system-board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central-arbitration control point gives the grant to the level -1 request, and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI service is reset.

Central-Arbiter Programming

The central-arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bit definitions are different for read and write operations, as shown in the following tables.

Bit	Definition
7	Enable System-Microprocessor Cycle
6	Arbitration Mask
5	Enable Extended Arbitration (Not Supported)
4 - 0	Reserved

Figure 3-2. Arbitration Register, Write to Hex 0090

Bit	Definition
7	Enable System-Microprocessor Cycle
6	Arbitration Masked by NMI
5	Bus Time-Out
4	Reserved
3 - 0	Value of Arbitration Bus during Previous Grant State

Figure 3-3. Arbitration Register, Read Hex 0090

Bit 7 When set to 1, this bit enables system-microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates system-microprocessor cycles are enabled during arbitration.

Bit 6 When set to 1, this bit causes the central-arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 When set to 1, this bit extends the arbitration cycle from a minimum of 400 nanoseconds to a minimum of 800 nanoseconds. The Model 65 SX does not support this mode of operation. When set to 1, this bit can cause unpredictable results.

Reading this bit as a 1 indicates that a bus time-out has occurred. The bus time-out indication is not reset until bit 6 of this register is set to 0.

Bit 4 This bit is reserved and should be set to 0.

Bits 3 - 0 These bits are undefined for a write operation and should be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Micro Channel Connectors

The Model 65 SX system board provides eight micro channel connectors:

- Seven 16-bit connectors
- One 16-bit connector with an auxiliary-video extension.

Diskette-Drive Controller

The system board uses the Type 1 diskette-drive controller. The following table shows the signal assignments and pin numbering for the 2- by 20-pin connector used in the Model 65 SX.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Drive 2 Installed	2	O	-Reduce Write
3	O	+5 Vdc	4	N/A	-Drive ID
5	N/A	Ground	6	O	+12 Vdc
7	N/A	Ground	8	I	-Index
9	N/A	Ground	10	O	-Motor Enable 0
11	N/A	Ground	12	O	-Drive Select 1
13	N/A	Ground	14	O	-Drive Select 0
15	N/A	Ground	16	O	-Motor Enable 1
17	N/A	Ground	18	O	-Direction
19	N/A	Ground	20	O	-Step
21	N/A	Ground	22	O	-Write Data
23	N/A	Ground	24	O	-Write Enable
25	N/A	Ground	26	I	-Track 0
27	N/A	Ground	28	I	-Write Protect
29	N/A	Ground	30	I	-Read Data
31	N/A	Ground	32	O	-Head 1 Select
33	N/A	Ground	34	I	-Diskette Change
35	N/A	Ground	36	N/A	Ground
37	N/A	+Slim/-Half High	38	O	+5 Vdc
39	N/A	Ground	40	O	+12 Vdc

Figure 3-4. Diskette-Drive Connector

Memory

The Model 65 SX uses the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- Real-time clock and CMOS RAM (RT/CMOS RAM).

ROM Subsystem

The ROM subsystem consists of 128KB. ROM is active at power-on time and is assigned the top of the first and last 1MB of address space (0E0000 to 0FFFFF and FE0000 to FFFFFF). After POST ensures that system memory is operating properly, the ROM code is copied to RAM at the same address space, and ROM is disabled.

The ROM enable bit in System-Board POS Register 5 (hex 0105) controls ROM or RAM access at address space hex 0E0000 to 0FFFFF. When enabled, ROM is not parity-checked and operates with three 62.5-nanosecond wait states.

RAM Subsystem

The RAM subsystem on the system board starts at address hex 000000 of the address space. The RAM subsystem is 18 bits wide: 16 data bits and 2 parity bits. One parity bit is generated for each byte of data written. During a read operation, one parity bit is checked for each byte of data read by the device controlling the bus.

The system board contains two 72-pin memory connectors. Each connector can support 1MB, 2MB, or 4MB of memory. The system enables and disables memory in 1MB blocks. Each 1MB block must start on a 1MB boundary. Because 128KB of I/O ROM, 128KB of system-board ROM, and 128KB of video memory are mapped within the first 1MB of address space, the first physical 1MB of RAM cannot be mapped to contiguous addresses and is therefore split at the 640KB boundary, creating a 384KB overflow. The high 128KB of the overflow is mapped to the system-board ROM address space; the remaining 256KB, called the *split-memory block*, is either disabled or mapped to the first available address following the last full 1MB of activated system-board memory. Split-memory-block remapping and disabling are controlled by System-Board POS Register 5 (hex 0105).

Additional memory can be added in any of the micro channel connectors. The total amount of memory installed must not exceed the 16MB addressing limit. The total amount of usable memory is less than the amount of memory installed because of ROM-to-RAM remapping and split-memory-block remapping.

Error Recovery

If POST detects a memory error in any part of the system-board memory, an attempt is made to deactivate the physical 1MB block of memory that contains the error. The addresses assigned to the deactivated block are reassigned to the next physical block of system-board memory, if installed (the first 1MB of memory-address space cannot be assigned to memory installed in any of the micro channel connectors). If 1MB of valid system-board memory cannot be found, the system sets the memory size according to the last good memory available and allows a system reset; however, if a minimum of 64KB of good memory cannot be found, POST cannot recover from the error.

If the first physical 1MB of memory is disabled, the split-memory block and ROM-to-RAM remap feature will not be enabled.

System-Memory Map

Memory is mapped by System-Board POS Register 5 (hex 0105).

Warning: IBM recommends that programmable options be set only through the System-Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignments of the same system resource, improper operation of the feature, loss of data, or damage to the hardware.

The first 640KB of system-board RAM is mapped starting at address hex 000000. A 256-byte and 1KB portion of this RAM is reserved as BIOS data areas. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* manual for details.

Figure 3-5 on page 3-10 shows the memory map for a properly functioning system. Memory can be mapped differently if POST detects an error in system-board memory or RT/CMOS RAM. In the following figure, the variable *X* represents the number of 1MB blocks of system-board memory starting at or above the hex 100000 boundary. The variable *Y* represents the number of 1MB blocks of addressable memory installed in the channel starting at or above the hex 100000 boundary (*Y* cannot exceed 14.75).

Hex Range	Function
000000 to 09FFFF	640KB System-Board RAM
0A0000 to 0BFFFF	128KB Video RAM
0C0000 to 0DFFFF	Feature ROM/RAM
0E0000 to 0FFFFF	128K System-Board ROM mapped to RAM
100000 to (100000 + XMB)	XMB System-Board RAM
(100000 + XMB) to (100000 + XMB + 256KB)	256KB System-Board RAM (Split-Memory Block)
(100000 + XMB + 256KB) to (100000 + XMB + 256KB + YMB)	YMB Channel RAM
(100000 + XMB + 256KB + YMB) to FDFFFF	Not Used
FE0000 to FFFFFF	128KB System-Board ROM (Same as 0E0000 to 0FFFFF)

Figure 3-5. System-Memory Map

System-Board Memory Connectors

The system board has two 72-pin memory connectors that support 1MB, 2MB, and 4MB memory cards. The following table shows the pin assignments for the connectors.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Ground	37	I/O	Parity Data 1
2	I/O	Data 0	38	I/O	Parity Data 1
3	I/O	Data 0	39	N/A	Ground
4	I/O	Data 1	40	O	CAS 0
5	I/O	Data 1	41	O	CAS 2
6	I/O	Data 2	42	O	CAS 3
7	I/O	Data 2	43	O	CAS 1
8	I/O	Data 3	44	O	RAS 0
9	I/O	Data 3	45	O	RAS 1
10	O	+5 Vdc	46	O	Block Select 1
11	O	-CAS Parity	47	O	Write Enable
12	O	Address 0	48	N/A	Reserved
13	O	Address 1	49	I/O	Data 8
14	O	Address 2	50	I/O	Data 8
15	O	Address 3	51	I/O	Data 9
16	O	Address 4	52	I/O	Data 9
17	O	Address 5	53	I/O	Data 10
18	O	Address 6	54	I/O	Data 10
19	N/A	Reserved	55	I/O	Data 11
20	I/O	Data 4	56	I/O	Data 11
21	I/O	Data 4	57	I/O	Data 12
22	I/O	Data 5	58	I/O	Data 12
23	I/O	Data 5	59	O	+5 Vdc
24	I/O	Data 6	60	I/O	Data 13
25	I/O	Data 6	61	I/O	Data 13
26	I/O	Data 7	62	I/O	Data 14
27	I/O	Data 7	63	I/O	Data 14
28	O	Address 7	64	I/O	Data 15
29	O	Block Select 0	65	I/O	Data 15
30	O	+5 Vdc	66	O	Block Select 2
31	O	Address 8	67	I	Presence Detect 0
32	O	Address 9	68	I	Presence Detect 1
33	O	RAS 3	69	I	Presence Detect 2
34	O	RAS 2	70	I	Presence Detect 3
35	I/O	Parity Data 0	71	O	Block Select 3
36	I/O	Parity Data 0	72	N/A	Ground

RAS = Row Address Strobe
CAS = Column Address Strobe

Figure 3-6. System-Board Memory Connectors

RT/CMOS RAM

The real-time clock/complementary metal-oxide semiconductor RAM (RT/CMOS RAM) chip contains the real-time clock and 64 bytes of CMOS RAM. The clock circuitry uses 14 bytes of this memory, and the rest is allocated to configuration and system-status information.

In addition to the 64 bytes of CMOS RAM, a 2KB CMOS RAM extension is provided for configuration and other system information.

A battery is built into each chip to keep the RT/CMOS RAM and the 2KB CMOS RAM extension active when the power supply is not in operation.

The following table shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000 - 00D	Real-Time-Clock Bytes
00E	Diagnostic-Status Byte
00F	Shutdown-Status Byte
010	Diskette-Drive-Type Byte
011 - 013	Reserved
014	Equipment Byte
015, 016	Low- and High-Base Memory Bytes
017, 018	Low- and High-Expansion Memory Bytes
019 - 031	Reserved
032, 033	Configuration CRC Bytes
034 - 036	Reserved
037	Date-Century Byte
038 - 03F	Reserved

Figure 3-7. RT/CMOS RAM Address Map

RT/CMOS Address and NMI Mask Register (Hex 0070)

This register is used in conjunction with the RT/CMOS Data register (hex 0071) to read from and write to the RT/CMOS RAM bytes.

Bit	Function
7	NMI Mask
6	Reserved
5 - 0	RT/CMOS RAM Address

Figure 3-8. RT/CMOS Address and NMI Mask Register (Hex 0070)

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Bit 7 When this bit is set to 1, the NMI is masked off (disabled). This bit is set to 1 by a power-on reset. This is a write-only bit.

Bit 6 This bit is reserved.

Bits 5 - 0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This register is used in conjunction with the RT/CMOS Address and NMI Mask register (hex 0070) to read from and write to the RT/CMOS RAM bytes.

Bit	Function
7 - 0	RT/CMOS Data

Figure 3-9. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts should be masked to prevent other interrupt routines from changing the RT/CMOS Address register before data is read or written. After I/O operations, the RT/CMOS Address and NMI Mask register (hex 0070) should be left pointing to Status Register D (hex 0D).

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Writing to the RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS Address and NMI Mask register (hex 0070).
2. Write the data to the RT/CMOS Data register (hex 0071).

Reading from the RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Read the data from the RT/CMOS Data register (hex 0071).

Real-Time-Clock Bytes (Hex 000-00D)

Bit definitions and addresses for the real-time-clock bytes are shown in the following table.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second Alarm	1
002	Minutes	2
003	Minute Alarm	3
004	Hours	4
005	Hour Alarm	5
006	Day of Week	6
007	Date of Month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-10. Real-Time Clock Bytes

Note: The Setup program initializes Status Registers A, B, C, and D when the time and date are set. Interrupt hex 1A is the BIOS interface to read and set the time and date, and it initializes the register the same way as the Setup program.

Status Register A (Hex 00A)

Bit	Function
7	Update in Progress
6 - 4	22-Stage Divider
3 - 0	Rate-Selection Bits

Figure 3-11. Status Register A

Bit 7 When set to 1, this bit indicates that the time-update cycle is in progress. When set to 0, it indicates that the current date and time can be read.

Bits 6 - 4 These bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768-kHz time base. This is the only value supported by the system for proper timekeeping.

Bits 3 - 0 These bits allow the selection of a divider output frequency. The system initializes the rate selection bits to a binary 0110, which selects a 1.024-kHz, square-wave output frequency and a 976.562 microsecond periodic-interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Periodic-Interrupt Enable
5	Alarm-Interrupt Enable
4	Update-Ended Interrupt Enabled
3	Square-Wave Enabled
2	Date Mode
1	24-Hour Mode
0	Daylight-Saving Time Enabled

Figure 3-12. Status Register B

Bit 7 When set to 0, this bit updates the cycle, normally by advancing the counts at a rate of one per second. When set to 1, this bit immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This read/write bit allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

Bit 5 When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit indicates whether the binary-coded-decimal (BCD) or binary format is used for time and date calendar updates. When set to 1, this bit indicates the binary format. The system initializes this bit to 0.

Bit 1 This bit indicates if the hours byte is in 12-hour or 24-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When set to 1, this bit enables the daylight-saving-time mode. When set to 0, this bit disables the mode and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt-Request Flag
6	Periodic-Interrupt Flag
5	Alarm-Interrupt Flag
4	Update-Ended-Interrupt Flag
3 - 0	Reserved

Figure 3-13. Status Register C

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When set to 1, this bit indicates that a periodic interrupt occurred.

Bit 5 When set to 1, this bit indicates that an alarm interrupt occurred.

Bit 4 When set to 1, this bit indicates that an update-ended interrupt occurred.

Bits 3 - 0 These bits are reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6 - 0	Reserved

Figure 3-14. Status Register D

Bit 7 This read-only bit monitors the internal battery. When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power.

Bits 6 - 0 These bits are reserved.

CMOS RAM Configuration

The following shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic-Status Byte (Hex 00E)

Bit	Function
7	Real-Time Clock Chip Power
6	Configuration Record and Checksum Status
5	Incorrect Configuration
4	Memory-Size Mismatch
3	Fixed Disk Controller/Drive C Initialization Status
2	Time-Status Indicator
1	Adapter-Configuration Miscompare
0	Adapter-ID Time-Out

Figure 3-15. Diagnostic-Status Byte

Bit 7 When set to 1, this bit indicates that the real-time clock chip lost power.

Bit 6 When set to 1, this bit indicates that the checksum is incorrect.

Bit 5 This is a power-on check of the equipment byte (hex 014). When set to 1, this bit indicates that the configuration information is incorrect.

Bit 4 When set to 1, this bit indicates that the memory size does not match the configuration information.

Bit 3 When set to 1, this bit indicates that the controller or fixed disk drive failed initialization.

Bit 2 When set to 1, this bit indicates that the time is invalid.

Bit 1 When set to 1, this bit indicates that the adapters do not match the configuration information.

Bit 0 When set to 1, this bit indicates that a time-out occurred while an adapter ID was being read.

Shutdown-Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette-Drive-Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7 - 4	First Diskette-Drive Type
3 - 0	Second Diskette-Drive Type

Figure 3-16. Diskette-Drive-Type Byte

Bits 7 - 4 These bits indicate the first diskette-drive type, as shown in the following table.

Bits 7654	Function
0000	No drive present
0001	Double-sided diskette drive (48 tracks per inch, 360KB)
0011	High-capacity diskette drive (720KB)
0100	High-density diskette drive (1.44MB)

Note: All combinations that are not shown are reserved.

Figure 3-17. Diskette-Drive-Type Bits (Bits 7-4)

Bits 3 - 0 These bits indicate the second diskette-drive type, as shown in the following table.

Bits 3 2 1 0	Function
0 0 0 0	No drive present
0 0 0 1	Double-sided diskette drive (48 tracks per inch, 360KB)
0 0 1 1	High-capacity diskette drive (720KB)
0 1 0 0	High-density diskette drive (1.44MB)

Note: All combinations that are not shown are reserved.

Figure 3-18. Diskette-Drive-Type Bits (Bits 3-0)

Reserved Bytes (Hex 011 through 013): These bytes are reserved.

Equipment Byte (Hex 014): This byte defines the basic equipment in the system for the power-on diagnostic tests.

Bit	Function
7, 6	Number of Diskette Drives
5, 4	Display Operating Mode
3, 2	Reserved
1	Math Coprocessor Presence
0	Diskette-Drive Presence

Figure 3-19. Equipment Byte

Bits 7, 6 These bits indicate the number of diskette drives installed, as shown in the following table.

Bits 7 6	Number of Diskette Drives
0 0	One Drive
0 1	Two Drives
1 0	Reserved
1 1	Reserved

Figure 3-20. Number of Diskette-Drive Bits

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port, as shown in the following table.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-Column Mode
1 0	80-Column Mode
1 1	Monochrome Mode

Figure 3-21. Display-Operating-Mode Bits

Bits 3, 2 These bits are reserved.

Bit 1 When set to 1, this bit indicates that a math coprocessor is installed.

Bit 0 When set to 1, this bit indicates that a diskette drive is installed.

Low- and High-Base Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 is equal to 640KB. The low byte is hex 015; the high byte is hex 016.

Low- and High-Expansion Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The hexadecimal values in these bytes represent the number of 1KB blocks of expansion memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 017; the high byte is hex 018.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check (CRC) data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 033; the high byte is hex 032.

Reserved Byte (Hex 034): This byte is reserved.

Low and High Useable Memory Bytes (Hex 035 and 036): These bytes define the total amount of useable memory above the 1MB.

The hexadecimal values in these bytes represent the number of 1KB

| blocks of useable memory. For example, hex 0800 is equal to
| 2048KB. The low byte is hex 35; the high byte is hex 36.

Date-Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* manual for information about reading and setting this byte.

Reserved Bytes (Hex 038 through 03F): These bytes are reserved.

Miscellaneous System Functions and Ports

Nonmaskable Interrupt

The Nonmaskable interrupt (NMI) service signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system watchdog time-out has occurred. The NMI service stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI service masks all other interrupts, and the IRET instruction restores the interrupt flag to the state it was in before the interrupt. A system reset causes a reset of the NMI.

The NMI requests from system-board parity and channel check are subject to mask control with the NMI mask bit in the RT/CMOS Address and NMI Mask register. The watchdog timer and system channel time-out are not masked by this bit. (See "RT/CMOS Address and NMI Mask Register (Hex 0070)" on page 3-12.) The power-on default of the NMI mask is 1 (NMI disabled). Before NMI service is enabled after a power-on reset, the parity-check and channel-check states are initialized by POST.

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System-Control Port B (Hex 0061)

Bit definitions for the write and read functions of this port are shown in the following tables.

Bit	Function
7	Reset Timer 0 Output Latch (IRQ0)
6 - 4	Reserved
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-22. System-Control Port B (Write)

Bit	Function
7	Parity Check
6	Channel Check
5	Timer 2 Output
4	Toggles with Each Refresh Request
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-23. System-Control Port B (Read)

Bit 7 When set to 1 during a write operation, this bit resets IRQ0. When read as a 1, this bit indicates a parity check has occurred.

Bit 6 When read as a 1, this bit indicates a channel check has occurred.

Bit 5 When read, this bit indicates the condition of the timer 2 'output' signal.

Bit 4 When read, this bit toggles for each refresh request.

Bit 3 When set to 0, this bit enables channel check. This bit is set to 1 during a power-on reset.

Bit 2 When set to 0, this bit enables parity check. This bit is set to 1 during a power-on reset.

Bit 1 When set to 1, this bit enables speaker data.

Bit 0 When set to 1, this bit enables the timer 2 gate.

System-Control Port A (Hex 0092)

Bit	Function
7 - 5	Reserved
4	Watchdog-Timer Status
3	Security-Lock Latch
2	Reserved
1	Alternate Gate A20
0	Alternate Hot Reset

Figure 3-24. System-Control Port A

Bits 7 - 5 These bits are reserved.

Bit 4 This read-only bit indicates the watchdog timer status. When this bit is set to 1, a watchdog time-out has occurred. The Hardware Interface Technical Reference manuals contain more information about the Watchdog Timer.

Bit 3 This bit provides the security lock for the secured area of RT/CMOS RAM. When set to 1, this bit electrically locks the 8-byte, power-on password. Once this bit is set by POST, it can be cleared only by turning the system off.

Bit 2 This bit is reserved.

Bit 1 This bit is used to enable the 'address 20' signal (A20) when the microprocessor is in the real-address mode. When this bit is set to 0, A20 cannot be used in real mode addressing. This bit is set to 0 during a system reset.

Bit 0 This bit provides an alternative method of resetting the system microprocessor. This alternative method supports operating systems requiring faster operation than was provided on the IBM Personal Computer AT*. Resetting the system microprocessor switches the microprocessor from the protected mode to the real-address mode. The alternative reset takes 13.4 microseconds.

This bit is set to 0 by either a system reset or a write operation. When a write operation changes this bit from 0 to 1, the alternative-reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch

* Personal Computer AT is a trademark of the International Business Machines Corporation.

remains set so that POST can read this bit. If the bit is set to 0, POST assumes the system was just powered on. If the bit is set to 1, POST assumes a switch from the protected mode to the real mode has taken place.

When bit 0 is used to reset the system microprocessor to the real mode, use the following procedure:

1. Disable all maskable and nonmaskable interrupts.
2. Reset the system microprocessor by writing bit 0 to 1.
3. Issue a Halt instruction to the system microprocessor.

If this procedure is not followed, the results will be unpredictable.

Note: Whenever possible, BIOS or ABIOS should be used as an interface to reset the system microprocessor to the real mode.

Power-On Password

Eight bytes of RT/CMOS RAM are reserved for the power-on password and its check character. The eight bytes are initialized to hex 00. The microprocessor can access these bytes only during POST. After the completion of a POST, if a power-on password is installed, the password bytes are locked and cannot be accessed by a program. The power-on password can be from one to seven characters.

During power-on password installation, the password (1 to 7 keyboard scan codes), is stored in the security space.

Installing the password is a function of a program on the Reference Diskette. The power-on password does not appear on the screen when you install, change, or remove it. Once you install the power-on password, it can be changed only during POST.

The system unit cover can be physically locked to prevent access to the speaker/password security connector.

The Model 65 SX also has a keyboard password. For more information, see the Hardware Interface Technical Reference keyboard and auxiliary-device controller information.

Type 2 Serial-Port Controller

Some Type 2 serial controllers used on the Model 65 SX system board do not respond as described in the Hardware Interface Technical Reference serial controller information.

After the FIFO mode is enabled, bit 6 of the Interrupt Identification register is erroneously set to 0, indicating a Type 1 serial controller is installed. Any application program or operating system that uses bit 6 of the Interrupt Identification register as an indicator to determine FIFO support will default to the character mode. This indicator is ignored by the Model 65 SX ABIOS. Therefore, programs that operate through ABIOS can use the FIFO mode. The ABIOS routines also clear any error indications remaining after a mode change.

Some application programs reset the received-data-ready indication by writing bit 0 of the Line Status register as a 0. This method can cause compatibility problems and is not supported by Type 1 or Type 2 serial controllers. Compatibility problems can be avoided by resetting bit 0 of the Line Status register to 0. This can be accomplished by reading the data and discarding the data if it is not used.

Hardware Compatibility

The Model 65 SX maintains many of the interfaces used by the IBM Personal Computer AT. In most cases command and status organization of these interfaces is maintained.

The functional interfaces for the Model 65 SX are compatible with the following interfaces:

- The Intel** 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller-address/transfer counters, page registers, and status fields only. The Command and Request registers are not supported. The rotate and mask functions are not supported. The Mode register is partially supported.

** Intel is a trademark of the Intel Corporation.

- Generally compatible with the National Semiconductor** NS16550A serial-communications controller.
- The Intel 8088, 8086, 80286, and 80386 microprocessors.
- The Intel 8272 diskette-drive controller. The BIOS limits support to diskette drives that have a 3-millisecond step rate during recalibration.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The Intel 8042 keyboard port at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.
- Generally compatible with the Intel 80387, 80287, and 8087 math coprocessors.

Whenever possible, BIOS or ABIOS should be used as an interface to reset the system microprocessor to the real mode.

The system microprocessor also can be reset to the real mode through bit 0 of port hex 0064 or hex 0092. When using either of these ports, you must perform the following procedure:

1. Disable all maskable and non-maskable interrupts.
2. Reset the system microprocessor.
3. Issue a Halt instruction to the system microprocessor.

If this procedure is not followed, the results will be unpredictable.

** National Semiconductor is a trademark of the National Semiconductor Corporation.

** Motorola is a trademark of Motorola, Incorporated.

Notes:

Index

A

acoustics 1-7, 1-8
adapter
  enable/setup register 2-12
  setup 2-4
address and NMI mask register, RT/CMOS 3-12
address map
  memory 3-9
  POS I/O 2-5
  reassignment 3-9
  system-board I/O 1-5
address 20 gate 3-24
alternate reset 3-24
altitude 1-7
anticipated page miss 1-6
arbiter programming 3-5
arbitration level 3-4
arbitration register 3-5
arbitration-control point 3-3
arbitration, central control point 3-5
audio subsystem 1-4

B

base-memory bytes 3-20
battery 3-17
bus contention 2-3
bus priority assignments 3-4

C

cables 1-7
card setup 2-12
card-selected feedback 2-5
-CD SETUP 2-12
-CD SFDBK 2-5
central-arbitration control point 3-3
channel 3-3
  check enable 3-23
  check latch 3-23
channel *(continued)*
  connector 1-4
  DMA 1-4, 3-4
  reset 2-12
clock, real-time 3-12, 3-14
CMOS RAM 1-4, 3-12—3-22
compatibility 3-26
configuration
  CRC bytes 3-20
  RT/CMOS 3-17
connector
  channel 1-4
  diskette-drive 3-6
  memory 3-11
connectors, micro channel 3-6
contention, bus 2-3
control ports, system 3-23—3-24
controller
  diskette-drive 1-4, 2-8, 3-6
  DMA 1-4
  interrupt 1-4
  keyboard/auxiliary device 1-4
  parallel 1-4
  serial 1-4, 3-26
coprocessor, math 1-4, 3-3
current, electrical 1-7

D

data register, RT/CMOS 3-13
date-century byte 3-21
depth, system unit 1-7
description, power supply 1-9
device types 1-3
diagnostic-status byte (RT/CMOS) 3-17
diskette drive
  connector 3-6
  controller 2-8, 3-6
  type byte 3-18
diskette overruns 3-4
display operating mode 3-20

© Copyright IBM Corp. 1989, 1990

DMA
channels 1-4, 3-4
controller 1-4
performance 1-6

E

electrical specifications 1-7
electromagnetic compatibility 1-7
enable NMI 3-12
equipment byte 3-19
error recovery 3-9
extended arbitration 3-5

F

fault, overvoltage 1-10
feedback, card-selected 2-5
fixed disk drive
initialization 3-17
fixed disk drive activity light 1-9

G

gate A20 3-24

H

hardware compatibility 3-26
heat output 1-7
height, system-unit 1-7
humidity 1-7

I

identifier, model 1-3
interrupt
controller 1-4
IRQ0 reset 3-23
NMI reset 3-22
I/O
address map 1-5
RT/CMOS RAM operations 3-13
system board 2-8

K

keyboard
cable 1-7
password 3-25

L

light, fixed disk drive activity 1-9
light, power 1-9

M

math coprocessor 1-4, 3-3
measurements, system-unit 1-7
memory
bytes 3-20
card ID bits 2-10
connector 3-11
control register 2-10
description 3-7
error recovery 3-9
memory map 3-9
performance 1-6
RAM 3-8
read 1-6
reassigning 3-9
refresh 3-4
ROM 3-7
RT/CMOS RAM 3-12
setup on system board 2-9
size miscompare 3-17
split 2-11
system-memory map 3-9
write 1-6
Micro Channel architecture
arbitration-control point 3-3
bus adapter 1-4
connector 1-4
general information 3-3
micro channel connectors 3-6
microprocessor
alternate reset 3-24
description 3-3
features 1-4
mode switch compatibility 3-24
performance 1-6

microprocessor *(continued)*
real-address mode 3-24
mode switch, protected 3-24
model/submodel bytes 1-3

N

NMI mask register 3-12
NMI service 3-4
NMI signal 3-4
noise readings 1-7
nonmaskable interrupt (NMI) 3-22

O

output voltage sequencing 1-10
outputs, power supply 1-9
overvoltage fault 1-10

P

page hit 1-6
page miss 1-6
parallel port 1-4, 2-8
parity check enable 3-23
password
keyboard 3-25
power-on 3-24, 3-25
performance, system 1-6
port
parallel 1-4, 2-8
serial 1-4, 2-8
system 3-22
POS
See programmable option select (POS)
POST 3-7
power
cable 1-7
loss 3-17
specifications 1-7
supply 1-4, 1-7
power supply description 1-9
power supply LED 1-9
power supply output protection 1-10
power supply outputs 1-9
power-on password 3-24, 3-25
programmable option select (POS)
adapter enable/setup register 2-12
address map 2-5
card-selected feedback register 2-5
description 2-3
setup procedures 2-4
system configuration utilities 2-3, 3-9
system-board enable/setup register 2-7
system-board I/O 2-8
system-board POS registers 2-10
system-board setup 2-6
system-memory map 3-9
video 2-7
warning 2-3, 3-9
programming, arbiter 3-5
protected mode switch 3-24
protection, power supply 1-10

R

RAM (random access memory) 3-8
RAM (random-access memory) 1-4
random access memory (RAM) 3-8
random-access memory (RAM) 1-4
read-only memory (ROM) 1-4, 3-7
real-mode switch 3-24
real-time clock 3-12, 3-14
recovery, error 3-9
refresh 3-4
refresh request 1-6, 3-23
register
adapter enable/setup 2-12
card-selected feedback 2-5
memory control 2-10
miscellaneous system 3-22
RT/CMOS address and NMI mask 3-12
RT/CMOS data 3-13
RT/CMOS status 3-15—3-17
system control 3-23
system-board enable/setup 2-7

register *(continued)*
system-board POS 2-5—2-10
reset, alternative 3-24
ROM enable 2-10
ROM (read-only memory) 1-4, 3-7
RT/CMOS RAM
address and NMI mask register 3-12
address map 3-12
configuration bytes 3-17
data register 3-13
description 3-12
diagnostic-status byte 3-17
I/O operations 3-13
power-on password 3-25
secured area 3-24
status registers 3-15—3-17

S

sequencing, output voltage 1-10
serial port 1-4, 2-8
setup
bus contention 2-3
system-board 2-4, 2-6
system-board I/O 2-8
system-memory map 3-9
video 2-7
shutdown-status byte 3-18
signal
card setup 2-12
card-selected feedback 2-5
channel reset 2-12
size, system unit 1-7
sound levels 1-7
speaker data enable 3-23
specifications
performance 1-6
physical 1-7
status registers
(RT/CMOS) 3-15—3-17
switch to real 3-24
system
configuration utilities 2-3, 3-9
control ports 3-23—3-24
description 1-3
functions, miscellaneous 3-22
system *(continued)*
performance 1-6
reset 3-22
specifications 1-7
timers 1-4
system-board
address map 1-5
description 3-3
enable/setup register 2-7
features 1-3
I/O 2-8
memory connector 3-11
memory register 2-9
model identifier 1-3
POS I/O address map 2-5
POS registers 2-10
setup 2-4, 2-6

T

temperature 1-7
time-status indicator 3-18
timers, system 1-4
type identifier 1-3

U

useable memory count 3-20

V

video
setup 2-7
subsystem 1-4, 2-4
voltage, power supply 1-7

W

warning
arbitration 3-4
central arbiter 3-5
NMI mask 3-22
POS 2-3, 3-9
reserved areas v
RT/CMOS 3-13
watchdog status 3-24
weight, system unit 1-7

width, system unit 1-7

Numerics

2KB CMOS RAM Extension 1-4
80386SX microprocessor 1-4, 1-6, 3-3
80387SX math coprocessor 1-4, 3-3

Notes:

Personal System/2
Model 70
Technical Reference

Fourth Edition (October 1990)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer of express or implied warranties in certain transactions, therefore, this statement may not apply to you.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Requests for technical information about IBM products should be made to your IBM Authorized Dealer or your IBM Marketing Representative.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

© Copyright International Business Machines Corporation 1989, 1990. All rights reserved.

Note to U.S. Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Special Notices

References in this publication to IBM products, programs, or services do not imply that IBM intends to make these available in all countries in which IBM operates. Any reference to an IBM product, program or service is not intended to state or imply that only IBM's product, program, or service may be used. Any functionally equivalent product, program, or service that does not infringe any of IBM's intellectual property rights or other legally protectible rights may be used instead of the IBM product, program, or service. Evaluation and verification of operation in conjunction with other products, programs, or services, except those expressly designated by IBM, are the user's responsibility.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

The following terms, denoted by an asterisk (*) in this publication, are trademarks of the IBM Corporation in the United States and/or other countries:

IBM
Micro Channel
Personal Computer AT
Personal System/2
PS/2

The following terms, denoted by a double asterisk (**) in this publication, are trademarks of other companies as follows:

Intel	Intel Corporation
Motorola	Motorola, Incorporated

Preface

This technical reference contains hardware and software interface information specific to the IBM Personal System/2 Model 70 computer. It is intended for those who develop hardware and software products for these systems. Users should understand computer architecture and programming concepts.

This publication consists of the following sections:

Section 1, "System Overview," describes the system, features, and specifications.

Section 2, "Programmable Option Select," describes the registers used for configuration.

Section 3, "System Board," describes the system-specific hardware implementations.

This technical reference should be used with the following publications:

IBM Personal System/2 Hardware Interface Technical Reference — Architectures

IBM Personal System/2 Hardware Interface Technical Reference — Common Interfaces

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference

These publications contain additional information on many of the subjects discussed in this technical reference.

Warning: The term "Reserved" describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

© Copyright IBM Corp. 1989, 1990

Contents

Section 1. System Overview 1-1
Description 1-3
System Board Features 1-4
System Board I/O Address Map 1-8
Specifications 1-9
Power Supply 1-15
Outputs 1-15
Output Protection 1-16
Voltage Sequencing 1-16

Section 2. Programmable Option Select 2-1
Description 2-3
POS Address Map 2-5
Card Selected Feedback 2-6
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-7
System Board POS Register 2 (Hex 0102) 2-8
System Board POS Register 3 (Hex 0103)—Types 1 and 2 . . 2-10
System Board POS Register 3 (Hex 0103)—Types 3 and 4 . . 2-12
System Board POS Register 4 (Hex 0104)—Types 3 and 4 . . 2-13
Memory Presence Detect 2-14
Adapter Enable/Setup Register (Hex 0096) 2-15

Section 3. System Board 3-1
Description 3-3
80387 Math Coprocessor 3-3
Micro Channel Implementation 3-3
Exception Reporting 3-3
Matched-Memory 3-3
Central Arbiter 3-6
Diskette Drive and Fixed Disk Connectors 3-9
Memory 3-14
Read-Only Memory Subsystem 3-14
Random Access Memory Subsystem 3-15
System and Nonsystem Memory 3-15
Memory Caching 3-16
Error Recovery 3-18
Memory Subsystem Control 3-19
System Memory Maps 3-24
System Board Memory Connectors 3-29
Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM 3-31

© Copyright IBM Corp. 1989, 1990

Miscellaneous System Functions 3-43
Nonmaskable Interrupt 3-43
System Control Port B (Hex 0061) 3-43
System Control Port A (Hex 0092) 3-45
Power-On Password 3-47
Hardware Compatibility 3-48
Error Codes 3-49

Index X-1

Figures

1-1. Model and Submodel Bytes 1-4
1-2. System Board Devices and Features—Types 1 and 2 . . 1-5
1-3. System Board Devices and Features—Type 3 1-6
1-4. System Board Devices and Features—Type 4 1-7
1-5. System Board I/O Address Map 1-8
1-6. Performance Specifications—Type 1 1-9
1-7. Performance Specifications—Type 2 1-10
1-8. Performance Specifications—Type 3 1-11
1-9. Performance Specifications—Type 4 1-12
1-10. Physical Specifications 1-13
1-11. Acoustical Readings 1-14
1-12. Component Maximum Current 1-15
1-13. Channel Load Current 1-15
2-1. POS I/O Address Map 2-5
2-2. Card Selected Feedback Register (Hex 0091) 2-6
2-3. System Board Enable/Setup Register (Hex 0094) 2-7
2-4. System Board POS Register 2 (Hex 0102) 2-8
2-5. Parallel Port Select Bits 2-8
2-6. System Board POS Register 3 (Read-Only)—Types 1 and 2 2-10
2-7. System Board POS Register 3 (Write-Access)—Types 1 and 2 2-11
2-8. Read Port with Bit 2 Set to 0 2-11
2-9. Read Port with Bit 2 Set to 1 2-11
2-10. System Board POS Register 3 (Hex 0103)—Types 3 and 4 2-12
2-11. System Board POS Register 4 (Hex 0104)—Types 3 and 4 2-13
2-12. Presence Detect Bits 2-14
2-13. Adapter Enable/Setup Register (Hex 0096) 2-15
3-1. Matched-Memory Extension Voltage and Signal Assignments 3-4
3-2. Arbitration Bus Priority Assignments 3-6
3-3. Arbitration Register (Hex 0090)—Write 3-7
3-4. Arbitration Register (Hex 0090)—Read 3-7
3-5. Direct Bus Attachment 3-10
3-6. Diskette Drive Connectors 3-12
3-7. Fixed Disk Drive Connector 3-13
3-8. Mapping of the First 32MB Segment 3-16
3-9. Memory Error Address Reassignment 3-18
3-10. Memory Encoding Register 1 (Hex 00E1) 3-19
3-11. Memory Encoding Register 2 (Hex 00E0) 3-21

© Copyright IBM Corp. 1989, 1990

3-12. Memory Encoding Register 3 (Hex 00E2) – Types 3 and 4 3-22
3-13. System Memory Map 1 3-24
3-14. System Memory Map 2 3-25
3-15. System Memory Map 3 3-25
3-16. System Memory Map 4 3-26
3-17. System Memory Map 5 3-26
3-18. System Memory Map 6 3-27
3-19. System Memory Map 7 3-27
3-20. System Memory Map 8 3-28
3-21. System Board Memory Connector 3-30
3-22. RT/CMOS RAM Address Map 3-31
3-23. RT/CMOS Address Register and NMI Mask (Hex 0070) 3-32
3-24. RT/CMOS Data Register (Hex 0071) 3-32
3-25. Real-Time Clock Bytes 3-34
3-26. Status Register A 3-35
3-27. Status Register B 3-35
3-28. Status Register C 3-37
3-29. Status Register D 3-37
3-30. Diagnostic Status Byte 3-38
3-31. Diskette Drive Type Byte 3-39
3-32. Diskette Drive Type Byte (Bits 7 - 4) 3-39
3-33. Diskette Drive Type Byte (Bits 3 - 0) 3-39
3-34. Equipment Byte 3-41
3-35. Equipment Byte (Bits 7, 6) 3-41
3-36. Equipment Byte (Bits 5, 4) 3-41
3-37. System Control Port B (Write) 3-44
3-38. System Control Port B (Read) 3-44
3-39. System Control Port A 3-45
3-40. POST Error Message Table 3-49

Section 1. System Overview

Description 1-3
System Board Features 1-4
System Board I/O Address Map 1-8
Specifications 1-9
| Power Supply 1-15
| Outputs 1-15
| Output Protection 1-16
| Voltage Sequencing 1-16

© Copyright IBM Corp. 1989, 1990

Notes:

Description

The IBM* Personal System/2* Model 70 computer is a self-contained, desktop computer that features the Micro Channel* architecture. This system can support two diskette drives and one internal fixed disk drive and comes with a keyboard.

A system can have either a Type 1, Type 2, Type 3, or Type 4 system board. The major differences among the four system boards are system clock speed, component layout, and memory. In addition, the Type 3 and Type 4 system boards have the following features.

The Type 3 system board:

- Uses a two-way, set-associative, store-through, 64KB (KB = 1,024 bytes) cache for instructions and data.
- Has the microprocessor, math coprocessor, cache, and cache controller mounted on a processor card that attaches to the system board.
- Has four connectors for system board memory.

The Type 4 system board:

- Uses the Intel 80486 microprocessor, which includes an internal 8KB, 4-way set-associative cache and an internal numeric coprocessor on a processor card.
- Has four connectors for system board memory.

* IBM, Personal System/2, and Micro Channel are trademarks of the International Business Machines Corporation.

Programs identify the type of system board by reading the model and submodel bytes. Interrupt hex 15, function code (AH) = hex C0, returns the model and submodel bytes. The following table shows these bytes, system board types, and system clock speeds.

Model Byte	Submodel Byte	System Board	System Clock/Microprocessor
F8	09	Type 1	16 MHz/80386
F8	04	Type 2	20 MHz/80386
F8	0D	Type 3	25 MHz/80386
F8	1B	Type 4	25 MHz/80486

Figure 1-1. Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems, and check the supplements section for updates to that listing.

System Board Features

The following tables list the system board devices and features. The *Hardware Interface Technical Reference* manuals describe devices common to PS/2* products by type number.

* PS/2 is a trademark of the International Business Machines Corporation.

Device	Type	Features
Microprocessor	---	80386 32-bit address and 32-bit data interface
System Timers	1	Channel 0 – System timer Channel 2 – Tone generation for speaker Channel 3 – Watchdog timer
ROM Subsystem	---	128KB (KB = 1024 bytes)
RAM Subsystem	---	1 to 6MB on the system board (MB = 1,048,576 bytes) Expandable on the channel
CMOS RAM Subsystem	---	64-byte CMOS RAM with real-time clock/calendar 2KB CMOS RAM extension Battery backup
Video Subsystem	1	Auxiliary connector on the channel Analog output 256KB video memory
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal.
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1, 2	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	1	Supports: - 720KB formatted diskette density - 1.44MB formatted diskette density
Serial Controller	2	RS-232C interface Programmable as serial port 1 or 2 FIFO mode and character mode
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output
Micro Channel	---	Three channel connectors for Type 3 adapters : - One 16-bit connector with an auxiliary video extension - Two 32-bit connectors with matched-memory extension
Math Coprocessor Socket	---	Supports 80387 Math Coprocessor Same clock speed as the system microprocessor
Power Supply	1	110 and 220 Vac support

Figure 1-2. System Board Devices and Features – Types 1 and 2

Device	Type	Features
Microprocessor	—	80386 32-bit address and 32-bit data interface
Microprocessor Cache	—	82385 Cache Controller 64KB of static-RAM cache
System Timers	1	Channel 0 — System timer Channel 2 — Tone generation for speaker Channel 3 — Watchdog timer
ROM Subsystem	—	128KB
RAM Subsystem	—	2 to 8MB on the system board Expandable on the channel
CMOS RAM Subsystem	—	64-byte CMOS RAM with real-time clock/calendar 2KB CMOS RAM extension Battery backup
Video Subsystem	1	Auxiliary connector on the channel Analog output 256KB video memory
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	1	Supports: - 720KB formatted diskette density - 1.44MB formatted diskette density
Serial Controller	2	RS-232C interface Programmable as serial port 1 or 2 FIFO mode and character mode
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output
Micro Channel	—	Three channel connectors for Type 3 adapters: - One 16-bit connector with an auxiliary video extension - Two 32-bit connectors with matched-memory extension.
Math Coprocessor Socket	—	Supports 80387 Math Coprocessor Same clock speed as the system microprocessor

Figure 1-3. System Board Devices and Features — Type 3

Device	Type	Features
Microprocessor	—	80486 at 25 MHz 32-bit address and 32-bit data interface
Microprocessor Cache	—	8KB internal cache 4-way set associative
Math Coprocessor	—	Internal floating point coprocessor 80387 compatible No optional math coprocessor
System Timers	1	Channel 0 – System timer Channel 2 – Tone generation for speaker Channel 3 – Watchdog timer
ROM Subsystem	—	128KB
RAM Subsystem	—	2 to 8MB on the system board Expandable on the channel
CMOS RAM Subsystem	—	64-byte CMOS RAM with real-time clock/calendar 2KB CMOS RAM extension Battery backup
Video Subsystem	1	Auxiliary connector on the channel Analog output 256KB video memory
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	1	Supports: - 720KB formatted diskette density - 1.44MB formatted diskette density
Serial Controller	2	RS-232C interface Programmable as serial port 1 or 2 FIFO mode and character mode
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output
Micro Channel	—	Three channel connectors for Type 3 adapters: - One 16-bit connector with an auxiliary video extension - Two 32-bit connectors with matched-memory extension

Figure 1-4. System Board Devices and Features – Type 4

System Board I/O Address Map

Hex Addresses	Device
0000 - 001F	DMA Controller (0–3)
0020, 0021	Interrupt Controller (Master)
0040, 0042 - 0044, 0047	System Timers
0060	Keyboard, Auxiliary Device
0061	System Control Port B
0064	Keyboard, Auxiliary Device
0070, 0071	RT/CMOS and NMI Mask
0081 - 0083, 0087	DMA Page Registers (0–3)
0089 - 008B, 008F	DMA Page Registers (4–7)
0090	Central Arbitration Control Point
0091	Card Selected Feedback Register
0092	System Control Port A
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
00A0 - 00A1	Interrupt Controller (Slave)
00C0 - 00DF	DMA Controller (4–7)
00E0 - 00E2	Memory Encoding Registers
00F0 - 00FF	Math Coprocessor
0100 - 0107	Programmable Option Select
01F0 - 01F8	Fixed Disk Drive Controller
0278 - 027B	Parallel Port 3
02F8 - 02FF	Serial Port 2 (RS-232C)
0378 - 037B	Parallel Port 2
03B4, 03B5, 03BA	Video Subsystem
03BC - 03BF	Parallel Port 1
03C0 - 03C5	Video Subsystem
03C6 - 03C9	Video DAC
03CA, 03CC, 03CE, 03CF	Video Subsystem
03D4, 03D5, 03DA	Video Subsystem
03F0 - 03F7	Diskette Drive Controller
03F8 - 03FF	Serial Port 1 (RS-232C)

Figure 1-5. System Board I/O Address Map

Specifications

Device	Number of Waits	Cycle Time (ns)
Microprocessor (16 MHz – 62.5 ns Clock):		
Access to System Board RAM: *		
Memory Read (Page Hit)	0	125
Memory Read (Page Miss)	2	250
Memory Write (Page Hit)	1	187.5
Memory Write (Page Miss)	2	250
Access to Channel:		
Default Transfer Cycle	2	250
Synchronous Extended Transfer Cycle	4	375
Refresh Rate (Typically performed every 15.1 μs)		625 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (8 MHz – 125 ns Clock):		
Single Transfer: 375 + I/O Access + Memory Access		
Burst Transfers: 375 + (I/O Access + Memory Access)N **		
System Board Memory Access		375
Default Transfer Cycle		250
Synchronous Extended Transfer Cycle		375

* Adapters installed in the channel should not rely on monitoring system board memory accesses because channel memory control signals may not be present during these accesses.

** N is the number of transfers in the burst.

Figure 1-6. Performance Specifications – Type 1

Device	Number of Waits	Cycle Time (ns)
Microprocessor (20 MHz – 50 ns Clock):		
Access to System Board RAM: *		
Memory Read (Page Hit)	0	100
Memory Read (Page Miss)	2	200
Memory Write (Page Hit)	1	150
Memory Write (Page Miss)	2	200
Access to Channel:		
Default Transfer Cycle	2	200
Synchronous Extended Transfer Cycle	4	300
Refresh Rate (Typically performed every 15.1 μs)		500 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer: 300 + I/O Access + Memory Access		
Burst Transfers: 300 + (I/O Access + Memory Access)N **		
System Board Memory Access		300
Default Transfer Cycle		200
Synchronous Extended Transfer Cycle		300

* Adapters installed in the channel should not rely on monitoring system board memory accesses because channel memory control signals may not be present during these accesses.

** N is the number of transfers in the burst.

Figure 1-7. Performance Specifications – Type 2

Device	Number of Waits	Cycle Time (ns)
Microprocessor (25 MHz – 40 ns Clock):		
Access to System Board RAM: *		
Memory Read (Cache Hit)	0	80
Memory Write (Cache Hit)	0	80**
Memory Read (Cache Miss, Page Hit)	0 - 2	80 - 160
Memory Write (Cache Miss, Page Hit)	1	80**
Memory Read (Cache Miss, Page Miss)	3 - 5	200 - 280
Memory Write (Cache Miss, Page Miss)	0	80**
Access to Channel:		
Default Transfer Cycle	4	240
Synchronous Extended Transfer Cycle	7	360
Refresh Rate (Typically performed every 15.1 μs)		600 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer: 300 + I/O Access + Memory Access		
Burst Transfers: 300 + (I/O Access + Memory Access)N ***		
System Board Memory Access		300
Default Transfer Cycle		200
Synchronous Extended Transfer Cycle		300

* Adapters installed in the channel should not rely on monitoring system board memory accesses because channel memory control signals may not be present during these accesses.

** The write operation is buffered outside the microprocessor. Additional time is required if another write operation or read operation with a cache-miss occurs before the write operation is completed.

*** N is the number of transfers in the burst.

Figure 1-8. Performance Specifications – Type 3

Device	Number of Waits	Cycle Time (ns)
Microprocessor (25 MHz – 40 ns Clock):		
Internal 80486 Cache Hits: *		
Access to System Board RAM: *		
Memory Read	0	40
Memory Write	0	40**
Memory Read (Page Hit)		400***
Memory Write (Page Hit)	4	240**
Memory Read (Page Miss)		520***
Memory Write (Page Miss)	5	280**
Access to Channel:		
Default Transfer Cycle	6	320
Synchronous Extended Transfer Cycle	9	440
Refresh Rate (Typically performed every 15.1 μs)		200 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer: 300 + I/O Access + Memory Access		
Burst Transfers: 300 + (I/O Access + Memory Access)N ****		
System Board Memory Access		300
Default Transfer Cycle		200
Synchronous Extended Transfer Cycle		300

* Adapters installed in the channel should not rely on monitoring system board memory accesses because channel memory control signals may not be present during these accesses.

** The memory write is buffered internally. The 80486 contains a four-deep write-through buffer (refer to the Intel specifications for more information). Additional time is required if another write operation or a read operation with a cache-miss occurs before the write operation is completed.

*** The 80486 bus cycle is nonpipelined, and always fetches a 16-byte line from cacheable memory space. The number of clock cycles for memory read with a cache miss:

- If page hit on first access, 4–2–2–2
- If page miss on first access, 7–2–2–2.

**** N is the number of transfers in the burst.

Figure 1-9. Performance Specifications – Type 4

Size:	
Width	360 mm (14.1 in)
Depth	420 mm (16.5 in)
Height	140 mm (5.5 in)
Weight	9.55 kg (21 lb)
Cables:	
Power Cable	1.8 m (6 ft)
Keyboard Cable	1.8 m (6 ft)
Air Temperature:	
System On	15.6 to 32.2°C (60 to 90°F)
System Off	10.0 to 43.0°C (50 to 110°F)
Humidity:	
System On	8% to 80%
System Off	8% to 80%
Maximum Altitude	2133.6 m (7000 ft)
Heat Output	215 Watts (735 BTUs per hour)
Acoustical Readings	(See Figure 1-11 on page 1-14)
Electrical Input:	
Input Voltage (Range is automatically selected; sinewave input is required):	
Low Range	90 (min) – 137 (max) Vac
High Range	180 (min) – 265 (max)Vac
Frequency:	
Low Range	47 (min) – 53 (max) Hz
High Range	57 (min) – 63 (max) Hz
Input in Kilovolt-Ampere (kVA):	
Minimum configuration (as shipped by IBM)	0.13 kVA
Maximum configuration	0.36 kVA
Electromagnetic Compatibility	
FCC Class B	

Figure 1-10. Physical Specifications

Description	L_{WAd} in bels Operate	Idle	L_{pAm} in dB Operate	Idle	$<L_{pA}>_m$ in dB Operate	Idle
Model 70	5.3	5.3	43	43	40	40

Notes:

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

All measurements made in accordance with ANSI S12.10, and reported in conformance with ISO DIS 9296.

The measurements are preliminary data and subject to change.

Figure 1-11. Acoustical Readings

Power Supply

The power supply requires a sineware input and converts the ac input voltage to three dc output voltages. The power supply provides power for the following:

- System board
- Channel adapters
- Internal diskette drives
- Internal fixed disk drive
- Auxiliary device
- Keyboard.

The power switch and one light-emitting diode (LED) are on the front of the system unit. The power supply is operating when the LED is lit.

Outputs

The power supply provides separate voltage sources for the system board and the drives. The system-board voltages are +5 Vdc, +12 Vdc, and −12 Vdc. The drive voltages are +5 Vdc and +12 Vdc. The following is a list of the approximate power provided for system components.

System Component	Maximum Current	
	+12 Vdc	+5 Vdc
Auxiliary Device	None	300 mA
Keyboard	None	275 mA

Figure 1-12. Component Maximum Current

The following are the load currents allowed for each channel connector.

Supply Voltage	16-Bit Connector Maximum Current	32-Bit Connector Maximum Current
+ 5.0 Vdc	1.6 A	2.0 A
+12.0 Vdc	0.175 A	0.175 A
−12.0 Vdc	0.040 A	0.040 A

Figure 1-13. Channel Load Current

The formulas used to determine the power requirements and the voltage regulation tolerances are in the Micro Channel adapter design information in the *Hardware Interface Technical Reference - Architectures* manual.

Output Protection

A short circuit placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state with no damage to the power supply.

If an overvoltage fault occurs (internal to the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of its nominal value.

If either of these shutdown states is actuated, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least ten seconds.

Voltage Sequencing

At power-on time, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Section 2. Programmable Option Select

Description 2-3
POS Address Map 2-5
Card Selected Feedback 2-6
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-7
System Board POS Register 2 (Hex 0102) 2-8
System Board POS Register 3 (Hex 0103) – Types 1 and 2 . . 2-10
POS Register 3 as a Read-Only Port 2-10
POS Register 3 as a Read/Write Port 2-11
System Board POS Register 3 (Hex 0103) – Types 3 and 4 . . 2-12
System Board POS Register 4 (Hex 0104) – Types 3 and 4 . . 2-13
Memory Presence Detect 2-14
Adapter Enable/Setup Register (Hex 0096) 2-15

© Copyright IBM Corp. 1989, 1990

Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used on the Model 70 system boards. For additional POS information, refer to the Hardware Interface Technical Reference Micro Channel architecture information.

Warning:

- IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignment of the same system resource, improper operation of the feature, loss of data, or possible damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention will occur, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- Bit 7 (channel reset) in the Adapter Enable/Setup register must be 0 to program the adapters.
- Only 8-bit instructions are supported for setup operations. Using 32- or 16-bit I/O instructions on 8-bit POS registers will cause erroneous data to be written or read.

Setup functions respond to I/O addresses hex 0100 through 0107 only when their unique setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

System Board Video Subsystem Setup:

- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 0 to place the system board video into the setup mode.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 7 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system board functions.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register must be set to 1 to allow adapter setup.
- Bit 5 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the Video Subsystem.
- Bit 7 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to a system board function.

Other System Board Setup:

- Bit 7 in the System Board Enable/Setup register must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 5 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the Video Subsystem.

POS Address Map

The following table shows the organization of the I/O address space used by POS. Bit 0 of POS Register 2 and bits 6 and 7 of POS Register 5 are fixed. All other bits in POS Registers 2 through 5 are free-form.

Address (Hex)	Function
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
0100	POS Register 0—Adapter Identification Byte (Low Byte)
0101	POS Register 1—Adapter Identification Byte (High Byte)
0102	POS Register 2—Option Select Data Byte 1 Bit 0 is Card Enable.
0103	POS Register 3—Option Select Data Byte 2
0104	POS Register 4—Option Select Data Byte 3
0105	POS Register 5—Option Select Data Byte 4 Bit 7 is the channel check active indicator Bit 6 is the channel check status-available indicator
0106	POS Register 6—Reserved
0107	POS Register 7—Reserved

Figure 2-1. POS I/O Address Map

Card Selected Feedback

When an adapter is addressed, it responds by setting the '-card selected feedback' signal (-CD SFDBK) to active. -CD SFDBK is derived from the address decode and driven by a totem pole driver. It is latched by the system board and can be read through the Card Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and thereby determine if the video subsystem, system board I/O, or an adapter is addressed and functioning.

Bit	Function
7 - 1	Reserved
0	-Card Selected Feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7 - 1 These bits are reserved.

Bit 0 This bit is set to 1 whenever -CD SFDBK was active on a previous cycle or whenever the system board I/O functions (diskette drive, serial, or parallel interfaces) are accessed by an I/O cycle. Reading this register resets the bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information during setup. The diskette drive controller, serial port, and parallel port are treated as a single device. The video subsystem is also an integrated part of the system board; however, POS treats it as a separate device. The System Board Enable/Setup register is used to place the system board or the video subsystem into the setup mode.

System Board Enable/Setup Register (Hex 0094)

This is a read/write register; all bits in this register default to 1 (enabled).

Bit	Function
7	Enable/-Setup System Board Functions
6	Reserved
5	Enable/-Setup Video Subsystem
4 - 0	Reserved

Figure 2-3. System Board Enable/Setup Register (Hex 0094)

Bit 7 When this bit is set to 0, various system board I/O functions are placed in the setup mode. The diskette drive controller, serial port, and parallel port are controlled through System Board POS Register 2 (hex 0102).

When this bit is set to 1, the system board function is enabled.

Bit 6 This bit is reserved.

Bit 5 When this bit is set to 0, the video subsystem is placed in the setup mode and controlled through POS Register 2 (hex 0102). When set to 1, and bit 0 in hex 0102 is set to 1, video is enabled.

Bit 0 of POS Register 2 is the video enable bit. When this bit is set to 0, the video subsystem does not respond to commands, addresses, or data. If video is being generated when the video enable bit is set to 0, the output is still generated. For information on BIOS calls to enable or disable the video, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Note: When video is disabled, access to the video DAC registers is disabled.

Bits 4 - 0 These bits are reserved.

System Board POS Register 2 (Hex 0102)

When the system board is in the setup mode, the diskette drive controller, serial port, and parallel port are controlled by this read/write register. Reading this register returns the current state of these system board functions.

Bit	Function
7	Disable Parallel Port Extended Mode
6, 5	Parallel Port Select
4	Enable Parallel Port
3	Serial Port Select
2	Enable Serial Port
1	Enable Diskette Drive Interface
0	Enable System Board

Figure 2-4. System Board POS Register 2 (Hex 0102)

Bit 7 When set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional interface. When set to 1, this bit disables the bidirectional mode. This bit is set to 0 at power-on and POST sets it to 1.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Hex Address	Interrupt Level
0 0	Parallel 1	03BC - 03BF	7
0 1	Parallel 2	0378 - 037B	7
1 0	Parallel 3	0278 - 027B	7
1 1	Reserved	----------	-

Figure 2-5. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bit 3 When set to 1, this bit sets the system board serial port as Serial 1 (addresses hex 03F8 through 03FF), which uses interrupt level 4. When set to 0, this bit sets the serial port as Serial 2 (addresses hex 02F8 through 02FF), which uses interrupt level 3.

Bit 2 When this bit and bit 0 are set to 1, the system board serial port is enabled.

Bit 1 When this bit and bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When set to 1, this bit allows bits 4, 2, and 1 to enable and disable their respective devices. When set to 0, this bit disables the diskette drive interface, system board serial port, and system board parallel port, regardless of the state of bits 4, 2, and 1.

System Board POS Register 3 (Hex 0103) – Types 1 and 2

This port contains information about the presence and type of memory card installed in each system board memory connector of Type 1 and Type 2 system boards.

How this information is stored and retrieved depends on whether the port is read-only or read/write. To determine the type of port, with a memory card in connector 1, set bit 2 of port hex 103 to 1, and then read port hex 103. If bit 0 of this byte is 0, the port is read-only (connector 1 card present); if bit 0 is 1, the port is read/write (the reserved bit is read as 1).

POS Register 3 as a Read-Only Port
For these systems, the memory connectors are numbered from left to right as viewed from the front of the system.

Bit	Function
7	Reserved
6	2MB/-1MB Card, Connector 3
5	-Card Present, Connector 3
4	Reserved
3	2MB/-1MB Card, Connector 2
2	-Card Present, Connector 2
1	2MB/-1MB Card, Connector 1
0	-Card Present, Connector 1

Figure 2-6. System Board POS Register 3 (Read-Only) – Types 1 and 2

Bits 7, 4 These bits are reserved.

Bits 6, 3, 1 Each bit indicates the type of memory card installed. When set to 1, the bit indicates that the card is a 2MB memory card. When set to 0, the bit indicates that the card is a 1MB memory card.

Bits 5, 2, 0 When set to 0, each bit indicates that a memory card is installed.

POS Register 3 as a Read/Write Port

For these systems, the memory connectors are numbered from right to left as viewed from the front of the system.

Bit	Function
7 - 3	Reserved
2	-Connector 1 and 2
1, 0	Reserved

Figure 2-7. System Board POS Register 3 (Write-Access) — Types 1 and 2

Bits 7 - 3 These bits are reserved.

Bit 2 This bit selects the connector information returned when port hex 0103 is read. When this bit is set to 0, the information for connectors 1 and 2 is shown. This bit is write only.

Bits 1, 0 These bits are reserved.

Bits	Function
7 - 4	Presence Detect 3 - 0, Connector 1
3 - 0	Presence Detect 3 - 0, Connector 2

Figure 2-8. Read Port with Bit 2 Set to 0

When bit 2 is set to 1, connector 3 information is shown.

Bits	Function
7 - 4	Presence Detect 3 - 0, Connector 3
3 - 0	Reserved

Figure 2-9. Read Port with Bit 2 Set to 1

Each set of four bits shows the state of the presence detect signals for that connector (see Figure 2-12 on page 2-14 for more information).

System Board POS Register 3 (Hex 0103) – Types 3 and 4

On the Type 3 and Type 4 system boards, two read-only registers, POS register 3 and POS register 4, contain information about the type of memory on the system board. The memory connectors are numbered from left to right as viewed from the front of the system. (See Figure 2-12 on page 2-14 for information on the signals.)

Bit	Function
7	AND of Presence Detect 3
6	Presence Detect 0, Connector 3
5	Presence Detect 2, Connector 3
4	Reserved
3	Presence Detect 0, Connector 2
2	Presence Detect 2, Connector 2
1	Presence Detect 0, Connector 1
0	Presence Detect 2, Connector 1

Figure 2-10. System Board POS Register 3 (Hex 0103) – Types 3 and 4

Bits 7 This bit is the AND of the 'presence detect 3' signal for all connectors. This bit is 1 if the proper memory cards are installed.

Bits 6, 3, 1 Each bit indicates the state of the 'presence detect 0' signal.

Bits 5, 2, 0 Each bit indicates the state of the 'presence detect 2' signal.

Bit 4 This bit is reserved.

System Board POS Register 4 (Hex 0104) – Types 3 and 4

On the Type 3 and Type 4 system boards, this read-only register and POS Register 3 contain information about the type of memory on the system boards.

Bit	Function
7	Presence Detect 1, Connector 4
6	Presence Detect 1, Connector 3
5	Presence Detect 1, Connector 2
4	Presence Detect 1, Connector 1
3, 2	Cache ID bits
1	Presence Detect 0, Connector 4
0	Presence Detect 2, Connector 4

Figure 2-11. System Board POS Register 4 (Hex 0104) – Types 3 and 4

Bits 7 - 4 These bits indicate the state of the 'presence detect 1' signal.

Bits 3, 2 These bits describe the processor card. Both bits are set to binary 00 on the Type 3 system board, indicating a 64KB cache with a 80386 microprocessor operating at 25 MHz. The cache ID bits are set to binary 01 on the Type 4 system board, indicating a 80486 microprocessor operating at 25 MHz.

Bit 1 This bit indicates the state of the 'presence detect 0' signal.

Bit 0 This bit indicates the state of the 'presence detect 2' signal.

Memory Presence Detect

The presence detect signals are used by the system to determine size and speed of memory on the memory card. The pins are either connected to ground or not connected.

A set of four bits shows the state of all presence detect signals for a specific memory connector; the bit is 0 when the signal is grounded. The following table shows the information indicated by these bits and the system board types that support each memory card. All combinations not shown are reserved.

Presence Detect 3 2 1 0	Function	System Board
0 0 1 0	1MB 100-ns Memory	Type 1
0 0 0 1	2MB 100-ns Memory	Type 1
0 1 1 0	1MB 85-ns Memory	Types 1 and 2
0 1 0 1	2MB 85-ns Memory	Types 1 and 2
1 0 0 1	2MB 80-ns Memory	Types 3 and 4

Figure 2-12. Presence Detect Bits

Adapter Enable/Setup Register (Hex 0096)

This read/write register selects the connector to be configured.

Bit	Symbol
7	Channel Reset
6 - 4	Reserved
3	Card Setup Enable
2 - 0	Channel Select 2 - 0

Figure 2-13. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6 - 4 These bits are reserved.

Bit 3 When set to 1, this bit enables the '-card setup' signal selected by bits 2 through 0.

Bits 2 - 0 These bits are the address bits for the '-card setup' signal. Connectors 1 through 3 are addressed as 0 through 2, respectively, and the fixed disk connector is addressed as 3. When bit 3 is set to 1, these bits select the connector that is put into setup mode.

Each channel connector has a unique '-card setup' signal (-CD SETUP) associated with it. This signal is used to put the adapters in the setup mode, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Notes:

1. -CD SETUP goes active only when an operation is performed in the I/O address range hex 0100 through 0107.
2. The status of port hex 0096 can be read by software. However, when the port is read, bits 6, 5, and 4 are set to 1.

Notes:

Section 3. System Board

Description 3-3
80387 Math Coprocessor 3-3
Micro Channel Implementation 3-3
| Exception Reporting 3-3
| Matched-Memory 3-3
| Matched-Memory Extension 3-4
| Signal Descriptions 3-5
Central Arbiter 3-6
Arbitration Bus Priority Assignments 3-6
Central Arbiter Programming 3-7
Diskette Drive and Fixed Disk Connectors 3-9
Direct Bus Attachment Connector 3-9
Diskette Drive Connectors 3-12
Fixed Disk Drive Connector 3-13
Memory 3-14
Read-Only Memory Subsystem 3-14
Random Access Memory Subsystem 3-15
System and Nonsystem Memory 3-15
Memory Caching 3-16
Error Recovery 3-18
Memory Subsystem Control 3-19
Memory Encoding Register 1 (Hex 00E1) 3-19
Memory Encoding Register 2 (Hex 00E0) 3-21
Memory Encoding Register 3 (Hex 00E2) – Types 3 and 4 . 3-22
System Memory Maps 3-24
System Board Memory Connectors 3-29
Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM 3-31
RT/CMOS Address Register and NMI Mask (Hex 0070) . . 3-32
RT/CMOS Data Register (Hex 0071) 3-32
RT/CMOS RAM I/O Operations 3-33
Real-Time Clock Bytes (Hex 000 - 00D) 3-34
CMOS RAM Configuration 3-38
Miscellaneous System Functions 3-43
Nonmaskable Interrupt 3-43
System Control Port B (Hex 0061) 3-43
System Control Port A (Hex 0092) 3-45
Power-On Password 3-47
Hardware Compatibility 3-48
Error Codes 3-49

© Copyright IBM Corp. 1989, 1990

Notes:

Description

This section describes the math coprocessor, channel differences, memory subsystems, and miscellaneous system ports and connectors for the Model 70. Additional information on these topics can be found in the *Hardware Interface Technical Reference* listed in the preface of this manual.

80387 Math Coprocessor

The 80387 Math Coprocessors are matched to the speed of the system microprocessor and operate in the synchronous mode. The different speed coprocessors are not interchangeable; their logical operation is the same.

The microprocessor on the Type 4 system board incorporates the 80387 Math Coprocessor. Programs written for the 80387 Math Coprocessor will run without modifications.

Micro Channel Implementation

This section describes the implementation of the Micro Channel architecture on Model 70 systems. Refer to the Hardware Interface Technical Reference Micro Channel information for more information.

Exception Reporting

Exceptions should be reported using the asynchronous channel check procedure. The synchronous channel check procedure is not supported.

Matched-Memory

Each 32-bit channel connector has a matched-memory extension. The system microprocessor activates the '-matched memory cycle' signal (-MMC) when it does a memory access. This allows the Model 70 to support the same memory adapter design as the PS/2 Model 80 system board.

Although a memory adapter can respond to -MMC active by driving the '-matched memory cycle request' signal (-MMCR) active, the

Model 70 system board ignores -MMCR and performs a default cycle if the 'channel ready' signal (CD CHRDY) is active, or a synchronous-extended cycle if CD CHRDY is inactive. The Model 70 also drives the '-matched memory cycle command' signal active at the same time as the '-command' signal.

Matched-Memory Extension

This extension to the 32-bit Micro Channel connector provides the signals necessary to accommodate matched-memory cycles.

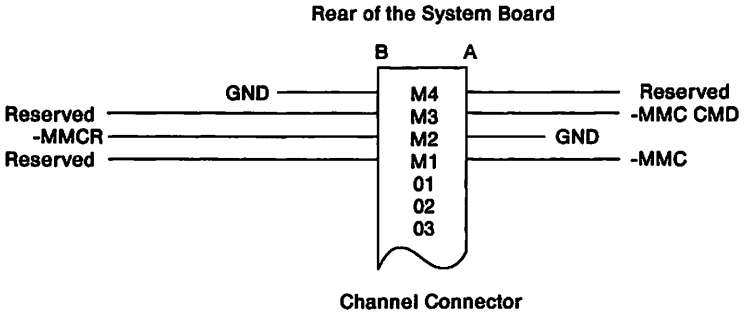


Figure 3-1. Matched-Memory Extension Voltage and Signal Assignments

Signal Descriptions

The following are descriptions of the matched-memory signals.

-MMC: -Matched Memory Cycle: This signal is driven by the system board logic to indicate to the channel slaves that the system microprocessor is the controlling master and is able to run a matched-memory cycle. -MMC is driven by a tri-state driver that can sink 24 milliamps.

-MMCR: -Matched Memory Cycle Request: This is a bus cycle control input signal. A 16- or 32-bit channel slave drives -MMCR to request a matched-memory cycle available on the system bus. This signal is driven active from an address decode and MEMORY/-IO signal.

If -MMCR is driven active by an 8-bit channel slave, or if it is driven active by a 16- or 32-bit channel slave during a cycle other than a microprocessor bus cycle, a default transfer cycle is run and -MMCR is not honored. CD CHRDY is used to extend the matched-memory cycle, as needed. The 'address latch' signal (-ADL) and -CMD remain inactive for the entire matched-memory cycle.

Only the system microprocessor can drive matched-memory cycles. This signal is wired separately to each of the 32-bit channel connectors on the system board and ORed by the system logic. This signal is driven by a totem-pole driver that can sink 6 milliamps.

-MMC CMD: -Matched Memory Cycle Command: This output signal to the bus is generated for system microprocessor bus cycles only. It is used during a matched-memory cycle to define when the data on the bus is valid. The trailing edge of this signal indicates the end of the matched-memory cycle. As with -CMD, this signal indicates the time that the data is valid on the bus, and indicates when to latch the data from the bus or stop driving the data onto the bus. -MMC CMD is driven by a tri-state driver that can sink 24 milliamps.

Central Arbiter

The central arbitration control point gives intelligent subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. This arbiter supports up to 16 arbitrating devices.

Arbitration Bus Priority Assignments

The following table shows the assignment of arbitration levels. The functions with the lowest arbitration level have the highest priority.

ARB Level	Primary Assignment
-2	Memory Refresh
-1	NMI
0	DMA Channel 0 (Programmable to any arbitration level)
1	DMA Channel 1
2	DMA Channel 2
3	DMA Channel 3
4	DMA Channel 4 (Programmable to any arbitration level)
5	DMA Channel 5
6	DMA Channel 6
7	DMA Channel 7
8 - E	Available
F	System Microprocessor

Figure 3-2. Arbitration Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation, and by the previous controlling master. The diskette drive controller should not be held inactive for more than 12 microseconds to prevent overrun.

Nonmaskable interrupt (NMI) service is executed at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal is in the arbitrate state.

When the central arbitration control point receives a level -1 request (NMI, a system-board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level -1 request, and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following tables.

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Mask
5	Enable Extended Arbitration
4 - 0	Reserved

Figure 3-3. Arbitration Register (Hex 0090) — Write

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Masked by NMI
5	Bus Time-out
4	Reserved
3 - 0	Value of Arbitration Bus During Previous Grant State

Figure 3-4. Arbitration Register (Hex 0090) — Read

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 enables extended arbitration. The minimum arbitration cycle is 300 nanoseconds; this bit extends that minimum cycle to 600 nanoseconds. This bit is set to 0 during a system reset.

Reading this bit as a 1 indicates that a bus time-out has occurred, and resets bit 6 in this register to 0.

Bit 4 This bit is reserved and should be 0.

Bits 3 - 0 These bits are undefined for a write operation and should be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Diskette Drive and Fixed Disk Connectors

The system board has a 2- by 56-pin connector that provides direct bus attachment for two diskette drives and one fixed disk through the fixed disk and diskette drive adapter.

For the diskette drives, this adapter passes control and data signals between the diskette drive controller on the system board and the drives. For the fixed disk drive, the adapter provides a path for the Micro Channel signals necessary for fixed disk operations. It also provides the power required for fixed disk and diskette drive operations.

When in the setup mode, the fixed disk drive is addressed as channel connector 4 through the Adapter Enable/Setup register. For more information about this register, see the POS information in the *Hardware Interface Technical Reference*. For more POS information about the fixed disk drive, refer to the technical reference for that drive.

Direct Bus Attachment Connector

The following figure shows the signal assignments and pin numbers for the 2- by 56-pin system board connector.

Side B			Side A		
Pin	I/O	Signal	Pin	I/O	Signal
1	O	-High Density Select	1	I	-2nd Drive Installed
2	O	+12 Vdc	2	O	+12 Vdc
3	O	+12 Vdc	3	O	+12 Vdc
4	O	+5 Vdc	4	I	CD CHRDY
5	I	-Index	5	O	M/-IO
6	O	-Motor Enable 1	6	N/A	Ground
7	O	-Drive Select 0	7	O	-S1
8	N/A	Ground	8	O	+5 Vdc
9	O	-Drive Select 1	9	O	-S0
10	O	-Motor Enable 0	10	N/A	Ground
11	O	-Direction In	11	N/A	Reserved
12	N/A	Ground	12	O	-TC
13	O	-Step	13	O	ARB/-GNT
14	O	-Write Data	14	N/A	Ground
15	O	-Write Enable	15	I/O	ARB 03
16	N/A	Frame Ground	16	I/O	ARB 02
17	I	-Track 0	17	I/O	ARB 01
18	I	-Write Protect	18	N/A	Frame Ground
19	I	-Read Data	19	N/A	Reserved
20	O	-Head 1 Select	20	I/O	ARB 00
21	I	-Diskette Change	21	I	-BURST
22	I	-IRQ 14	22	N/A	Ground
23	I	-CD DS 16	23	I	-PREEMPT
24	N/A	Ground	24	O	+5 Vdc
25	O	-SBHE	25	O	-ADL
26	I/O	D13	26	N/A	Ground
27	O	+12 Vdc	27	O	+12 Vdc
28	I/O	D11	28	O	A00
29	I/O	D10	29	O	A01
30	I/O	D07	30	N/A	Ground
31	I/O	D06	31	O	A02
32	N/A	Ground	32	O	+5 Vdc
33	I/O	D05	33	O	A03
34	I/O	D02	34	N/A	Ground
35	O	+12 Vdc	35	O	+12 Vdc
36	I/O	D00	36	O	A04
37	I/O	D15	37	O	A05
38	I/O	D14	38	N/A	Ground
39	I/O	D12	39	O	A06
40	N/A	Ground	40	O	+5 Vdc
41	I/O	D09	41	O	A07
42	I/O	D08	42	N/A	Ground
43	O	CHRESET	43	N/A	Reserved
44	O	+5 Vdc	44	N/A	Reserved
45	I/O	D04	45	O	A08
46	N/A	Key	46	N/A	Key

Figure 3-5 (Part 1 of 2). Direct Bus Attachment

Side B			Side A		
Pin	I/O	Signal	Pin	I/O	Signal
47	N/A	Key	47	N/A	Key
48	N/A	Ground	48	O	+5 Vdc
49	I/O	D03	49	O	A09
50	I/O	D01	50	N/A	Ground
51	I	-CD SFDBK	51	O	A10
52	N/A	Ground	52	O	+5 Vdc
53	O	-CMD	53	O	A11
54	O	A12	54	N/A	Ground
55	O	14.3 MHz Osc	55	O	A13
56	N/A	Ground	56	O	+5 Vdc
57	O	A14	57	O	-CD SETUP
58	O	A15	58	N/A	Ground

Figure 3-5 (Part 2 of 2). Direct Bus Attachment

Diskette Drive Connectors

The following figure shows the signal assignments and pin numbers for the 2- by 20-pin diskette drive connectors on the adapter.

Pin	I/O	Signal	Pin	I/O	Signal
1	I	-2nd Drive Installed	2	O	-High Density Select
3	N/A	Reserved	4	N/A	Reserved
5	N/A	Ground	6	N/A	Reserved
7	N/A	Signal Ground	8	I	-Index
9	N/A	Signal Ground	10	N/A	Reserved
11	N/A	Signal Ground	12	O	-Drive Select
13	N/A	Ground	14	N/A	Reserved
15	N/A	Signal Ground	16	O	-Motor Enable
17	N/A	Signal Ground	18	O	-Direction In
19	N/A	Signal Ground	20	O	-Step
21	N/A	Signal Ground	22	O	-Write Data
23	N/A	Signal Ground	24	O	-Write Enable
25	N/A	Signal Ground	26	I	-Track 0
27	N/A	Signal Ground	28	I	-Write Protect
29	N/A	Signal Ground	30	I	-Read Data
31	N/A	Signal Ground	32	O	-Head 1 Select
33	N/A	Signal Ground	34	I	-Diskette Change
35	N/A	Frame Ground	36	N/A	Frame Ground
37	N/A	Ground	38	O	+5 Vdc
39	N/A	Ground	40	O	+12 Vdc

Figure 3-6. Diskette Drive Connectors

Fixed Disk Drive Connector

The following figure shows the signal assignment and pin numbering for the fixed disk drive connector on the adapter. The fixed disk drive connector is a 2- by 36-pin connector. Side A of the connector is the top and Side B is the bottom.

Side B			Side A		
Pin	I/O	Signal	Pin	I/O	Signal
1	I	-CD SETUP	1	O	A15
2	N/A	A13	2	O	A14
3	N/A	Ground	3	N/A	Ground
4	N/A	A11	4	O	14.3 MHz Osc
5	N/A	A10	5	N/A	Ground
6	N/A	A09	6	O	A12
7	N/A	+5 Vdc	7	O	-CMD
8	N/A	A08	8	I	-CD SFDBK
9	N/A	A07	9	N/A	Ground
10	N/A	A06	10	I/O	D01
11	N/A	Ground	11	I/O	D03
12	N/A	A05	12	I/O	D04
13	N/A	A04	13	N/A	Ground
14	N/A	A03	14	O	CHRESET
15	N/A	+5 Vdc	15	I/O	D08
16	N/A	A02	16	I/O	D09
17	N/A	A01	17	N/A	Ground
18	N/A	A00	18	I/O	D12
19	N/A	+12 Vdc	19	I/O	D14
20	N/A	-ADL	20	I/O	D15
21	N/A	-PREEMPT	21	N/A	Ground
22	N/A	-BURST	22	I/O	D00
23	N/A	+5 Vdc	23	I/O	D02
24	N/A	ARB 00	24	I/O	D05
25	N/A	ARB 01	25	N/A	Ground
26	N/A	ARB 02	26	I/O	D06
27	N/A	+12 Vdc	27	I/O	D07
28	N/A	ARB 03	28	I/O	D10
29	N/A	ARB/-GNT	29	N/A	Ground
30	N/A	-TC	30	I/O	D11
31	N/A	+5 Vdc	31	I/O	D13
32	N/A	-S0	32	O	-SBHE
33	N/A	-S1	33	N/A	Ground
34	N/A	M/-IO	34	I	-CD DS 16
35	N/A	Ground	35	I	-IRQ 14
36	N/A	CD CHRDY	36	N/A	Ground

Figure 3-7. Fixed Disk Drive Connector

Memory

Model 70 systems use the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- Real-time Clock and CMOS RAM.

Read-Only Memory Subsystem

The ROM subsystem consists of 128KB. At power-on, ROM is active in two address spaces: hex 000E0000 to 000FFFFF and hex FFFE0000 to FFFFFFFF. After POST (power-on self test) ensures the proper operation of system memory, the ROM code is copied to RAM. ROM is then disabled, and the RAM responds to the ROM addresses. This RAM is write protected.

CAUTION:
Although this RAM is write protected, writing to this space can cause unpredictable results on systems with cache.

ROM or RAM access at address space hex 000E0000 to 000FFFFF is controlled by the ROMEN bit in Memory Encoding Register 1 (hex 00E1). When enabled, ROM is not parity-checked and operates with a minimum of 200-nanoseconds in wait states.

For the Type 3 and Type 4 system boards, the address space hex 000E0000 to 000FFFFF is not cached if ROM is enabled, and is cached if ROM is disabled.

Warning: On systems with a cache, writing to the ROM address space with the ROM enable bit set to 0 (bit 1 address hex 00E1) might produce unpredictable results, including parity errors or problems with cache integrity.

Random Access Memory Subsystem

The RAM subsystem on the system board starts at address hex 00000000 of the address space. The RAM subsystem is 36 bits wide: 32 data bits and 4 parity bits. One parity bit is generated for each byte of data written. During a read operation, one parity bit is checked for each byte of data read by the device controlling the bus.

The Model 70 enables and disables memory in 1MB blocks. Each 1MB block must start on a 1MB boundary. Because 128KB of I/O ROM, and 128KB of video memory are mapped within the first 1MB address space, an overflow is created from the first 1MB of RAM installed in the system. The first 1MB of RAM can be split at either 512KB or 640KB; the memory from the split to the start of the RAM that contains the ROM code is called the *split memory block*. This split memory block can be disabled, or it can be remapped to the first address following the last 1MB of memory. Split memory block remapping and disabling are controlled by the memory encoding registers.

Notes:

1. Additional memory can be added in either of the 32-bit Micro Channel connectors. However, the total amount of memory installed should not exceed the 16MB addressing limit of the DMA controller.
2. For the Type 3 and Type 4 system boards, system memory must be 32-bits wide (nonsystem memory can be any width).

System and Nonsystem Memory

Two basic types of memory can be assigned addresses within the memory address space: system memory and nonsystem memory.

System memory is memory that is managed and allocated by the primary operating system. It remains assigned to and fixed in the 4GB (GB = 1,073,741,824 bytes) physical address space, and its contents can be accessed or modified only by an independent master (bus master, system microprocessor, or DMA controller).

Nonsystem memory is memory that is not managed or allocated by the primary operating system. It is made up of memory-mapped I/O devices, memory on an adapter that can be directly modified by the adapter, or memory that can be relocated within the address space, such as bank switched and EMS (expanded memory specifications). Nonsystem memory should not be mapped into microprocessor's cacheable address space.

Memory Caching

The following figure is the memory map for the first 32MB of address space on Type 3 and Type 4 system boards and shows which addresses can be used with the cache. On these system boards, the address space from 32MB to the end of the second GB is not usable. The third and fourth GB are not mapped into the cache, but can be used, especially for nonsystem memory.

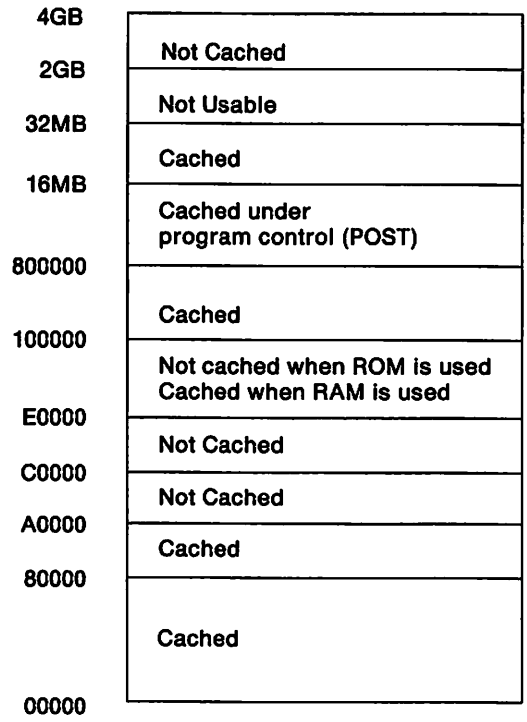


Figure 3-8. Mapping of the First 32MB Segment

Within the first 16MB of address space, all system memory above 1MB must be one contiguous sum starting at the 1MB boundary. If nonsystem memory is present, it should be assigned addresses starting at 16MB and counting down. Do not assign addresses below 8MB to nonsystem memory.

If nonsystem memory exists between 8MB and 16MB, caching for that 8MB block must be disabled even if system memory is also located there. Setup routines must be aware of the existence and location of nonsystem memory so that POST can properly control the caching of the second 8MB.

In the 16MB to 4GB address space, system memory can be contiguously placed from 16MB up to 32MB and can be cached. If nonsystem memory is located within the 16MB to 4GB address space, it should be assigned addresses starting at 4GB and counting down, allowing space for system ROM.

Error Recovery

If POST detects a memory error in the first 512KB of memory, the first physical 1MB block of memory is deactivated. The addresses assigned to the deactivated block are reassigned to the second physical block of system board memory (the first 1MB of system memory must reside in connector 1 or 2). If 1MB of valid memory cannot be allocated from connector 1 or 2, the system cannot recover from the error. The first 1MB of memory address space cannot be assigned to memory on the channel.

POST does not deactivate a memory block if an error is detected in the second 512KB of that block. If an error is detected in that area of memory, the 1MB block containing the error can be deactivated and have its addresses reassigned by running the customer-level memory diagnostics program on the Reference Diskette supplied with the system. Once a block of memory is deactivated, it is ignored by POST on subsequent power-ons.

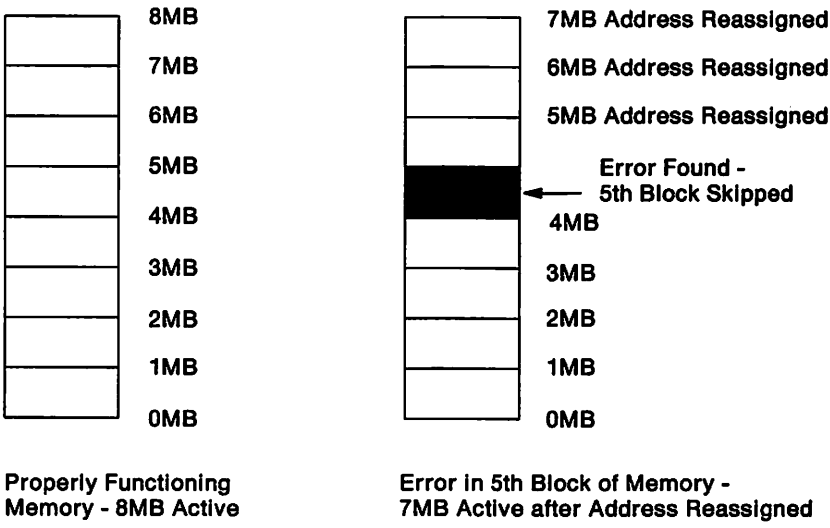


Figure 3-9. Memory Error Address Reassignment

Memory Subsystem Control

These read/write registers define and control the ROM and RAM subsystems.

Memory Encoding Register 1 (Hex 00E1)

This register determines how the first 1MB of memory is addressed and is used with Memory Encoding Register 2 to determine the amount of system board memory enabled.

Bit	Function
7	-Card 2 EN2
6	-Card 2 EN1
5	-Card 1 EN2
4	-Card 1 EN1
3	-ENSPLIT
2	-640
1	ROMEN
0	-ENPLRPCH

Figure 3-10. Memory Encoding Register 1 (Hex 00E1)

Bits 7, 6 These bits define system board memory in connector 2. When they are set to 0, bit 6 enables the first 1MB block and bit 7 enables the second 1MB block.

Bits 5, 4 These bits define system board memory in connector 1. When they are set to 0, bit 4 enables the first 1MB block and bit 5 enables the second 1MB block.

Bit 3 This bit determines if the split-memory block is assigned addresses or is disabled. The top 128KB of the first 1MB is always mapped into the ROM address space and the code in ROM is copied into this space.

When this bit is set to 0, the split-memory block is enabled. The split-memory block size is dependent on the value of the 640 bit. Its address is determined in Memory Encoding Register 2. When this bit is set to 1, the split-memory block is disabled.

Note: If the total system memory is equal to or greater than 16MB, the split-memory block cannot be used.

Bit 2 This bit determines where the first active 1MB of memory is split.

Note: Because the memory below 640KB is always cached, this bit is always set to 0 for Type 3 and Type 4 system boards.

When this bit is set to 0, the system maps 640KB of the first 1MB to address hex 00000000 to 0009FFFF. The split-memory block, 256KB, is mapped to the address specified in Memory Encoding Register 2.

When this bit is set to 1, the system maps 512KB of the first 1MB to address hex 00000000 to 0007FFFF. The split-memory block, 384KB, is mapped to the address specified in Memory Encoding Register 2. The addresses hex 00080000 to 0009FFFF are unassigned.

Bit 1 This bit determines how addresses hex 000E0000 to 000FFFFF are assigned.

When this bit is set to 1, ROM is enabled and the read-access addresses are assigned to ROM; the write-access addresses are assigned to RAM. When this bit is set to 0, ROM is disabled and read addresses are assigned to RAM; the write addresses are disabled while ROM is disabled.

Note: When this bit is set to 1, system performance will be substantially slower because of 16-bit accesses to ROM and a longer cycle.

Bit 0 When set to 0, this bit enables parity checking of system board memory. For compatibility with other systems, enabling and disabling of parity checking should be done through System Control Port B at address hex 0061 (see "System Control Port B (Hex 0061)" on page 3-43).

Memory Encoding Register 2 (Hex 00E0)

This register is used with Memory Encoding Register 1 to determine the amount of system board memory that is enabled. It also contains the address for the split-memory block.

Bit	Function
7	-Card 4 EN2
6	-Card 4 EN1
5	-Card 3 EN2
4	-Card 3 EN1
3	SPA23
2	SPA22
1	SPA21
0	SPA20

Figure 3-11. Memory Encoding Register 2 (Hex 00E0)

Bits 7, 6 These bits are used on the Type 3 system board only. They define the system board memory in connector 4. When set to 0, bit 6 enables the first 1MB block and bit 7 enables the second 1MB block. For Type 1 and Type 2 system boards, these bits must be set to 1.

Bits 5, 4 These bits define the system board memory in connector 3. When they are set to 0, bit 4 enables the first 1MB block and bit 5 enables the second 1MB block.

Bits 3 - 0 These bits define the starting address of the split-memory block. When split memory is enabled, these bits determine its starting address. The starting location can be at any 1MB boundary from 1MB to 15MB.

Memory Encoding Register 3 (Hex 00E2) – Types 3 and 4

This read/write register is used by the Type 3 and Type 4 system boards only and provides control of the cache memory.

Bit	Function
7	Reserved
6	-Preempt Enable
5	-Cache Flush
4	Lock
3	Reserved
2	-Cache 2nd 8MB
1	Reserved
0	-Enable Cache

Figure 3-12. Memory Encoding Register 3 (Hex 00E2) – Types 3 and 4

Bit 7 This bit is reserved.

Bit 6 This bit controls the preempt support for the system microprocessor. When this bit is set to 1, preempting is disabled. When this bit is set to 0, system logic activates the '-preempt' signal when the system microprocessor accesses a memory location not satisfied in the cache (cache miss).

Bit 5 See the description of bit 0.

Bit 4 On the Type 3 system board, this bit controls if locked-access operations from the system microprocessor can or cannot be cache hits.

If this bit is set to 0, all locked-access operations are treated as cache misses. If this bit is set to 1, locked-access operations can be cache hits.

This bit is not used on the Type 4 system board.

Bit 3 This bit is reserved.

Bit 2 This bit determines if the second 8MB of memory is cached or not. When the bit is set to 0, the second 8MB is cached.

Note: Before disabling the caching of the second 8MB, disable and flush the cache.

Bit 1 This bit is reserved.

Bit 0 This bit and bit 5 work together to control the state of the cache. These bits must always be modified in the same I/O instruction.

For Type 3, these bits must always be written in the sequence shown below and always be opposite polarities. The following describes their control.

1. Bit 5=0 and Bit 0=1 for the disabled/flushed state.
2. Bit 5=1 and Bit 0=0 for the enabled state.

For the Type 4 system board, these bits work together to control the state of the cache; either disabled, disabled and flushed, or enabled. These bits must always be written in the sequence shown below for the Type 4 system board.

1. Bit 5=0 and Bit 0=1 for the disabled/flushed state.
2. Bit 5=1 and Bit 0=1 for the disabled state.
3. Bit 5=1 and Bit 0=0 for the enabled state.

Notes:

1. Refer to the 80486 specification microprocessor section for information on CR0, which must also be set to enable the 80486 internal 8KB cache.
2. The cache must be disabled and flushed before enabling ROM or disabling the caching of the second 8MB.

System Memory Maps

Memory is mapped by the Memory Encoding registers. The mapping results in either 512KB or 640KB of system board RAM starting at address hex 00000000 (system boards Type 3 and Type 4 do not support the split at 512KB). A 256-byte and 1KB portion of this RAM are reserved as BIOS data areas. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for details.

In the following tables, the variable *X* represents the number of 1MB blocks of system board memory starting at or above the hex 00100000 boundary. The variable *Y* represents the number of 1MB blocks of memory installed in the channel starting at or above the hex 00100000 boundary (*Y* = 0 to 15).

The following table shows the memory mapping when:

Enable Split bit = 1
640 bit = 1
ROM enable bit = 1.

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-13. System Memory Map 1

The following table shows the memory mapping when:

Enable Split bit = 1
640 bit = 0
ROM enable bit = 1.

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-14. System Memory Map 2

The following table shows the memory mapping when:

Enable Split bit = 0
640 bit = 1
ROM enable bit = 1
Split address bits = 1 + *X* + *Y* (Total range = 1 to 15).

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to (00100000 + XMB + YMB +384KB)	384KB System Board RAM
(00100000 + XMB + YMB + 384KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-15. System Memory Map 3

The following table shows the memory mapping when:

Enable Split bit = 0
640 bit = 0
ROM enable bit = 1
Split address bits = 1 + *X* + *Y* (Total range = 1 to 15).

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to (00100000 + XMB + YMB + 256KB)	256KB System Board RAM
(00100000 + XMB + YMB + 256KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-16. System Memory Map 4

The following table shows the memory mapping when:

Enable Split bit = 1
640 bit = 1
ROM enable bit = 0.

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00008000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM Mapped to RAM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-17. System Memory Map 5

The following table shows the memory mapping when:

Enable Split bit = 1
640 bit = 0
ROM enable bit = 0.

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM Mapped to RAM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-18. System Memory Map 6

The following table shows the memory mapping when:

Enable Split bit = 0
640 bit = 1
ROM enable bit = 0
Split address bits = 1 + X + Y (Total range = 1 to 15).

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM Mapped to RAM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to (00100000 + XMB + YMB + 384KB)	384KB of First 1MB at Split Address
(00100000 + XMB + YMB + 384KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-19. System Memory Map 7

The following table shows the memory mapping when:

Enable Split bit = 0
640 bit = 0
ROM enable bit = 0
Split address bits = 1 + *X* + *Y* (Total range = 1 to 15).

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128K System Board ROM Mapped to RAM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to (00100000 + *X*MB + *Y*MB + 256KB-1)	256KB of First 1MB at Split Address
(00100000 + *X*MB + *Y*MB + 256KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-20. System Memory Map 8

System Board Memory Connectors

The Type 1 and Type 2 system boards have three 72-pin memory connectors that support the 1MB and 2MB memory cards. The numbering of the connectors depends on the location. If the memory connectors are under the diskette drives, the connectors are numbered from left to right. If the connectors are under the fixed disk drive, the connectors are numbered from right to left.

The Type 3 and Type 4 system boards have four 72-pin memory connectors and only support the 2MB, 80-nanosecond memory card. The four connectors are numbered from the left as viewed from the front of the system.

The following figure shows the pin assignments for the 1- by 72-pin memory connectors. Refer to "Memory Presence Detect" on page 2-14 for decoding of the presence detect signal.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Ground	37	I/O	Parity Data 1
2	I/O	Data 0	38	I/O	Parity Data 3
3	I/O	Data 16	39	N/A	Ground
4	I/O	Data 1	40	O	Column Address Strobe 0
5	I/O	Data 17	41	O	Column Address Strobe 2
6	I/O	Data 2	42	O	Column Address Strobe 3
7	I/O	Data 18	43	O	Column Address Strobe 1
8	I/O	Data 3	44	O	Row Address Strobe 0
9	I/O	Data 19	45	O	Row Address Strobe 1
10	O	+5 Vdc	46	O	Block Select 1
11	O	-Column Address Strobe P	47	O	Write Enable
12	O	Address 0	48	N/A	Reserved
13	O	Address 1	49	I/O	Data 8
14	O	Address 2	50	I/O	Data 24
15	O	Address 3	51	I/O	Data 9
16	O	Address 4	52	I/O	Data 25
17	O	Address 5	53	I/O	Data 10
18	O	Address 6	54	I/O	Data 26
19	N/A	Reserved	55	I/O	Data 11
20	I/O	Data 4	56	I/O	Data 27
21	I/O	Data 20	57	I/O	Data 12
22	I/O	Data 5	58	I/O	Data 28
23	I/O	Data 21	59	O	+5 Vdc
24	I/O	Data 6	60	I/O	Data 29
25	I/O	Data 22	61	I/O	Data 13
26	I/O	Data 7	62	I/O	Data 30
27	I/O	Data 23	63	I/O	Data 14
28	O	Address 7	64	I/O	Data 31
29	O	Block Select 0	65	I/O	Data 15
30	O	+5 Vdc	66	O	Block Select 2
31	O	Address 8	67	I	Presence Detect 0
32	N/A	Reserved	68	I	Presence Detect 1
33	O	Row Address Strobe 3	69	I	Presence Detect 2
34	O	Row Address Strobe 2	70	I	Presence Detect 3
35	I/O	Parity Data 2	71	O	Block Select 3
36	I/O	Parity Data 0	72	N/A	Ground

Figure 3-21. System Board Memory Connector

Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM

The real-time clock/complementary metal-oxide semiconductor RAM (RT/CMOS) chip contains the real-time clock and 64 bytes of CMOS RAM. The internal clock circuitry uses 14 bytes of this memory, and the rest is allocated to configuration and system status information.

In addition to the 64 bytes of CMOS RAM, a 2KB CMOS RAM extension is provided for configuration and other system information.

A battery maintains voltage to the RT/CMOS RAM and 2KB CMOS RAM extension when the power supply is not in operation.

The system cover can be locked to prevent battery removal and loss of password and configuration information.

The following table shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000 - 00D	Real-Time Clock Bytes
00E	Diagnostic Status Byte
00F	Shutdown Status Byte
010	Diskette Drive Type Byte
011	First Fixed Disk Drive Type Byte
012	Second Fixed Disk Drive Type Byte
013	Reserved
014	Equipment Byte
015 - 016	Low and High Base Memory Bytes
017 - 018	Low and High Expansion Memory Bytes
019 - 031	Reserved
032 - 033	Configuration CRC Bytes
034	Reserved
035 - 036	Low and High Useable Memory Bytes
037	Date Century Byte
038 - 03F	Reserved

Figure 3-22. RT/CMOS RAM Address Map

RT/CMOS Address Register and NMI Mask (Hex 0070)

This read/write register is used in conjunction with the port at hex 0071 to read and write the RT/CMOS RAM bytes.

Bit	Function
7	NMI Mask
6	Reserved
5 - 0	RT/CMOS RAM Address

Figure 3-23. RT/CMOS Address Register and NMI Mask (Hex 0070)

Warning: The operation following a write to hex 0070 must access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Bit 7 When this bit is set to 1, the NMI is masked off (the NMI is disabled). This bit is set to 1 by a power-on reset. This is a write-only bit.

Bit 6 This bit is reserved.

Bits 5 - 0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This port is used in conjunction with the address register at hex 0070 to read and write the RT/CMOS RAM bytes.

Bit	Function
7 - 0	RT/CMOS Data

Figure 3-24. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts should be masked to prevent other interrupt routines from changing the CMOS Address register before data is read or written. After I/O operations, the RT/CMOS and NMI Mask register (hex 0070) should be left pointing to Status Register D (hex 00D).

Warning: The operation following a write to hex 0070 must access hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

The following steps are required to perform I/O operations to the RT/CMOS RAM addresses:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Write the data to address hex 0071.

Reading RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Read the data from address hex 0071.

Real-Time Clock Bytes (Hex 000 - 00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following table.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second Alarm	1
002	Minutes	2
003	Minute Alarm	3
004	Hours	4
005	Hour Alarm	5
006	Day of Week	6
007	Date of Month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-25. Real-Time Clock Bytes

Note: The Setup program initializes status registers A, B, C, and D when the time and date are set. Interrupt hex 1A is the BIOS interface to read and set the time and date. It initializes the register the same way as the Setup program.

Status Register A (Hex 00A)

Bit	Function
7	Update in Progress
6 - 4	22-Stage Divider
3 - 0	Rate Selection Bits

Figure 3-26. Status Register A

Bit 7 When set to 1, this bit indicates the time-update cycle is in progress. When set to 0, it indicates the current date and time can be read.

Bits 6 - 4 These three divider-selection bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768 kHz time base. This is the only value supported by the system for proper time-keeping.

Bits 3 - 0 These bits allow the selection of a divider output frequency. The system initializes the rate selection bits to a binary 0110, which selects a 1.024 kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Periodic Interrupt Enable
5	Alarm Interrupt Enable
4	Update-Ended Interrupt Enable
3	Square Wave Enable
2	Date Mode
1	24-Hour Mode
0	Daylight Savings Enable

Figure 3-27. Status Register B

Bit 7 When set to 0, this bit updates the cycle, normally by advancing the counts at a rate of one per second. When set to 1, this bit immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This bit is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

Bit 5 When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit indicates if the time-and-date calendar updates use binary or binary-coded-decimal (BCD) formats. When set to 1, this bit indicates a binary format. The system initializes this bit to 0.

Bit 1 This bit establishes if the hours byte is in the 24-hour or 12-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When set to 1, this bit enables the daylight savings time mode. When set to 0, it disables the mode, and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt Request Flag
6	Periodic Interrupt Flag
5	Alarm Interrupt Flag
4	Update-Ended Interrupt Flag
3 - 0	Reserved

Figure 3-28. Status Register C

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 This bit is used in conjunction with bits 6, 5, and 4. When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When set to 1, this bit indicates that a periodic interrupt occurred.

Bit 5 When set to 1, this bit indicates that an alarm interrupt occurred.

Bit 4 When set to 1, this bit indicates that an update-ended interrupt occurred.

Bits 3 - 0 These bits are reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6 - 0	Reserved

Figure 3-29. Status Register D

Bit 7 This read-only bit monitors the power-sense pin. A low state of this pin indicates a loss of power to the real-time clock (dead battery). When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power.

Bits 6 - 0 These bits are reserved.

CMOS RAM Configuration

The following figure shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-Time Clock Chip Power
6	Configuration Record and Checksum Status
5	Incorrect Configuration
4	Memory Size Miscompare
3	Fixed Disk Controller/Drive C Initialization Status
2	Time Status Indicator
1	Adapter Configuration Miscompare
0	Adapter ID Time-Out

Figure 3-30. Diagnostic Status Byte

Bit 7 When set to 1, this bit indicates the real-time clock chip lost power.

Bit 6 When this bit is set to 1, the checksum is incorrect.

Bit 5 This is a check, at power-on time, of the Equipment byte. When set to 1, the configuration information is incorrect. Power-on checks require that at least one diskette drive be installed (bit 0 of the Equipment byte, hex 014, is set to 1).

Bit 4 When set to 1, this bit indicates the power-on check determined that the memory size is not the same as in the configuration record.

Bit 3 When set to 1, this bit indicates that the controller or drive C failed initialization, which prevents the system from attempting a power-on reset.

Bit 2 When set to 0, this bit indicates the time is valid. When set to 1, this bit indicates the time is invalid.

Bit 1 This bit indicates if the installed adapters match the configuration information. When this bit is set to 1, the adapters do not match the configuration information.

Bit 0 When set to 1, this bit indicates a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7 - 4	First Diskette Drive Type
3 - 0	Second Diskette Drive Type

Figure 3-31. Diskette Drive Type Byte

Bits 7 - 4 These bits indicate the first diskette drive type, as shown in the following table.

Bits 7 6 5 4	Function
0 0 0 0	No Drive Present
0 0 0 1	Double-sided Diskette Drive (48 tracks per inch, 360KB)
0 0 1 1	High-capacity Diskette Drive (720KB)
0 1 0 0	High-density Diskette Drive (1.44MB)

All combinations that are not shown are reserved.

Figure 3-32. Diskette Drive Type Byte (Bits 7 - 4)

Bits 3 - 0 These bits indicate the second diskette drive type, as shown in the following table.

Bits 3 2 1 0	Function
0 0 0 0	No Drive Present
0 0 0 1	Double-sided Diskette Drive (48 tracks per inch, 360KB)
0 0 1 1	High-capacity Diskette Drive (720KB)
0 1 0 0	High-density Diskette Drive (1.44MB)

All combinations that are not shown are reserved.

Figure 3-33. Diskette Drive Type Byte (Bits 3 - 0)

First Fixed Disk Drive Type Byte (Hex 011): This byte defines the type of the first fixed disk drive (drive C). Hex 00 indicates that a fixed disk drive is *not* installed.

Second Fixed Disk Drive Type Byte (Hex 012): This byte defines the type of the second fixed disk drive (drive D). Hex 00 indicates that a fixed disk drive is *not* installed.

Note: For more information about fixed disk drive types, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Reserved Byte (Hex 013): This byte is reserved.

Equipment Byte (Hex 014): The equipment byte, for the power-on diagnostic tests, defines the basic equipment in the system.

Bit	Function
7, 6	Number of Diskette Drives
5, 4	Display Operating Mode
3, 2	Reserved
1	Math Coprocessor Presence
0	Diskette Drive Presence

Figure 3-34. Equipment Byte

Bits 7, 6 These bits indicate the number of diskette drives installed, as shown in the following table.

Bits 7 6	Number of Diskette Drives
0 0	One Drive
0 1	Two Drives
1 0	Reserved
1 1	Reserved

Figure 3-35. Equipment Byte (Bits 7, 6)

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port, as shown in the following table.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-Column Mode
1 0	80-Column Mode
1 1	Monochrome Mode

Figure 3-36. Equipment Byte (Bits 5, 4)

Bits 3, 2 These bits are reserved.

Bit 1 When set to 1, this bit indicates that a math coprocessor is installed.

Bit 0 When set to 1, this bit indicates that a diskette drive is installed.

Low and High Base Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 is equal to 640KB. The low byte is hex 15; the high byte is hex 16.

Low and High Expansion Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The value from these bytes represents the number of 1KB blocks of expansion memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 17; the high byte is hex 18.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check (CRC) data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 33; the high byte is hex 32.

Reserved Byte (Hex 034): This byte is reserved.

Low and High Useable Memory Bytes (Hex 035 and 036): These bytes define the total amount of useable memory above the 1MB address space.

The hexadecimal values in these bytes represent the number of 1KB blocks of useable memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 35; the high byte is hex 36.

Date Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 through 03F): These bytes are reserved.

Miscellaneous System Functions

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system Watchdog time-out has occurred. The NMI stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts and the IRET instruction restores the interrupt flag to the state it was in prior to the interrupt. A system reset causes a reset of the NMI.

Nonmaskable interrupt requests caused by system board parity checks or channel checks are subject to mask control by the NMI mask bit in the RT/CMOS Address register. The Watchdog Timer and system channel time-out are not masked by this bit. (See "RT/CMOS Address Register and NMI Mask (Hex 0070)" on page 3-32). The power-on default of the NMI mask is 1 (NMI disabled). Prior to enabling the NMI after a power-on reset, the parity check and channel check state are initialized by the POST.

Warning: The operation following a write to hex 0070 must access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the read and write functions of this port are shown in the following tables.

Bit	Function
7	Reset Timer 0 Output Latch (IRQ0)
6 - 4	Reserved
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-37. System Control Port B (Write)

Bit	Function
7	Parity Check
6	Channel Check
5	Timer 2 Output
4	Toggles with Each Refresh Request
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-38. System Control Port B (Read)

Bit 7 Setting this bit to 1 resets IRQ0. Reading this bit as a 1 indicates a parity check has occurred.

Bit 6 Reading this bit as a 1 indicates a channel check has occurred.

Bit 5 This bit indicates the condition of the timer/counter 2 'output' signal.

Bit 4 This bit toggles for each refresh request.

Bit 3 Setting this bit to 0 enables channel check. Setting this bit is set to 1 during a power-on reset. Setting this bit to 1 disables channel check and clears the channel check latch.

Bit 2 Setting this bit to 0 enables parity check. This bit is set to 1 during a power-on reset. To clear a parity error, set this bit to 1 and then to 0.

Bit 1 Setting this bit to 1 enables speaker data.

Bit 0 Setting this bit to 1 enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7, 6	Fixed-Disk Activity Light
5	Reserved
4	Watchdog Timer Status
3	Security Lock Latch
2	Reserved
1	Alternate Gate A20
0	Alternate Hot Reset

Figure 3-39. System Control Port A

Bits 7, 6 These bits control the fixed-disk activity light. Setting either bit to 1 turns the fixed-disk activity light on. Setting both bits to 0 turns the light off. The power-on reset condition of each bit is 0.

Bit 5 This bit is reserved.

Bit 4 This read-only bit indicates the Watchdog Timer status. When this bit is set to 1, a Watchdog time-out has occurred. The Hardware Interface Technical Reference manuals contain more information about the Watchdog Timer.

Bit 3 This bit provides the security lock for the secured area of RT/CMOS. Setting this bit to 1 electrically locks the 8-byte, power-on password. Once this bit is set by POST, it can only be cleared by turning the system off.

Bit 2 This bit is reserved.

Bit 1 This bit is ORed with bit 1 in the keyboard output port to enable the 'address 20' signal (A20). When both bits are set to 0, A20 is disabled and set to 0. This bit is set to 0 during a system reset. (See the Keyboard and Auxiliary Device Controller section in the *Hardware Interface Technical Reference*.)

Bit 0 This bit provides an alternate method of resetting the system microprocessor. This alternate method supports operating systems requiring faster operation than was provided on the IBM Personal Computer AT*. Resetting the system microprocessor is used to switch the microprocessor from the protected mode to the real address mode. The alternate reset takes 13.4 microseconds.

This bit is set to 0 either by a system reset or a Write operation. When a Write operation changes this bit from 0 to 1, the alternate reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is 0, POST assumes the system was just powered on. If the bit is 1, POST assumes a switch from the protected mode to the real mode has taken place.

---

* Personal Computer AT is a trademark of the International Business Machines Corporation.

Power-On Password

RT/CMOS RAM has eight bytes reserved for the power-on password and its check character. The eight bytes are initialized to hex 00. The microprocessor can only access these bytes during power-on self-test (POST). After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by a program. A power-on password can be from 1 to 7 characters.

During power-on password installation, the password (1 to 7 keyboard scan codes), is stored in the security space.

Power-on password installation is a function of a program contained on the Reference Diskette. Once the power-on password utility has been installed, the password can be changed only during POST (power-on self-test). When the new power-on password is installed, changed, or removed, the password is not visible on the display.

The system unit cover can be physically locked to prevent unauthorized access to the battery. This helps prevent unauthorized battery removal and loss of power-on password and configuration information.

For information about the keyboard password, see the Keyboard and Auxiliary Device Controller section in the *Hardware Interface Technical Reference*.

Hardware Compatibility

The Model 70 maintains many of the interfaces used by the IBM Personal Computer AT. In most cases, command and status organization of these interfaces is maintained.

The functional interfaces for the Model 70 are compatible with the following interfaces:

- The Intel** 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller address/transfer counters, page registers and status fields only. The Command and Request registers are not supported. The rotate and mask functions are not supported. The Mode register is partially supported.
- The NS16450 serial port.
- The Intel 8088, 8086, and 80286 microprocessors.
- The Intel 8272 diskette drive controller.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The Intel 8042 keyboard port at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.
- Generally compatible with the Intel 80287 and 8087 Math Coprocessors.

** Intel is a trademark of the Intel Corporation.

** Motorola is a trademark of Motorola, Incorporated.

Error Codes

POST returns a message in the form of a number to indicate the type of test that failed. The following table gives the failure by error code. For information on unlisted error codes, contact Developer Assistance at 1-800-IBM-7763 (this number is for developers who are registered with IBM).

Error Number	Error Indication
101	Interrupt Failure
102	Timer Failure
103	Timer Interrupt Failure
104	Protected Mode Failure
105	Keyboard Controller Command Failure
107	Hot NMI Test
108	Timer Bus Test
109	Memory Select
110	System Board Parity
111	I/O Parity
112	Watchdog Timeout
113	DMA Arbitration Timeout
114	External ROM Checksum
160	System Board ID Not Recognized
161	Bad Battery or Configuration
162	CMOS Checksum or Adapter ID Mismatch
163	Date and Time Not Set
164	Memory Size Mismatch
165	Adapter ID Mismatch
166	Card Busy
167	System Clock Not Updating
201	Memory Miscompare or Parity
202	Memory Address Line Error (Address Line 00 - 15)
203	Memory Address Line Error (Address Line 16 - 31)
211	Memory Base 64KB on System Board Failed
215	Memory Base 64KB on Daughter/SIP 2 Failed
216	Memory Base 64KB on Daughter/SIP 1 Failed

Figure 3-40 (Part 1 of 2). POST Error Message Table

Error Number	Error Indication
221	ROM to RAM Copy
225	Wrong Speed Memory on System Board
301	Keyboard Interface
303	Keyboard or System Board
304	Keyboard Clock Failure
305	Keyboard +5V Error
601	Diskette Drive or Controller
602	Diskette Boot Record
1101	Async Error
2401	System Board Video
8601	Mouse Timeout
8602	Mouse Interface
8603	Mouse Interrupt
10480	Drive C Seek Failure
10481	Drive D Seek Failure
10482	Drive Failed Controller Test
10483	Drive Controller Failed to Reset
10490	Drive C Read Failure
10491	Drive D Read Failure
12901	Failed Processor Portion of Processor Board Test (Type 3 and Type 4)
12902	Failed Cache Portion of Processor Board Test (Type 3 and Type 4)
12903	Failed Math Coprocessor Portion of Processor Board Test (Type 4)

Figure 3-40 (Part 2 of 2). POST Error Message Table

Index

A

acoustic readings 1-14
activity light 3-45
adapter setup register 2-15
adapter, fixed disk and diskette drive 3-9
address maps
  memory 3-24
  POS 2-5
  reassignment 3-18
  system 1-8
address 20 gate 3-45
address, split memory 3-21, 3-22
alternate reset 3-46
arbiter programming 3-7
arbitration control point 3-6
arbitration level 3-6
arbitration register 3-7
arbitration, central control point 3-7
assistance, developer 3-49

B

base memory bytes 3-42
battery 3-31
block, split memory 3-15
bus attachment, direct 3-9
bus contention 2-3
bus priority assignments 3-6

C

cache, memory 3-15
card present bits 2-10
card selected feedback 2-6
-CD SFDBK 2-6
central arbitration control point 3-6
channel 1-5, 3-3
channel check enable 3-44
channel check latch 3-44
channel connectors 3-4
CMOS RAM 3-31
codes, POST error 3-49
compatibility, hardware 3-48
configuration CRC bytes 3-42
configuration, RT/CMOS 3-38
connectors
  drives 3-9
  fixed disk and diskette drive 3-9
  memory 3-29
connector, drives 3-9
connector, matched memory 3-4

D

date century byte 3-42
description
  math coprocessor 3-3
  memory 3-14
  NMI 3-43
  password 3-47
  programmable option select 2-3
  real-time clock 3-31
  system 1-3
  system board 1-4
description, power supply 1-15
developer assistance 3-49
diagnostic status byte (RT/CMOS) 3-38
direct bus attachment 3-9
diskette
diskette drive connector 3-12
diskette drive type byte 3-39
diskette overruns 3-6
DMA channels 3-6

E

enable error checking 3-20
enable NMI 3-32
enable, memory 3-19
equipment byte 3-41
error codes, POST 3-49

© Copyright IBM Corp. 1989, 1990

error recovery 3-18
extended arbitration 3-8
extension, matched memory 3-4

F

failures and messages, POST 3-49
fault, overvoltage 1-16
feedback, card selected 2-6
fixed disk activity light 3-45
fixed disk connector 3-13
fixed disk drive activity light 1-15
fixed disk drive initialization 3-38
fixed disk type byte 3-40

G

gate A20 3-45

H

hardware compatibility 3-48

I

identifier, model 1-4
interrupts
  IRQ0 reset 3-44
  NMI reset 3-43
I/O address map 1-8

L

light, fixed disk drive activity 1-15
light, power 1-15
list of features 1-5

M

matched memory 3-3, 3-4
matched memory extension 3-4
math coprocessor 3-3
maximum current 1-13
measurements 1-13
memory
  cached 3-15
  connectors 3-29
  description 3-14
memory *(continued)*
  enable bits 3-19
  error recovery 3-18
  nonsystem 3-15
  performance 1-9
  reassigning 3-18
  refresh 3-6
  split block 3-19
  system memory maps 3-24
memory card definition 2-10
memory encoding registers 3-19
memory maps 3-24
memory size miscompare 3-38
messages, POST error 3-49
micro channel 1-5, 3-3
microprocessor
  alternate reset 3-46
  gate A20 3-45
  mode switch compatibility 3-46
  performance 1-9
microprocessor cache 3-15
-MMC 3-5
-MMC CMD 3-5
-MMCR 3-5
mode switching 3-46
model/submodel bytes 1-4

N

NMI mask 3-32
NMI service 3-7
NMI signal 3-6
noise readings 1-14
nonmaskable interrupt (NMI) 3-43
nonsystem memory 3-15

O

output voltage sequencing 1-16
outputs, power supply 1-15
overvoltage fault 1-16

P

parallel port select 2-8
parity check 3-20
parity check enable 3-44

password, power-on 3-47
performance 1-9, 3-3
ports, system 3-43
POS register 2 2-8
POS register 3 2-10
POS register 4 2-13
POST error codes 3-49
power specifications 1-13
power supply 1-5
power supply description 1-15
power supply LED 1-15
power supply output
protection 1-16
power supply outputs 1-15
programmable option select
(POS) 2-3
address decode 2-6
address map 2-5
registers 2-5
setup procedures 2-4
setup register 2-7
system board 2-6
system board I/O 2-8
system configuration
utilities 2-3
system memory maps 3-24
video 2-7
warning 2-3
programming, arbiter 3-7
protected mode switch 3-46
protection, power supply 1-16

R

random access memory 3-15
read-only memory (ROM) 3-14
real mode switch 3-46
real-time clock bytes 3-34
refresh 3-7
refresh request 3-44
registers
adapter setup 2-15
card feedback 2-6
memory encoding 3-19
miscellaneous system 3-43
RT/CMOS and NMI mask 3-32
RT/CMOS status registers 3-35
registers *(continued)*
system board POS 2-7
system control 3-43
ROM enable 3-20
RT/CMOS address register 3-32
RT/CMOS RAM 3-31
password 3-47
secured area 3-45

S

second fixed disk type byte 3-40
sequencing, output voltage 1-16
setup
bus contention 2-3
registers 2-7
system board 2-6
system board I/O 2-8
system memory maps 3-24
video 2-7
shutdown status byte 3-38
size 1-13
size determine, memory 2-10
sound specifications 1-14
speaker data enable 3-44
specifications
performance 1-9, 1-10, 1-11,
1-12
physical 1-13
system unit 1-13
split address 3-21, 3-22
split memory block 3-15, 3-19
status registers (RT/CMOS) 3-35
subsystems, memory 3-14
switch to real 3-46
system address map 1-8
system board 1-4
features 1-4
I/O register 2-8
memory connector 3-29
memory registers 3-19
model identifier 1-4
POS registers 2-7
setup 2-6
system configuration utilities 2-3
system control port A 3-45

system control port B 3-43
system control ports 3-43
system description 1-3
system functions,
  miscellaneous 3-43
system memory 3-15
system performance 1-9
system ports, miscellaneous 3-43
system reset 3-43
system unit specifications 1-13

T

time status indicator 3-38
type identifier 1-4

U

useable memory 3-42

V

valid RAM bit 3-37
video setup 2-7

W

warnings
  arbitration 3-6
  central arbiter 3-8
  NMI mask 3-43
  POS 2-3
  real-time clock 3-32
watchdog status 3-45

Numerics

80287 Math Coprocessor 3-48
80386 performance 1-9
80387 Math Coprocessor 3-3
8087 Math Coprocessor 3-48

IBM PS/2 Model P75 Supplement for the Hardware Interface and BIOS Interface Technical Reference

November 15, 1990

Part Number 84F7592

Form Number S84F-7592-00

Instructions

1. Use the *IBM* Personal System/2* Model P75 Technical Reference* with the *IBM Personal System/2 Hardware Interface Technical Reference.*
2. Use the *IBM Personal System/2 Model P75 Supplement*, located at the back of this package, with the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

---

* IBM and Personal System/2 are trademarks of the International Business Machines Corporation.

Personal System/2
Model P75
Technical Reference

First Edition (November 1990)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law. INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer or express or implied warranties in certain transactions, therefore, this statement may not apply to you.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Requests for technical information about IBM products should be made to your IBM Authorized Dealer or your IBM Marketing Representative.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Armonk, NY 10577.

© Copyright International Business Machines Corporation 1990. All rights reserved.
Note to US Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Special Notices

References in this publication to IBM products, programs, or services do not imply that IBM intends to make these available in all countries in which IBM operates. Any reference to an IBM product, program or service is not intended to state or imply that only IBM's product, program, or service may be used. Any functionally equivalent product, program, or service that does not infringe any of IBM's intellectual property rights or other legally protectible rights may be used instead of the IBM product, program, or service. Evaluation and verification of operation in conjunction with other products, programs, or services, except those expressly designated by IBM, are the user's responsibility.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

The following terms, denoted by an asterisk (*) in this publication, are trademarks of the IBM Corporation in the United States and/or other countries:

IBM
IBM Personal Computer AT
Personal System/2
Micro Channel.

The following terms, denoted by a double asterisk (**) in this publication, are trademarks of other companies as follows:

800386SX	Intel Corporation
80387SX	Intel Corporation
Intel	Intel Corporation
Motorola	Motorola Incorporated.

Preface

The Technical Reference library is intended for those who develop hardware and software products for IBM Personal Computers and IBM Personal System/2. Users should understand computer architecture and programming concepts.

This technical reference provides hardware and software interface information for the IBM Personal System/2 Model P75 and should be used with the following publications:

IBM Personal System/2 Hardware Interface Technical Reference

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.

This manual consists of the following sections:

Section 1, "System Overview," describes the system, features, and specifications.

Section 2, "Programmable Option Select," describes the registers used for configuration.

Section 3, "System Board," describes the system-specific hardware implementations.

Section 4, "Video Subsystem," describes the function of the plasma display and the display adapter card.

Warning: The term *Reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware.

For information about components or devices not described in this manual, refer to the *Hardware Interface Technical Reference.* Information about diskette drives, fixed disk drives, adapters, and external options are in separate option technical references.

Notes:

Contents

Section 1. System Overview 1-1
Description 1-3
System Board Features 1-5
System Board Block Diagram 1-7
System Board I/O Address Map 1-8
Micro Channel Compatibility 1-12
  Procedures 1-12
  Buses and Extensions 1-12
Power Supply 1-15
  Input Protection 1-15
  Output Protection 1-15
  Power Supply Connectors 1-17
Dimensions for Micro Channel Adapter 1-18

Section 2. Programmable Option Select 2-1
Description 2-3
POS Address MAP 2-4
Card Selected Feedback 2-5
System Board Setup 2-6
  System Board Enable/Setup Register (Hex 0094) 2-6
  Adapter Enable/Setup Register (Hex 0096) 2-8
  System Board Functions 2-9
  System Board POS Register 0 (Hex 0100) 2-9
  System Board POS Register 1 (Hex 0101) 2-9
  System Board POS Register 2 (Hex 0102) 2-10
  System Board POS Register 3 (Hex 0103) 2-12
  Memory Presence Detect 2-14
  I/O Controller Functions 2-15
  I/O Controller POS Register 2 (Hex 0102) 2-16
  I/O Controller POS Register 3-1 (Hex 0103), Index 0000 2-17
  I/O Controller POS Register 4-1 (Hex 0104), Index 0000 2-18
  I/O Controller POS Register 3-3 (Hex 0103), Index 0002 2-19

Section 3. System Board 3-1
Description 3-3
Micro Channel 3-3
  Matched-Memory Cycles 3-3
  Central Arbiter 3-3
  Diskette Drive and Fixed Disk Drive Connectors 3-6

Memory 3-10
Read-Only Memory Subsystem 3-10
Random Access Memory Subsystem 3-11
System and Non-system Memory 3-11
Memory Caching 3-12
Memory Requirements and Limitations 3-14
Interleave Operation 3-14
Error Recovery 3-16
Memory Subsystem Control 3-17
System Memory Maps 3-22
System Board Memory Connectors 3-29
Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM 3-31
SCSI Port 3-43
Miscellaneous System Functions 3-46
Nonmaskable Interrupt 3-46
System Control Port B (Hex 0061) 3-46
System Control Port A (Hex 0092) 3-48
Power-On Password 3-50
Hardware Compatibility 3-51
POST Error Codes 3-53

Section 4. Video Subsystem 4-1
Description 4-3
Plasma Display 4-3
Plasma Display Card 4-4
Overview 4-4
Video Mode 4-6
Distinctive-mapping 4-7
Half-toning (Dithering) 4-8
Connectors and Signals 4-8

Index X-1

Figures

1-1. Model and Submodel Bytes 1-4
1-2. System Board Devices and Features 1-5
1-3. System Board 1-7
1-4. System Board I/O Address Map 1-9
1-5. Performance Specifications 1-10
1-6. Physical Specifications 1-11
1-7. Acoustical Readings 1-11
1-8. The 32-bit Connector 1-13
1-9. The 16-bit Connector 1-14
1-10. System-Board Power Supply Connector 1-18
1-11. Plasma-Display Power-Supply Connector 1-18
1-12. Adapter Dimensions (Half-Length) 1-19
1-13. Adapter Retainer 1-20
1-14. Typical Adapter Assembly 1-22
1-15. Permissive Areas (Full-Length Adapter) 1-23
1-16. Permissive Areas (Half-Length Adapter) 1-24
2-1. POS I/O Address MAP 2-4
2-2. Card Selected Feedback Register (Hex 0091) 2-5
2-3. System Board Enable/Setup Register (Hex 0094) 2-6
2-4. Adapter Enable/Setup Register (Hex 0096) 2-8
2-5. System Board POS Register 0 (Hex 0100) 2-9
2-6. System Board POS Register 1 (Hex 0101) 2-9
2-7. System Board POS Register 2 (Hex 0102) 2-10
2-8. Parallel Port Select Bits 2-10
2-9. POS Register 3 as a Write Port 2-12
2-10. POS Register 3 as a Read-Only Port (Bank 1) 2-13
2-11. POS Register 3 as a Read-Only Port (Bank 2) 2-13
2-12. Memory Presence Detect 2-14
2-13. I/O Controller Function 2-15
2-14. I/O Controller POS Register 2 (Hex 0102) 2-16
2-15. I/O Controller POS Register 3-1 (Hex 0103) 2-17
2-16. I/O Controller POS Register 4-1 (Hex 0104) 2-18
2-17. I/O Controller POS Register 3-3 (Hex 0103) 2-19
2-18. I/O POS Register 3-3 (Hex 0103), Bit 3 2-19
2-19. I/O POS Register 3-3 (Hex 0103), Bit 2 through 0 2-19
3-1. Arbitration Bus Priority Assignments 3-3
3-2. Arbitration Register (Hex 0090)-Write 3-4
3-3. Arbitration Register (Hex 0090)-Read 3-5
3-4. Internal Diskette Drive Connector 3-7

3-5. External Storage Device Connector 3-8
3-6. Fixed Disk Connector 3-9
3-7. Memory Caching 3-13
3-8. Example of the Interleave Operation 3-15
3-9. Example of the Non-Interleave Operation 3-15
3-10. Memory Error Address Reassignment 3-16
3-11. Memory Encoding Register 1 (Hex 00E0) 3-17
3-12. Memory Encoding Register 2 (Hex 00E1) 3-18
3-13. Memory Encoding Register 3 (Hex 00E2) 3-19
3-14. Memory Encoding Register 4 (Hex 00E3) 3-21
3-15. System Memory Map 3-22
3-16. System Memory Map 1 3-23
3-17. System Memory Map 2 3-24
3-18. System Memory Map 3 3-25
3-19. System Memory Map 4 3-25
3-20. System Memory Map 5 3-26
3-21. System Memory Map 6 3-26
3-22. System Memory Map 7 3-27
3-23. System Memory Map 8 3-28
3-24. System Board Memory Connector 3-29
3-25. Presence Detect Encoding 3-30
3-26. RT/CMOS RAM Address Map 3-31
3-27. RT/CMOS Address Register and NMI Mask (Hex 0070) 3-32
3-28. RT/CMOS Data Register (Hex 0071) 3-32
3-29. Real-Time Clock Bytes 3-34
3-30. Status Register A 3-35
3-31. Status Register B 3-35
3-32. Status Register C 3-37
3-33. Status Register D 3-37
3-34. Diagnostic Status Byte 3-38
3-35. Diskette Drive Type Byte 3-39
3-36. Diskette Drive Type Byte (Bits 7 - 4) 3-39
3-37. Diskette Drive Type Byte (Bits 3 - 0) 3-39
3-38. Equipment Byte 3-41
3-39. Equipment Byte (Bits 7, 6) 3-41
3-40. Equipment Byte (Bits 5, 4) 3-41
3-41. 50-pin SCSI Signal Connector 3-44
3-42. 60-pin SCSI Signal Connector 3-45
3-43. System Control Port B (Write) 3-47
3-44. System Control Port B (Read) 3-47
3-45. System Control Port A 3-48
3-46. POST Error Code Table 3-54

4-1. Block Diagram of the Plasma Display Card 4-5
4-2. Video Modes 4-6
4-3. System Interface Connector 4-9
4-4. 32-bit Extension 4-11
4-5. Auxiliary Video Extension 4-12
4-6. Plasma Display Connector 4-12

Section 1. System Overview

Description 1-3
System Board Features 1-5
System Board Block Diagram 1-7
System Board I/O Address Map 1-8
Micro Channel Compatibility 1-12
  Procedures 1-12
  Buses and Extensions 1-12
Power Supply 1-15
  Input Protection 1-15
    Ground-Leakage Current 1-15
  Output Protection 1-15
    Voltage Sequence 1-16
    No-Load Operation 1-16
  Power Supply Connectors 1-17
Dimensions for Micro Channel Adapter 1-18

Notes:

Description

The IBM* Personal System/2* Model P75 is a self-contained, portable computer system with a built-in keyboard and a built-in plasma display. One diskette drive and one internal fixed disk drive are standard. With a built-in Small Computer System Interface (SCSI) on the system board, the Model P75 is capable of connecting up to six external I/O devices (fixed disk drive, optical disk drive, tape drive or printer). In addition, the system can support one external storage device.

The system board function consists of three logical elements: main logic board, plasma-display card, and processor card. The main logic board and the plasma-display card provide the following:

- Four Micro Channel* connectors
  - Two 32-bit connectors
  - Two 16-bit connectors
- Extended Graphics Array (XGA)
- DMA controller
- Parallel port, serial port, and diskette drive controllers
- Keyboard/mouse port
- SCSI device interface
- External storage device.

The processor card determines system performance and model/submodel byte information. The processor card contains:

- System microprocessor
- System clock
- Read-only memory basic input/output system (ROM BIOS).

---

* IBM, Personal System/2, and Micro Channel are trademarks of the International Business Machines Corporation.

Programs identify the type of system board by reading the model and the submodel byte. Interrupt hex 15, function code (AH) = hex C0, returns this information. The following shows the system information of the Model P75.

Model Byte	Submodel Byte	Revision Code	Micro Processor	System Clock
F8	52	00	i486	33 MHz

Figure 1-1. Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems, and check the supplements section for updates to that listing.

System Board Features

The following figure lists the system board devices and features. The *Hardware Interface Technical Reference* describes devices common to PS/2 products.

Device	Feature
Microprocessor	80486 at 33MHz 32-bit address and 32-bit data interface
Processor Cache	8KB internal cache, 4-way set associative
Math Coprocessor	Internal floating point coprocessor (compatible with 80387) No optional math coprocessor
System Timers	Channel 0 – System timer Channel 2 – Tone generation for speaker Channel 3 – Watchdog timer
ROM Subsystem	128KB (KB = 1024 bytes)
RAM Subsystem	8MB on the system board (MB = 1,048,576 bytes) Expandable on the system board or channel up to 16MB
CMOS RAM Subsystem	64-byte CMOS RAM with real-time clock/calendar 2KB CMOS RAM extension Battery backup
Video Subsystem	XGA (IMB Video Memory) PDPC (Plasma Display Panel Control)
Audio Subsystem	Driven by: • System-timer channel 2 • Micro Channel, 'audio sum node' signal
DMA Controller	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	Supports: • 720KB formatted diskette density • 1.44MB formatted diskette density Auxiliary connector for an external storage device
Serial Controller	RS-232C interface Programmable as serial ports 1 to 8 FIFO mode and character mode

Figure 1-2 (Part 1 of 2). System Board Devices and Features

Device	Feature
Parallel Controller	Programmable as parallel ports 1 to 4 Supports bidirectional input and output
SCSI Controller	Refer to the *IBM PS/2 Micro Channel SCSI Adapter Technical Reference*, S68X-2397.
Micro Channel	Four channel connectors: • Two 16-bit connector for half-length adapter card • One 32-bit connector with matched-memory extension • One 32-bit connecter with Auxiliary Video Extension
Power Supply	110 and 220 Vac support

Figure 1-2 (Part 2 of 2). System Board Devices and Features

System Board Block Diagram

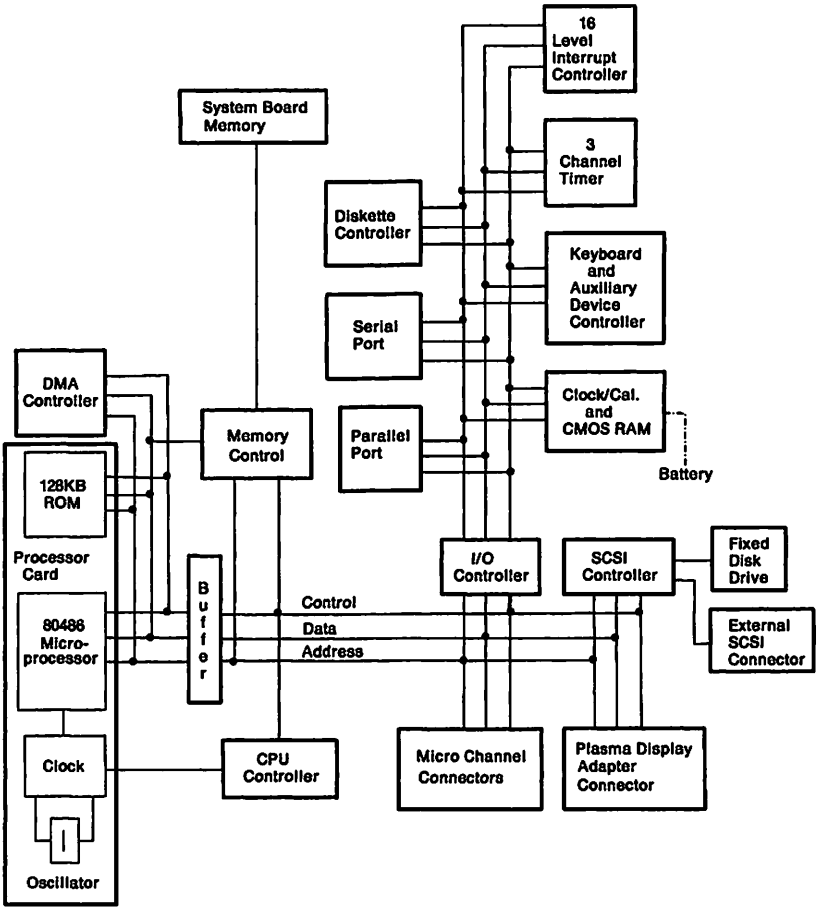


Figure 1-3. System Board

Note: Additional memory can be added in the 32-bit Micro Channel connectors. However, the total amount of memory installed should not exceed the 16MB addressing limit of the DMA controller.

System Board I/O Address Map

Hex Addresses	Device
0000 - 001F	DMA Controller (0 – 3)
0020, 0021	Interrupt Controller (Master)
0040, 0042 - 0044, 0047	System Timers
0060	Keyboard, Auxiliary Device
0061	System Control Port B
0064	Keyboard, Auxiliary Device
0070, 0071	RT/CMOS and NMI Mask
0081 - 0083, 0087	DMA Page Registers (0 – 3)
0089 - 008B, 008F	DMA Page Registers (4 – 7)
0090	Central Arbitration Control Point
0091	Card Selected Feedback Register
0092	System Control Port A
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
00A0 - 00A1	Interrupt Controller (Slave)
00C0 - 00DF	DMA Controller (4 – 7)
00E0 - 00E3	Memory Encoding Registers
00F0 - 00FF	Math Coprocessor
0100 - 0107	Programmable Option Select
0278 - 027B	Parallel Port 3
02F8 - 02FF	Serial Port 2 (RS-232C)
0378 - 037B	Parallel Port 2
03B4, 03B5, 03BA	Video Subsystem
03BC - 03BF	Parallel Port 1
03C0 - 03C5	Video Subsystem
03C6 - 03C9	Video DAC
03CA, 03CC, 03CE, 03CF	Video Subsystem
03D4, 03D5, 03DA	Video Subsystem
03F0 - 03F7	Diskette Drive Controller
03F8 - 03FF	Serial Port 1 (RS-232C)
2100 - 217F	Video Subsystem
1378 - 137B	Parallel Port 4
3220 - 3227	Serial Port 3
3228 - 322F	Serial Port 4
4220 - 4227	Serial Port 5
4228 - 422F	Serial Port 6
5220 - 5227	Serial Port 7
5228 - 522F	Serial Port 8

Figure 1-4. System Board I/O Address Map

Device					Clock Counts	Cycle Time (ns)
Microprocessor (33 MHz – 30 ns Clock):						
Access to System Board RAM*:						
Type	*Read /Write*	*Cache Fill*	*Interleave*	*Page Hit*	*Clock Count*	
A	Read	Yes	Yes	Hit	4-1-1-1	210
B	Read	Yes	Yes	Miss	7-1-1-1	300
C	Read	Yes	No	Hit	4-2-2-2	300
D	Read	Yes	No	Miss	7-2-2-2	390
E	Read	No	N/A	Hit	4	120
F	Write	No	N/A	Hit	5	150
G	N/A	No	N/A	Miss	7	210
Access to Channel:						
Default Transfer Cycle					9	270
Synchronous Extended Transfer Cycle					12	360
Refresh Rate						500 (min)
(Typically performed every 15.1 μs)						
Bus Master Access to System Board RAM						300 (min)
DMA Controller (10 MHz – 100 ns Clock):						
Single Transfer: 300 + I/O Access + Memory Access						
Burst Transfers: 300 + (I/O Access + Memory Access)N **						
System Board Memory Access						300
Default Transfer Cycle						200
Extended Transfer Cycle						300

* Adapters installed in the channel should not rely on monitoring system board memory accesses because channel memory control signals may not be present during these accesses.

** N is the number of transfers in the burst.

Figure 1-5. Performance Specifications

Size:	
Width	465 mm (18.3 in.)
Depth	156.0 mm (6.1 in.)
Height	305 mm (12.0 in.)
Air Temperature:	
System On	10.0 to 40.0°C (50 to 104°F)
System Off	10.0 to 50.0°C (50 to 125°F)
Humidity:	
System On	8% to 80%
System Off	8% to 80%
Maximum Altitude	2133.6 m (7000 ft.)
Heat Output	220 W
Acoustical Readings	See Figure 1-7 on page 1-11.
Electrical:	
Power Supply Input:	
Low Range	90 (min) - 137 (max) Vac
High Range	180 (min) - 265 (max) Vac
Maximum Current Draw:	
Low Range	5.0 A
High Range	3.0 A
Frequency	50 ±3Hz/60 ±3 Hz
Maximum Current Allowable:	
Keyboard Port	275 mA
Auxiliary Device Port	300 mA
Electromagnetic Compatibility	FCC Class B / VCCI Class 2 / VDE GOP

Figure 1-6. Physical Specifications

Description	L_{WAd} in bels Operate	Idle	L_{pAm} in dB Operate	Idle	$<L_{pA}>_m$ in dB Operate	Idle
Model P75	5.5	5.3	48	43	42	40

Notes:

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

These measurements are preliminary and subject to change.

Figure 1-7. Acoustical Readings

Micro Channel Compatibility

The following describes the way the system implements the Micro Channel architecture.

Procedures

The Micro Channel procedures supported are:

- Arbitration
- Basic Transfer
- Direct Memory Access
- Interrupt
- Refresh
- System Configuration
- Channel Reset.

Buses and Extensions

The following shows the Micro Channel buses and extensions supported for the 16-bit and 32-bit connectors. The top of the figure represents signal protocols supported; the bottom identifies the extensions provided.

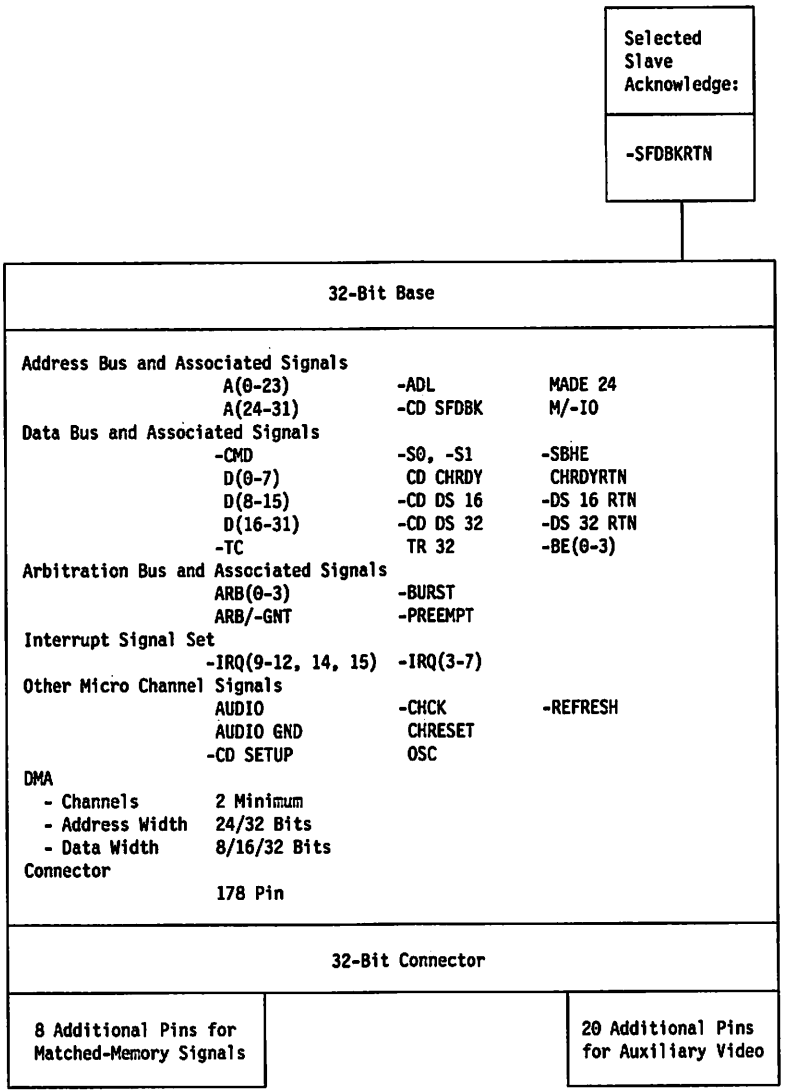


Figure 1-8. The 32-bit Connector

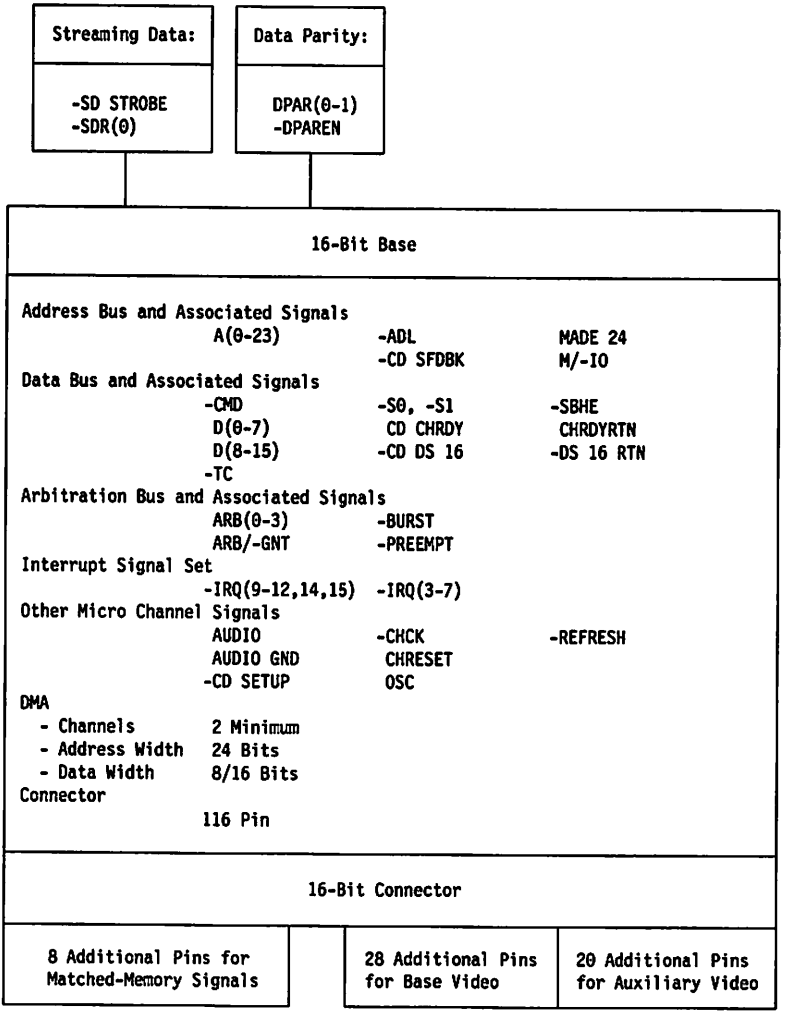


Figure 1-9. The 16-bit Connector

Power Supply

The power supply converts the ac input voltage to six dc output voltages: +5 V dc, +5 V dc (for plasma display), +12 V dc, −12 V dc, −175 V dc, −180 V dc. The power supply provides power for the following:

- System board
- Channel adapters
- Diskette drives
- Fixed disk drives
- Auxiliary device
- Plasma-display
- Keyboard.

The power switch and one light-emitting diode (LED) is on the front of the computer. The power supply is operating when the green LED is lit.

Input Protection

The input power line is protected against an overcurrent condition by an internal fuse.

Ground-Leakage Current

The system-ground-leakage current does not exceed 500 microamperes at any nominal input voltage.

Output Protection

A short circuit placed on any dc output (between outputs or between an output and dc return) shuts down all dc outputs with no damage to the power supply.

If an overvoltage fault occurs within the power supply, all dc outputs are shut down before any output exceeds 130% of its nominal value.

If the power supply is shut down, it returns to normal operation only after the fault has been removed and the power has been turned off for at least 1 second.

Voltage Sequence

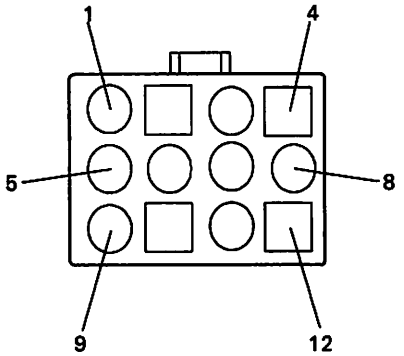
At power-on time, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

No-Load Operation

The power supply is capable of operation with *no load* on the outputs. The output regulation is ±25%, and the 'power-good' signal can be either active or inactive.

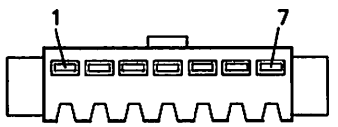
Power Supply Connectors

The power supply uses a 12-pin connector for the system board and a 7-pin connector for the plasma display.



Pin	Signal	Pin	Signal
1	−12 Vdc	7	Not connected
2	+12 Vdc	8	GND
3	+5 Vdc	9	GND
4	+5 Vdc	10	GND
5	+5 Vdc	11	GND
6	Not connected	12	Power Good

Figure 1-10. System-Board Power Supply Connector



Pin	Signal
1	GND
2	+5 Vdc
3	Not connected
4	+5 Vdc
5	Not connected
6	−175 Vdc
7	−180 Vdc

Figure 1-11. Plasma-Display Power-Supply Connector

Dimensions for Micro Channel Adapter

The system board provides channel connectors to support the following types of adapters.

- 16 bit adapter (half-length)
- 32 bit adapter (full-length)

The following figures show the dimensions of the half-length adapter card and it's retainer. The other dimensions (that is, connector dimensions, holder dimensions) are the same as the standard size (full-length) adapter card dimensions that are described in the *Hardware Interface Technical Reference.*

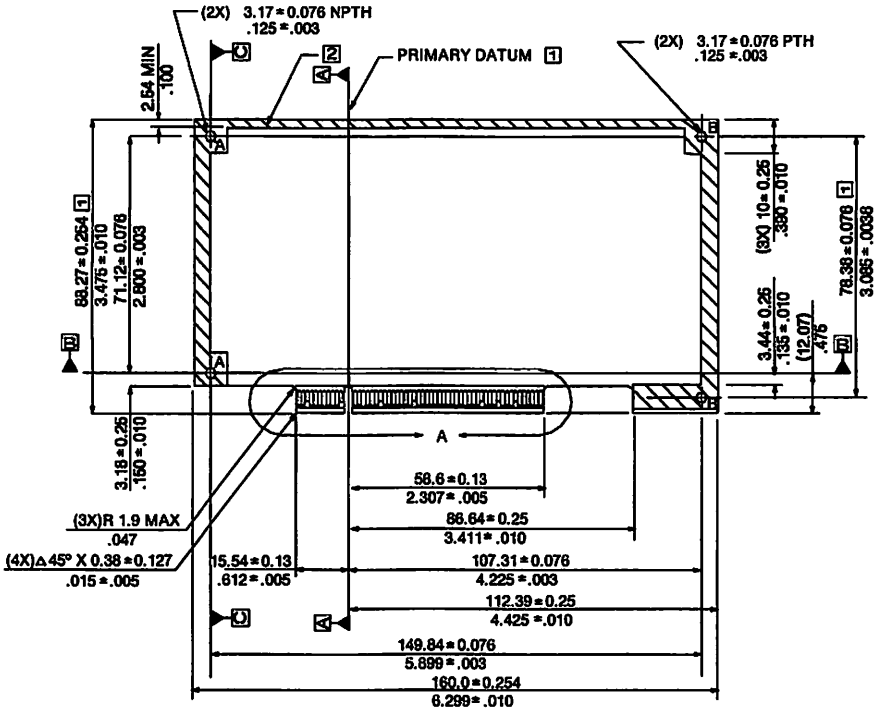


Figure 1-12. Adapter Dimensions (Half-Length)

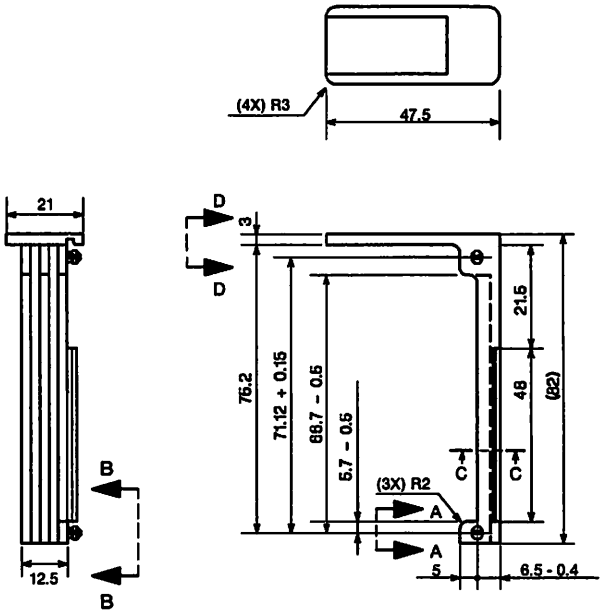


Figure 1-13 (Part 1 of 2). Adapter Retainer

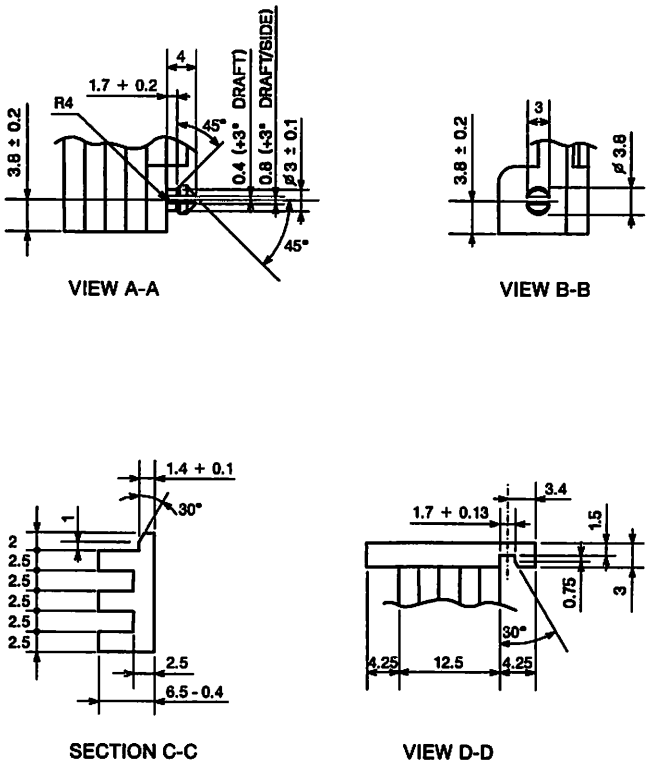
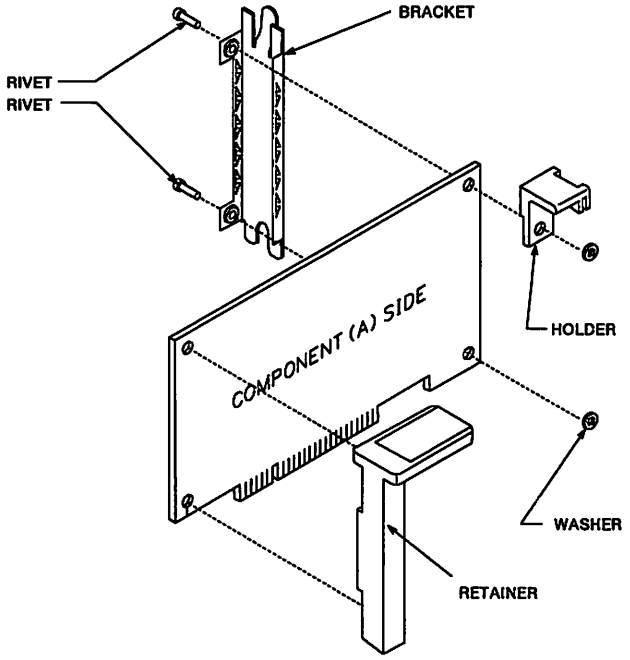


Figure 1-13 (Part 2 of 2). Adapter Retainer



MATERIALS:
HOLDER AND RETAINER - POLYCARBONATE UL 94 V-0
BRACKET - AISI TYPE 302 1/4 HARD STAINLESS STEEL

Figure 1-14. Typical Adapter Assembly

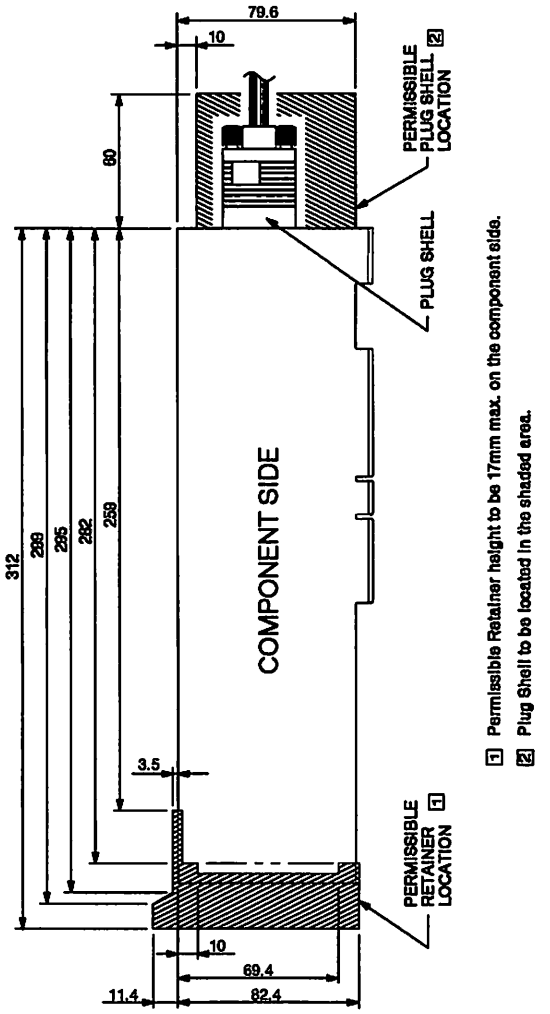
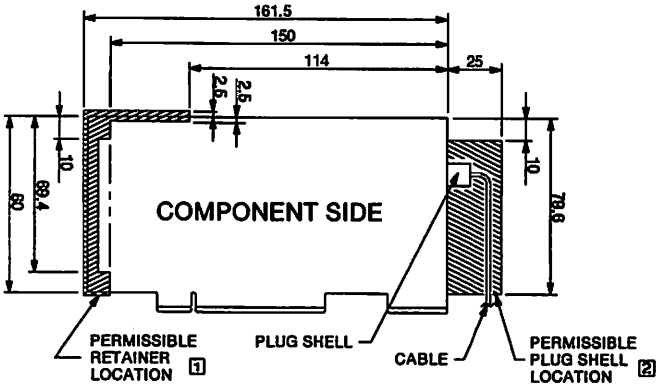


Figure 1-15. Permissive Areas (Full-Length Adapter)



1 Permissible Retainer height to be 17mm max. on the component side.

2 Plug Cable to be bent by 90° in the shaded area.

Figure 1-16. Permissive Areas (Half-Length Adapter)

Section 2. Programmable Option Select

Description 2-3
POS Address MAP 2-4
Card Selected Feedback 2-5
System Board Setup 2-6
- System Board Enable/Setup Register (Hex 0094) 2-6
- Adapter Enable/Setup Register (Hex 0096) 2-8
- System Board Functions 2-9
- System Board POS Register 0 (Hex 0100) 2-9
- System Board POS Register 1 (Hex 0101) 2-9
- System Board POS Register 2 (Hex 0102) 2-10
- System Board POS Register 3 (Hex 0103) 2-12
  - POS Register 3 as a Write Port 2-12
  - POS Register 3 as a Read-Only Port (Bank 1) 2-13
  - POS Register 3 as a Read-Only Port (Bank 2) 2-13
- Memory Presence Detect 2-14
- I/O Controller Functions 2-15
- I/O Controller POS Register 2 (Hex 0102) 2-16
- I/O Controller POS Register 3-1 (Hex 0103), Index 0000 2-17
- I/O Controller POS Register 4-1 (Hex 0104), Index 0000 2-18
- I/O Controller POS Register 3-3 (Hex 0103), Index 0002 2-19

Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used on the Model P75 system boards. For additional POS information, refer to the *Hardware Interface Technical Reference*.

Setup functions respond to I/O addresses hex 0100 through 0107 only when their unique setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

Important

- IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignment of the same system resource, improper operation of the feature, loss of data, or possible damage to the hardware.
- Application programs should not use the adapter identification unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention will occur, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, set the Adapter Enable/Setup register (hex 0096) to hex 00, and the System Board Enable/Setup register (hex 0094) to hex FF.
- Bit 7 (channel reset) in the Adapter Enable/setup register must be 0 to program the adapters.
- Only 8-bit instructions are supported for setup operations. Using 32- or 16-bit I/O instructions on 8-bit POS registers cause erroneous data to be written or read.

POS Address MAP

The following table shows the organization of the I/O address space used by POS. Bit 0 of POS Register 2, and bits 6 and 7 of POS Register 5 are fixed. All other bits in POS Registers 2 through 5 are free-form.

Address (Hex)	Function
0091	Card Selected Feedback Register
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
00E0 - 00E3	Memory Encoding Registers (See "System Board" section.)
0100	POS Register 0 - Adapter Identification Byte (Low Byte)
0101	POS Register 1 - Adapter Identification Byte (High Byte)
0102	POS Register 2 - Option Select Data Byte 1
0103	POS Register 3 - Option Select Data Byte 2
0104	POS Register 4 - Option Select Data Byte 3
0105	POS Register 5 - Option Select Data Byte 4
0106	POS Register 6 - Subaddress Extension (Low Byte)
0107	POS Register 7 - Subaddress Extension (High Byte)

Figure 2-1. POS I/O Address MAP

Card Selected Feedback

When an adapter is addressed, it responds by setting the '-Card Selected Feedback' signal (-CD SFDBK) to active. -CD SFDBK is derived from the address decode and driven by a totem pole driver. It is latched by the system board and can be read through the Card Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and thereby determine if the video subsystem, system board I/O, or an adapter is addressed and functioning.

Bit	Function
7 – 1	Reserved
0	–Card Selected Feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7-1 These bits are reserved.

Bit 0 This bit is set to 1 whenever -CD SFDBK was active on a previous cycle or whenever the system board I/O function (diskette drive, serial, or parallel interface) is accessed by an I/O cycle. Reading this register resets the bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information during setup. The System Board Enable/Setup register is used to place the system board or the video subsystem into the setup mode.

System Board Enable/Setup Register (Hex 0094)

This is a read/write register. All bits in this register default to 1 (enabled).

Bit	Function
7	Enable/-Setup System Board Functions
6	Enable/-Setup I/O Controller Functions
5	Enable/-Setup Video Subsystem
4	Enable/-Setup Plasma Display Controller
3	Reserved
2	Reserved
1	Reserved
0	Reserved

Figure 2-3. System Board Enable/Setup Register (Hex 0094)

Bit 7 When this bit is set to 0, the system board function is placed in the setup mode.

When this bit is set to 1, the system board function is enabled.

Bit 6 When this bit is set to 0, the system board I/O controller is placed in the setup mode. The diskette drive controller, serial port, and parallel port are controlled through System Board I/O POS registers.

When this bit is set to 1, the system board I/O functions are enabled.

Bit 5 When this bit is set to 0, the video subsystem is placed in the setup mode and controlled through POS Register 2 (hex 0102). When set to 1, and bit 0 in hex 0102 is set to 1, video is enabled.

Bit 0 of POS Register 2 is the video enable bit. When this bit is set to 0, the video subsystem does not respond to commands, addresses, or data. If video is being generated when the video enable bit is set to 0, the output is still generated. For information on BIOS calls to enable or disable the video, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Bit 4 When this bit is set to 0, the plasma display controller is placed in the setup mode.
When this bit is set to 1, the plasma display controller is enabled.

Bits 3 - 0 These bits are reserved and must be 1.

Adapter Enable/Setup Register (Hex 0096)

This read/write register selects the connector to be configured.

Bit	Function
7	Channel Reset
6 - 4	Reserved
3	Card Setup Enable
2 - 0	Channel Select 2 - 0

Figure 2-4. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When this bit is set to 1, this bit activates the Channel Reset signal to all connectors.

Bit 6 - 4 These bits are reserved.

Bit 3 When set to 1, this bit enables the '-Card Setup' signal selected by bits 2 through 0.

Bit 2 - 0 These bits are the address bits for the '-Card Setup' signal, connectors 1 through 4 are addressed as 0 through 3, respectively.

Each channel connector has a unique '-Card Setup' signal (-CD SETUP) associated with it. This signal is used to put the adapters in the setup mode, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Notes:

1. -CD SETUP goes active only when an operation is performed in the I/O address range hex 0100 through 0107.
2. The status of port hex 0096 can be read by software. However, When the port is read, bit 6, 5, and 4 are set to 1.

System Board Functions

System Board Functions are controlled by the following POS registers.

- Hex 0100: POS Register 0, Planar Board ID Byte (Low Byte)
- Hex 0101: POS Register 1, Planar Board ID Byte (High Byte)
- Hex 0102: POS Register 2, Option Select Data Byte 1
- Hex 0103: POS Register 3, Option Select Data Byte 2

Note: The above four registers are controlled by bit 7 of the System Board Enable/Setup register (Hex 0094).

System Board POS Register 0 (Hex 0100)

When the system board is in the setup mode, the planar ID (Low Half) can be read from this register. The Planar ID for Model P75 is E0FFh.

Bit	Function
7 - 0	Planar ID (Low Byte), Value is FF for Model P75

Figure 2-5. System Board POS Register 0 (Hex 0100)

System Board POS Register 1 (Hex 0101)

When the system board is in the setup mode, the planar ID (High Half) can be read from this register.

Bit	Function
7 - 0	Planar ID (High Byte), Value is E0 for Model P75

Figure 2-6. System Board POS Register 1 (Hex 0101)

System Board POS Register 2 (Hex 0102)

When the system board is in the setup mode, the diskette drive controller, serial port, and parallel port are controlled by this read/write register. Reading this register returns the current state of three system board functions.

Bit	Function
7	Disable Parallel Port Extended Mode
6, 5	Parallel Port Select
4	Enable Parallel Port
3	Reserved
2	Enable Serial Port
1	Enable Diskette Drive Interface
0	Enable System Board

Figure 2-7. System Board POS Register 2 (Hex 0102)

Bit 7 When set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional interface. When set to 1, this bit disables the bidirectional mode. This bit is set to 0 at power-on and POST sets it to 1.

Bits 6,5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Hex Address	Interrupt Level
0 0	Parallel 1	03BC - 03BF	7
		(1278 - 127F)	7
0 1	Parallel 2	0378 - 037B	7
1 0	Parallel 3	0278 - 027B	7
1 1	Parallel 4	1378 - 137B	7

Figure 2-8. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bit 3 This bit is reserved and must be set to 0.

Bit 2 When this bit and bit 0 are set to 1, the the system board serial port is enabled.

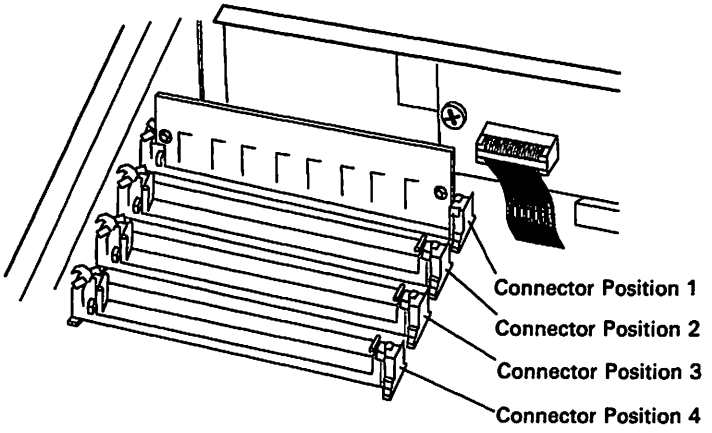
Bit 1 When this bit and Bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When set to 1, this bit allows bits 4, 2, and 1 to enable and disable their respective devices. When set to 0, this bit disables the diskette drive interface, system board serial port, and system board parallel port regardless of the state of bits 4, 2, and 1.

System Board POS Register 3 (Hex 0103)

This port contains information about the presence and type of memory module installed on the system board. The bank selector and Fast Refresh control bits are in this write register.

The memory connectors are numbered from top to bottom as viewed from the back of the system.



POS Register 3 as a Write Port

Bit	Function
7 - 2	Reserved
1	Reserved
0	Bank Select

Figure 2-9. POS Register 3 as a Write Port

Bits 7 - 1 These bits are reserved.

Bit 0 When set to 0, the bank 1 is selected; when set to 1, the bank 2 is selected in this write register.

POS Register 3 as a Read-Only Port (Bank 1)

When bit 0 of the POS register 3 (write) is set to 0, this register indicates the presence of data in the bank 1.

Bit	Function
7	SIMM 3, Presence Detect bit 3
6	SIMM 3, Presence Detect bit 2
5	SIMM 3, Presence Detect bit 1
4	SIMM 3, Presence Detect bit 0
3	SIMM 1, Presence Detect bit 3
2	SIMM 1, Presence Detect bit 2
1	SIMM 1, Presence Detect bit 1
0	SIMM 1, Presence Detect bit 0

Figure 2-10. POS Register 3 as a Read-Only Port (Bank 1)

Bits 7 - 4 These bits indicate the state of the 'Presence Detect bits 3 - 0' signals for connector position 3 (SIMM 3).

Bits 3 - 0 These bits indicate the state of the 'Presence Detect bits 3 - 0' signals for connector position 1 (SIMM 1).

POS Register 3 as a Read-Only Port (Bank 2)

When bit 0 of the POS register 3 (write) is set to 1, this register indicates the presence of data in the bank 2.

Bit	Function
7	SIMM 4, Presence Detect bit 3
6	SIMM 4, Presence Detect bit 2
5	SIMM 4, Presence Detect bit 1
4	SIMM 4, Presence Detect bit 0
3	SIMM 2, Presence Detect bit 3
2	SIMM 2, Presence Detect bit 2
1	SIMM 2, Presence Detect bit 1
0	SIMM 2, Presence Detect bit 0

Figure 2-11. POS Register 3 as a Read-Only Port (Bank 2)

Bits 7 - 4 These bits indicate the state of the 'Presence Detect bits 3 - 0' signals for connector position 4 (SIMM 4).

Bits 3 - 0 These bits indicate the state of the 'Presence Detect bits 3 - 0' signals for connector position 2 (SIMM 2).

Memory Presence Detect

The presence detect signals are used by the system to determine size and speed of the memory card. The pins are either connected to ground or not connected.

A set of four bits shows the state of all presence detect signals for a specific memory connector; the bit is 0 when the signal grounded. The following table shows the information indicated by these bits.

Presence Detect 3 2 1 0	Function
1 1 0 0	2MB 70-ns Memory
0 1 0 0	4MB 70-ns Memory

Figure 2-12. Memory Presence Detect

I/O Controller Functions

I/O Controller Functions can be programmed. They are enabled and disabled by the following POS registers.

- Hex 0102: POS Register 2, I/O Controller Enable Register
- Hex 0103: POS Register 3-1, I/O Controller Diskette Drive Interface Setup
- Hex 0104: POS Register 4-1, I/O Controller Parallel Port Setup
- Hex 0103: POS Register 3-3, I/O Controller Port A Address Setup
- Hex 0106: POS Register 6, Subaddress Extension (Low Byte)
- Hex 0107: POS Register 7, Subaddress Extension (High Byte)

Note: The above seven registers are controlled by bit 6 of the system board enable/setup register (Hex 0094).

POS register 3-1, 3, 4, and 4-1, are selected by POS register 6 and 7 as follows.

Index	POS 7 (High) (Hex 0107)	POS 6 (Low) (Hex 0106)	Address	Function
0000	00	00	0103	Diskette Drive Interface Setup
0000	00	00	0104	Parallel Port Setup
0001	00	01	0103	Reserved
0001	00	01	0104	Reserved
0002	00	02	0103	Serial Port Address Setup
0002	00	02	0104	Reserved

Figure 2-13. I/O Controller Function

I/O Controller POS Register 2 (Hex 0102)

When the I/O Controller is in the setup mode, the diskette drive, serial port, and parallel port are controlled by this read/write register.

Bit	Function
7	Reserved
6	Include/-Exclude Mouse IRQ signal
5	Enable/-Disable I/O Controller Keyboard and Mouse controller
4	Enable/-Disable I/O Controller Parallel Port
3	Reserved
2	Enable/-Disable I/O Controller Serial Port A
1	Enable/-Disable I/O Controller Diskette Drive Interface
0	Reserved

Figure 2-14. I/O Controller POS Register 2 (Hex 0102)

Bit 7 This bit is reserved.

Bit 6 When set to 1, this bit allows the 'PDPC auto dim reset' signal to include the Mouse IRQ (Keyboard + Mouse IRQs). When set to 0, the PDPC auto dim reset signal is driven by the keyboard IRQ only (see the PDPC section).

Bit 5 When set to 1, the I/O Controller keyboard and mouse controller is enabled. When set to 0, the I/O Controller keyboard and mouse controller is disabled.

Bit 4 When set to 1, the I/O Controller parallel port is enabled. When set to 0, the I/O Controller parallel port is disabled.

Bit 3 This bit is reserved and must be set to 1.

Bit 2 When set to 1, the I/O Controller serial port is enabled. When set to 0, the I/O Controller external serial port A is disabled.

Bit 1 When set to 1, the I/O Controller diskette drive interface is enabled. When set to 0, The I/O Controller diskette drive interface is disabled.

Bit 0 This bit is reserved and must be set to 1.

Note: All bits are set to 0 at power-on.

I/O Controller POS Register 3-1 (Hex 0103), Index 0000

When the I/O Controller is in the setup mode, the diskette drive controller interface is controlled by this read/write register.

Bit	Function
7	Reserved
6	Enable/-Disable Diskette Burst Mode
5	Reserved
4	Enable/-Disable Diskette Arbitration Fairness
3 - 0	Diskette Arbitration Level Select

Figure 2-15. I/O Controller POS Register 3-1 (Hex 0103)

Bit 7 This bit is reserved and must be 1.

Bit 6 When set to 1, the diskette burst mode is enabled. When set to 0, the diskette burst mode is disabled.

Bit 5 This bit is reserved and must be 0.

Bit 4 When set to 1, the diskette arbitration fairness is enabled. When set to 0, the diskette arbitration fairness is disabled.

If this bit is set to 1, Bit 6 must also be set to 1.

Bits 3 - 0 These bits select the arbitration level of the diskette interface from arbitration level 0H to FH. Bit 0 is LSB, bit 3 is MSB. Arbitration level 2H is selected at power-on.

I/O Controller POS Register 4-1 (Hex 0104), Index 0000

When the I/O Controller is in the setup mode, the parallel port arbitration level is selected by this read/write register.

Bit	Function
7 - 5	Reserved, must be 0
4	Reserved, must be 1
3 - 0	Parallel Port arbitration Level Select

Figure 2-16. I/O Controller POS Register 4-1 (Hex 0104)

Bits 7 - 4 These bits are reserved.

Bits 3 - 0 These bits select the arbitration level of the parallel port from arbitration level 0H to FH. Bit 0 is LSB, bit 3 is MSB. Arbitration level 6H is selected at power-on.

I/O Controller POS Register 3-3 (Hex 0103), Index 0002

When the I/O Controller is in the setup mode, the serial port address is selected by this read/write register.

Bit	Function
7 - 4	Reserved
3	Serial Port IRQ Select
2 - 0	Serial Port Address Select

Figure 2-17. I/O Controller POS Register 3-3 (Hex 0103)

Bit 7 - 4 These bits are reserved.

Bit 3 This bit selects IRQ level of the serial ports.

Bit 3	Serial Port
0	IRQ 3
1	IRQ 4

Figure 2-18. I/O POS Register 3-3 (Hex 0103), Bit 3

Bits 2 - 0 These bits select the serial port 1 address. 0H is selected at power-on.

Bits 2 1 0	Address
0 0 0	03F8 - 03FF
0 0 1	02F8 - 02FF
0 1 0	3220 - 3227
0 1 1	3228 - 322F
1 0 0	4220 - 4227
1 0 1	4228 - 422F
1 1 0	5220 - 5227
1 1 1	5228 - 522F

Figure 2-19. I/O POS Register 3-3 (Hex 0103), Bit 2 through 0

Section 3. System Board

Description 3-3
Micro Channel 3-3
  Matched-Memory Cycles 3-3
  Central Arbiter 3-3
    Arbitration Bus Priority Assignments 3-3
    Central Arbiter Programming 3-4
  Diskette Drive and Fixed Disk Drive Connectors 3-6
    Internal Diskette Drive Connector 3-7
    External Storage Device Connector 3-8
    Fixed Disk Drive Connector 3-9
Memory 3-10
  Read-Only Memory Subsystem 3-10
  Random Access Memory Subsystem 3-11
  System and Non-system Memory 3-11
  Memory Caching 3-12
  Memory Requirements and Limitations 3-14
  Interleave Operation 3-14
  Error Recovery 3-16
  Memory Subsystem Control 3-17
    Memory Encoding Register 1 (Hex 00E0) 3-17
    Memory Encoding Register 2 (Hex 00E1) 3-18
    Memory Encoding Register 3 (Hex 00E2) 3-19
    Memory Encoding Register 4 (Hex 00E3) 3-21
  System Memory Maps 3-22
    System Memory Map 1 3-23
    System Memory Map 2 3-24
    System Memory Map 3 3-25
    System Memory Map 4 3-25
    System Memory Map 5 3-26
    System Memory Map 6 3-26
    System Memory Map 7 3-27
    System Memory Map 8 3-28
  System Board Memory Connectors 3-29
  Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM 3-31
    RT/CMOS Address Register and NMI Mask (Hex 0070) 3-32
    RT/CMOS Data Register (Hex 0071) 3-32
    RT/CMOS RAM I/O Operations 3-33
    Real-Time Clock Bytes (Hex 000-00D) 3-34

CMOS RAM Configuration 3-38
SCSI Port 3-43
Connector Pin Assignment 3-44
Termination Resistors 3-45
Miscellaneous System Functions 3-46
Nonmaskable Interrupt 3-46
System Control Port B (Hex 0061) 3-46
System Control Port A (Hex 0092) 3-48
Power-On Password 3-50
Hardware Compatibility 3-51
POST Error Codes 3-53

Description

This section describes channel differences, I/O device connectors, memory subsystems, and miscellaneous system ports for the Model P75. For additional information about these and other topics, refer to the *Hardware Interface Technical Reference.*

Micro Channel

This section describes the implementation of the Micro Channel architecture on Model P75 systems. For general Micro Channel information, refer to the *Hardware Interface Technical Reference.*

Matched-Memory Cycles

The 32-bit channel connector has a matched-memory extension. The system microprocessor activates the '-Matched Memory Cycle' signal (-MMC) when it does a memory access. This allows the Model P75 to support the same memory adapter design as the PS/2 Model 80 system board.

Although a memory adapter can respond to -MMC active by driving the '-Matched Memory Cycle Request' signal (-MMCR) active, the Model P75 system board ignores -MMCR and performs a default cycle if the 'channel ready' signal (CD CHRDY) is active, or a synchronous-extended cycle if CD CHRDY is inactive. The Model P75 also drives the '-Matched Memory Cycle Command' signal (-MMC CMD) active at the same time as the '-command' signal (-CMD).

Central Arbiter

The central arbitration control point gives devices on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. This arbiter supports up to 16 arbitrating devices.

Arbitration Bus Priority Assignments

The following figure shows the assignment of arbitration levels. The functions with the lowest arbitration level have the highest priority.

ARB Level	Primary Assignment
-2	Memory Refresh
-1	NMI
0	DMA Channel 0 (Programmable to any arbitration level)
1	DMA Channel 1
2	DMA Channel 2
3	DMA Channel 3
4	DMA Channel 4 (Programmable to any arbitration level)
5	DMA Channel 5
6	DMA Channel 6
7	DMA Channel 7
8 - E	Available
F	System Microprocessor

Figure 3-1. Arbitration Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation, and by the previous controlling master. The diskette drive controller should not be held inactive for more than 12 microseconds to prevent overrun.

NMI service is executed at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'Arbitrate/-Grant' signal is in the arbitrate state.

When the central arbitration control point receives a level -1 request (NMI, a system-board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places the 'Arbitrate/-Grant' signal in the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level -1 request, and holds 'Arbitrate/-Grant' signal in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following figures.

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Mask
5	Enable Extended Arbitration
4 - 0	Reserved

Figure 3-2. Arbitration Register (Hex 0090)-Write

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Masked by NMI
5	Bus Time-out
4	Reserved
3 - 0	Value of Arbitration Bus During Previous Grant State.

Figure 3-3. Arbitration Register (Hex 0090)-Read

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 enables extended arbitration. The minimum arbitration cycle is 300 nanoseconds; this bit extends that minimum cycle to 600 nanoseconds. This bit is set to 0 during a system reset.

Reading this bit as a 1 indicates that a bus time-out has occurred, and resets bit 6 in this register to 0.

Bit 4 This bit is reserved and should be 0.

Bits 3 - 0 These bits are undefined for a write operation and should be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Diskette Drive and Fixed Disk Drive Connectors

The system board has a 2- by 17-pin connector for one internal diskette drive, a 30-pin connector for external diskette drive, and a 2 by 25-pin connector for an internal SCSI fixed disk drive.

The internal diskette drive connector passes control and data signals between the internal diskette drive and the diskette drive controller on the system board. Micro Channel signals necessary for fixed disk operations are present on the fixed disk connector. The external diskette drive attaches to the 30-pin connector, which passes the necessary signals from the diskette drive controller.

Internal Diskette Drive Connector

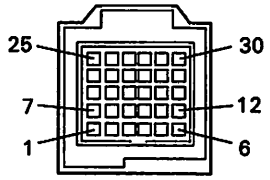
The following figure shows the signal assignment and pin numbering for the internal diskette drive connector on the system board. The internal diskette drive connector is a 2- by 17-pin connector that is numbered with the odd numbers on the top.

Pin	I/O	Signal	Pin	I/O	Signal
1	I	–2nd Drive Installed	2	O	–High Density Select
3	O	+5 Vdc	4	N/A	Reserved
5	N/A	Ground	6	O	+12 Vdc
7	N/A	Signal Ground	8	I	–Index
9	N/A	Signal Ground	10	N/A	Reserved
11	N/A	Signal Ground	12	O	–Drive Select
13	N/A	Ground	14	N/A	Reserved
15	N/A	Signal Ground	16	O	–Motor Enable
17	N/A	Signal Ground	18	O	–Direction In
19	N/A	Signal Ground	20	O	–Step
21	N/A	Signal Ground	22	O	–Write Data
23	N/A	Signal Ground	24	O	–Write Enable
25	N/A	Signal Ground	26	I	–Track 0
27	N/A	Signal Ground	28	I	–Write Protect
29	N/A	Signal Ground	30	I	–Read Data
31	N/A	Signal Ground	32	O	–Head 1 Select
33	N/A	Signal Ground	34	I	–Diskette Change

Figure 3-4. Internal Diskette Drive Connector

External Storage Device Connector

The following figure shows the signal assignment and pin numbering for the external storage device connector on the system board. This external storage device connector is a 30-pin connector located at the rear of the system unit. The system can support an external diskette drive through this connector.



Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Ground	2	I	–Second Drive Installed
3	N/A	Ground	4	O	+Reduced Write Current
5	N/A	Ground	6	N/A	Reserved
7	N/A	Ground	8	I	–Index
9	O	–Motor On 1	10	O	–Drive Select 1
11	N/A	Reserved	12	N/A	Reserved
13	N/A	Ground	14	O	–Direction
15	N/A	Ground	16	O	–Step
17	N/A	Ground	18	O	–Write Data
19	N/A	Ground	20	O	–Write Gate
21	N/A	Ground	22	I	–Track 00
23	N/A	Ground	24	I	–Write Protect
25	N/A	Ground	26	I	–Read Data
27	N/A	Ground	28	O	–Side 1 Select
29	N/A	Ground	30	I	–Diskette Change

Figure 3-5. External Storage Device Connector

Fixed Disk Drive Connector

The following figure shows the signal assignment and pin numbering for the fixed disk drive connector on the adapter. The fixed disk drive connector is a 2- by 25-pin connector. Side A of the connector is the top and Side B is the bottom.

Pin	Signal	Pin	Signal
1	Ground	2	– Data Bus (0)
3	Ground	4	– Data Bus (1)
5	Ground	6	– Data Bus (2)
7	Ground	8	– Data Bus (3)
9	Ground	10	– Data Bus (4)
11	Ground	12	– Data Bus (5)
13	Ground	14	– Data Bus (6)
15	Ground	16	– Data Bus (7)
17	Ground	18	– Data Bus (P)
19	Ground	20	Ground
21	Ground	22	Ground
23	Reserved	24	Reserved
25	Not used	26	Termpwr
27	Reserved	28	Reserved
29	Ground	30	Ground
31	Ground	32	– ATN
33	Ground	34	Ground
35	Ground	36	– BSY
37	Ground	38	– ACK
39	Ground	40	– RST
41	Ground	42	– MSG
43	Ground	44	–SEL
45	Ground	46	–C/D
47	Ground	48	–REG
49	Ground	50	–I/O

Figure 3-6. Fixed Disk Connector

Notes:

1. Reserved pins are at ground on the device side.
2. The minus sign next to a signal indicates active low.

Memory

The Model P75 uses the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- Real-time clock and CMOS RAM.

Read-Only Memory Subsystem

The ROM subsystem consists of 128KB. At power-on, ROM is active in two address spaces: hex 000E0000 to 000FFFFF and hex FFFE0000 to FFFFFFFF. After POST ensures the proper operation of system memory, the ROM code is copied to RAM. ROM is then disabled, and the RAM responds to the ROM address. This RAM is write protected.

ROM or RAM access at address space hex 000E0000 to 000FFFFF is controlled by the ROMEN bit in Memory Encoding Register 2 (hex 00E1). When enabled, ROM is not parity-checked and operates with a minimum of 200 nanoseconds in wait states.

A snoop address protocol is in ROM address to keep the 486 microprocessor's cache contents consistent with RAM subsystem.

Random Access Memory Subsystem

The RAM subsystem on the system board starts at address hex 00000000 of the address space. The RAM subsystem is 36 bits wide: 32 data bits and 4 parity bits. One parity bit is generated for each byte of data written. During a read operation, one parity bit is checked for each byte of data read by the device controlling the bus.

The Model P75 enables and disables memory in 2MB blocks. Each 2MB block must start on a 2MB boundary.

System and Non-system Memory

Two basic types of memory can be assigned addresses within the memory address space: system memory and non-system memory.

System memory is memory that is managed and allocated by the primary operating system. It remains assigned to and fixed in the 4GB (GB equals 1,073,741,824 bytes) physical address space, and its contents can be accessed or modified only by an independent master(bus master, system microprocessor, or DMA controller).

Non-system memory is memory that is not managed or allocated by the primary operating system. It is made up of memory-mapped I/O devices, memory on an adapter that can be directly modified by the adapter, or memory that can be relocated within the address space, such as bank switched memory and EMS (expanded memory specifications).

Memory Caching

The following figure is the memory map for the first 16MB of address space on the system boards and shows which addresses can be used with the cache. The third and fourth GB are not mapped into the cache, but can be used, especially for non-system memory.

Within the first 16MB of address space, all system memory above 1MB must be one contiguous sum starting at the 1MB boundary. If non-system memory is present, it should be assigned addresses starting at 16MB and counting down. Do not assign addresses below 8MB to non-system memory.

If non-system memory exists between 8MB and 16MB, caching for that 8MB block must be disabled even if system memory is also located there. Setup routines must be aware of the existence and location of non-system memory so that POST can properly control the caching of the second 8MB.

In the 16MB to 4GB address space, system memory can be contiguously placed from 16MB up to 32MB and can be cached. If non-system memory is located within the 16MB to 4GB address space, it should be assigned addresses starting at 4GB and counting down, allowing space for system ROM.

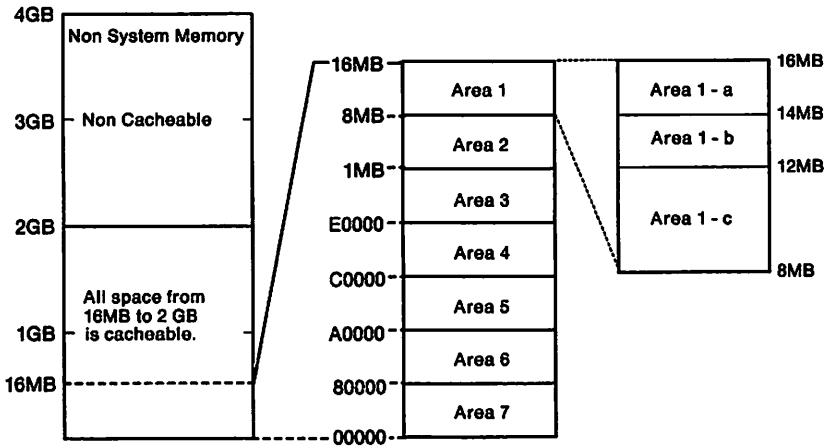


Figure 3-7. Memory Caching

Legend:

Area 1	Cached under program control (POST)
Area 2	Cached
Area 3	Not cached when ROMEN is active. Not cached (E0000-E0FFF) when DIS4K is active.
Area 4, 5	Not cached
Area 6, 7	Cached

Memory Requirements and Limitations

The four memory-module connectors on the system board accept 2MB and/or 4MB memory modules in any combination. However, they do not have to be fully populated by these memory modules. A minimum of 2MB memory area is required in the memory module that is installed either in connector position 1 or 2. If a 4MB memory module is in connector position 1 or 2, the system needs more than 2M bytes of usable memory.

Interleave Operation

The Model P75 has two modes of operation during cache-fill so the processor can work efficiently.

- Interleave mode

  This operational mode occurs only when the same capacity of memory modules exist in successive memory-module connectors as shown in Figure 3-8 on page 3-15.

- Non-interleave mode

  If any defective memory, or an absence of memory, module on either connector is found, the Non-interleave mode is assumed. See Figure 3-9 on page 3-15.

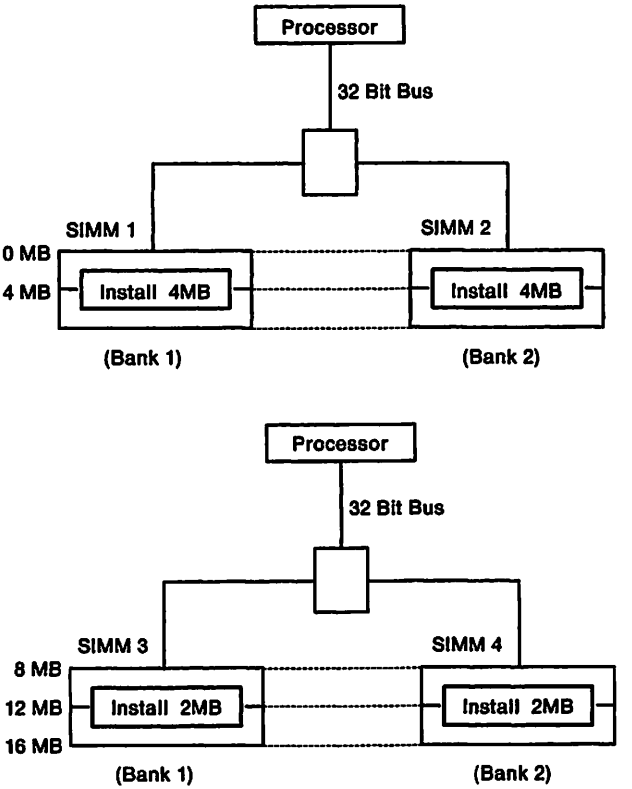


Figure 3-8. Example of the Interleave Operation

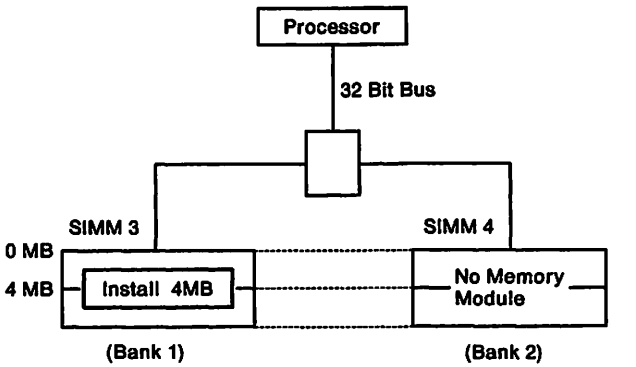


Figure 3-9. Example of the Non-Interleave Operation

Error Recovery

If POST detects a memory error in the first 512KB of memory, the first physical 2MB block of memory is deactivated. The addresses assigned to the deactivated block are reassigned to the second physical block of system board memory (the first 1MB of system memory must reside in connector 1 or 2). If 1MB of valid memory cannot be allocated from connector 1 or 2, the system cannot recover from the error. The first 1MB of memory address space cannot be assigned to memory on the channel.

POST does not deactivate a memory block if an error is detected in the second 512KB of that block. If an error is detected in that area of memory, the 1MB block containing the error can be deactivated and have its addresses reassigned by running the customer-level memory diagnostics program on the Reference Diskette supplied with the system. Once a block of memory is deactivated, it is ignored by POST on subsequent power-ons.

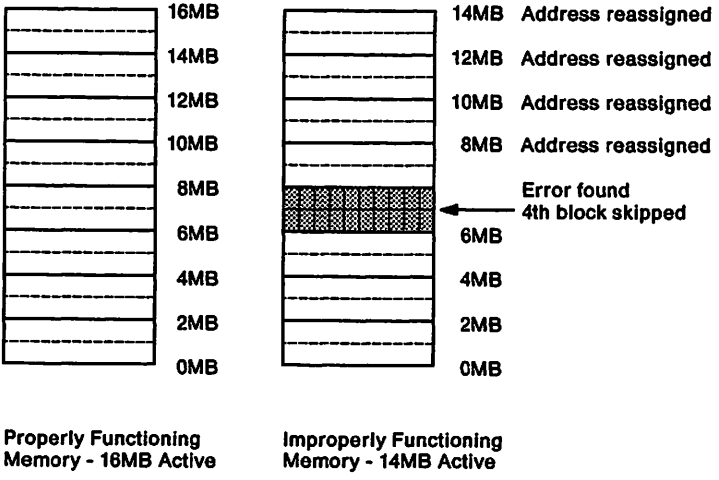


Figure 3-10. Memory Error Address Reassignment

Memory Subsystem Control

These read/write registers define and control the ROM and RAM subsystems.

Memory Encoding Register 1 (Hex 00E0)

This register determines how much memory on the system board is enabled.

Bit	Function
7	–Card 4 EN2
6	–Card 4 EN1
5	–Card 3 EN2
4	–Card 3 EN1
3	–Card 2 EN2
2	–Card 2 EN1
1	–Card 1 EN2
0	–Card 1 EN1

Figure 3-11. Memory Encoding Register 1 (Hex 00E0)

Bits 7, 6 These bits define system board memory in connector 4. When they are set to 0, bit 6 enables the first 2MB block and bit 7 enables the second 2MB block.

Bits 5, 4 These bits define system board memory in connector 3. When they are set to 0, bit 4 enables the first 2MB block and bit 5 enables the second 2MB block.

Bit 3, 2 These bits define system board memory in connector 2. When they are set to 0, bit 2 enables the first 2MB block and bit 3 enables the second 2MB block.

Bit 1, 0 These bits define system board memory in connector 1. When they are set to 0, bit 0 enables the first 2MB block and bit 1 enables the second 2MB block.

Memory Encoding Register 2 (Hex 00E1)

This register determines how much memory on the system board is enabled.

Bit	Function
7	SPA23
6	SPA22
5	SPA21
4	SPA20
3	–ENSPLIT
2	Reserved
1	ROMEN
0	–ENPLRPCH

Figure 3-12. Memory Encoding Register 2 (Hex 00E1)

Bits 7 - 4 These bits define the starting address of the split-memory block. When split memory is enabled, these bits determine its starting address. The starting location can be any size from 1MB to 15MB.

Bits 3 This bit determines whether the split-memory block is assigned addresses or is disabled. The top 128KB of the first 1MB is always mapped into the ROM address space and the code in ROM is copied into this space.

When this bit is set to 0, the split-memory block is enabled (the split-memory block size is always 256KB). The address is determined with bits 7 - 4.
When this bit is set to 1, the split-memory block is disabled.

Note: If the total system memory is equal to or greater than 16MB, the split-memory block cannot be used.

Bit 2 This bit is reserved and must be 0.

Bit 1 This bit determines how addresses hex 000E0000 to 000FFFFF are assigned.

When this bit is set to 1, ROM is enabled and the read-access addresses are assigned to ROM; the write-access addresses are assigned to RAM.
When this bit is set to 0, ROM is disabled and read addresses are assigned to RAM; the write addresses are disabled while ROM is disabled.

Memory Encoding Register 4 (Hex 00E3)

This register determines cache support function.

Bit	Function
7	SIMM TYPE 3 (+2MB SIMM/-4MB SIMM) SLOT 4
6	SIMM TYPE 2 (+2MB SIMM/-4MB SIMM) SLOT 3
5	SIMM TYPE 1 (+2MB SIMM/-4MB SIMM) SLOT 2
4	SIMM TYPE 0 (+2MB SIMM/-4MB SIMM) SLOT 1
3	—Cache 4K Enable
2	—Cache 2nd 8MB A
1	—Cache Flush
0	—Enable Cache

Figure 3-14. Memory Encoding Register 4 (Hex 00E3)

Bits 7 - 4 These bits determine whether the installed single in-line memory module (SIMM) is 4MB or 2MB. When this bit is set to 1, this socket is controlled as a 2MB SIMM. When this bit is set to 0, this bit is controlled as a 4MB SIMM.

Bit 3 This bit controls processor access to the first 4KB of segment E0000.

When this bit is set to 1, 4KB of memory from 000E0000 to 000E0FFF is mapped to non-cache memory.

Bits 2 This bit and bit 3 of the Memory Encoding Register 3 (hex 00E2) determine whether the second 8MB of memory is cached or not. See the description for Bit 3 of the "Memory Encoding Register 3 (Hex 00E2)" on page 3-19.

Note: Before disabling the caching of the second 8MB, disable and flush the cache.

Bit 1 See the description of bit 0.

Bit 0 This bit and bit 1 controls the state of the cache : either disabled and clear, or enabled. These bits must always be opposite polarities, and they must be modified in the same I/O instruction. When bit 1 is set to 0 and bit 0 is set to 1, the cache is disabled and flushed of data; when bit 1 is set to 1 and bit 0 is set to 0, the cache is enabled.

Note: The cache must be disabled and flushed before enabling ROM or disabling the caching of the second 8MB.

System Memory Maps

Memory is mapped by the Memory Encoding registers. The mapping results in 640KB of system board RAM starting at address hex 00000000. A 256-byte and 1KB portion of this RAM is reserved as BIOS data areas. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for more information.

In the following tables, the variable X represents the number of 2MB blocks of system board memory starting at or above the hex 00100000 boundary. The variable Y represents the number of 2MB blocks of memory installed in the channel starting at or above the hex 00100000 boundary (Y = 0 to 15).

–ENSPLIT	DIS4K	ROMEN	Map Number
1	0	1	1
0	0	1	2
1	1	1	3
0	1	1	4
1	0	0	5
0	0	0	6
1	1	0	7
0	1	0	8

Figure 3-15. System Memory Map

System Memory Map 1

The following table shows the memory mapping when:

—ENSPLIT = 1
DIS4K = 0
ROMEN = 1

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to 001FFFFF	1MB System Board RAM
00200000 to (00200000 + XMB)	XMB System Board RAM
(00200000 + XMB) to (00200000 + XMB + YMB)	YMB Channel RAM
(00200000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-16. System Memory Map 1

System Memory Map 2

The following figure shows the memory mapping when:

–ENSPLIT = 0
DIS4K = 0
ROMEN = 1

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to 001FFFFF	1MB System Board RAM
00200000 to (00200000 + YMB)	XMB System Board RAM
(00200000 + XMB) to (00200000 + XMB + YMB)	YMB Channel RAM
(00200000 + XMB + YMB) to (00200000 + XMB + YMB + 256KB – 1)	256KB System Board RAM
(00200000 + XMB + YMB + 256KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (same as 000E0000 to 000FFFFF)

Figure 3-17. System Memory Map 2

System Memory Map 3

The following figure shows the memory mapping when:

−ENSPLIT = 1
DIS4K = 1
ROMEN = 1

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000EFFFF	4KB Non System Video ROM
00E10000 to 000FFFFF	124KB System Board ROM
00100000 to 001FFFFF	1MB System Board RAM
00200000 to (00200000 + XMB)	XMB System Board RAM
(00200000 + XMB) to (00200000 + XMB + YMB)	YMB Channel RAM
(00200000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-18. System Memory Map 3

System Memory Map 4

The following figure shows the memory mapping when:

−ENSPLIT = 0
DIS4K = 1
ROMEN = 1

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000E0FFF	4KB Non System Video ROM
000E1000 to 000FFFFF	124KB System Board ROM
00100000 to 001FFFFF	1MB System Board RAM
00200000 to (00200000 + XMB)	XMB System Board RAM
(00200000 + XMB) to (00200000 + XMB + YMB)	YMB Channel RAM
(00200000 + XMB + YMB) to (00200000 + XMB + YMB + 256KB − 1)	256KB System Board RAM
(00200000 + XMB + YMB + 256KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (same as 000E0000 to 000FFFFF)

Figure 3-19. System Memory Map 4

System Memory Map 5

The following figure shows the memory mapping when:

−ENSPLIT = 1
DIS4K = 0
ROMEN = 0

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM space
00100000 to 001FFFFF	1MB System Board RAM
00200000 to (00200000 + XMB)	XMB System Board RAM
(00200000 + XMB) to (00200000 + XMB + YMB)	YMB Channel RAM
(00200000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (same as 000E0000 to 000FFFFF)

Figure 3-20. System Memory Map 5

System Memory Map 6

The following figure shows the memory mapping when:

−ENSPLIT = 0
DIS4K = 0
ROMEN = 0

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM space
00100000 to 001FFFFF	1MB System Board RAM
00200000 to (00200000 + XMB)	XMB System Board RAM
(00200000 + XMB) to (00200000 + XMB + YMB)	YMB Channel RAM
(00200000 + XMB + YMB) to (00200000 + XMB + YMB + 256KB − 1)	256KB System Board ROM
(00200000 + XMB + YMB + 256KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (same as 000E0000 to 000FFFFF)

Figure 3-21. System Memory Map 6

System Memory Map 7

The following figure shows the memory mapping when:

–ENSPLIT = 1
DIS4K = 1
ROMEN = 0

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000E0FFF	4KB Non System Video ROM
000E1000 to 000FFFFF	124KB System Board ROM mapped to RAM space
00100000 to 001FFFFF	1MB System Board RAM
00200000 to (00200000 + XMB)	XMB System Board RAM
(00200000 + XMB) to (00200000 + XMB + YMB)	YMB Channel RAM
(00200000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (same as 000E0000 to 000FFFFF)

Figure 3-22. System Memory Map 7

System Memory Map 8

The following figure shows the memory mapping when:

−ENSPLIT = 0
DIS4K = 1
ROMEN = 0

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000E0FFF	4KB Non System Video ROM
000E1000 to 000FFFFF :124KB System Board ROM mapped to RAM space	
00100000 to 001FFFFF	1MB System Board RAM
00200000 to (00200000 + XMB)	XMB Channel Board RAM
(00200000 + XMB) to (00200000 + XMB + YMB)	YMB Channel RAM
(00200000 + XMB + YMB) to (00200000 + XMB + YMB + 256KB − 1)	256KB System Board RAM
(00200000 + XMB + YMB + 256KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (same as 000E0000 to 000FFFFF)

Figure 3-23. System Memory Map 8

System Board Memory Connectors

The system board has four 72-pin memory connectors that support the 2MB and 4MB memory cards. The four connectors are numbered 1-2-3-4 from the top of the system. Memory-refresh requests typically occur once every 15 microseconds.

The following figure shows the pin assignments for the 1- by 72-pin memory connectors.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Ground	37	I/O	Parity Data 1
2	I/O	Data 0	38	I/O	Parity Data 3
3	I/O	Data 16	39	N/A	Ground
4	I/O	Data 1	40	O	Column Address Strobe 0
5	I/O	Data 17	41	O	Column Address Strobe 2
6	I/O	Data 2	42	O	Column Address Strobe 3
7	I/O	Data 18	43	O	Column Address Strobe 1
8	I/O	Data 3	44	O	Row Address Strobe 0
9	I/O	Data 19	45	O	Row Address Strobe 1
10	O	+5 Vdc	46	O	Block Select 1
11	O	–Column Address Strobe P	47	O	Write Enable
12	O	Address 0	48	N/A	Reserved
13	O	Address 1	49	I/O	Data 8
14	O	Address 2	50	I/O	Data 24
15	O	Address 3	51	I/O	Data 9
16	O	Address 4	52	I/O	Data 25
17	O	Address 5	53	I/O	Data 10
18	O	Address 6	54	I/O	Data 26
19	N/A	Reserved	55	I/O	Data 11
20	I/O	Data 4	56	I/O	Data 27
21	I/O	Data 20	57	I/O	Data 12
22	I/O	Data 5	58	I/O	Data 28
23	I/O	Data 21	59	O	+5 Vdc
24	I/O	Data 6	60	I/O	Data 29
25	I/O	Data 22	61	I/O	Data 13
26	I/O	Data 7	62	I/O	Data 30
27	I/O	Data 23	63	I/O	Data 14
28	O	Address 7	64	I/O	Data 31

Figure 3-24 (Part 1 of 2). System Board Memory Connector

Pin	I/O	Signal	Pin	I/O	Signal
29	O	Block Select 0	65	I/O	Data 15
30	O	+5 Vdc	66	O	Block Select 2
31	O	Address 8	67	I	Presence Detect 0
32	N/A	Reserved	68	I	Presence Detect 1
33	O	Row Address Strobe 3	69	I	Presence Detect 2
34	O	Row Address Strobe 2	70	I	Presence Detect 3
35	I/O	Parity Data 2	71	O	Block Select 3
36	I/O	Parity Data 0	72	N/A	Ground

Figure 3-24 (Part 2 of 2). System Board Memory Connector

The 'presence detect' signals are used by the system to determine memory card size and memory speed. The pins are either connected to ground (G) or not connected (N). The following table shows those combinations supported by Model P75.

Card Type	Presence Detect Signals			
	0	1	2	3
2MB Memory at 70 ns	G	G	N	N
4MB Memory at 70 ns	G	G	N	G

Figure 3-25. Presence Detect Encoding

Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM

The real-time clock/complementary metal-oxide semiconductor RAM (RT/CMOS) chip contains the real-time clock and 64 bytes of CMOS RAM. The internal clock circuitry uses 14 bytes of this memory, and the rest is allocated to configuration and system status information.

In addition to the 64 bytes of CMOS RAM, a 2KB CMOS RAM extension is provided for configuration and other system information.

A backup 6-Vdc lithium battery maintains voltage to the RT/CMOS RAM and 2KB CMOS RAM extension when the power supply is not in operation.

The system cover can be locked to prevent battery removal and loss of password and configuration information.

The following figure shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000 - 00D	Real-Time Clock Bytes
00E	Diagnostic Status Byte
00F	Shutdown Status Byte
010	Diskette Drive Type Byte
011	First Fixed Disk Drive Type Byte
012	Reserved
013	Reserved
014	Equipment Byte
015 - 016	Low and High Base Memory Bytes
017 - 018	Low and High Expansion Memory Bytes
019 - 031	Reserved
032 - 033	Configuration CRC Bytes
034 - 036	Reserved
037	Date Century Byte
038 - 03F	Reserved

Figure 3-26. RT/CMOS RAM Address Map

RT/CMOS Address Register and NMI Mask (Hex 0070)

This register is used in conjunction with the port at hex 0071 to read and write the RT/CMOS RAM bytes.

Bit	Function
7	NMI Mask
6	Reserved
5 - 0	RT/CMOS RAM Address

Figure 3-27. RT/CMOS Address Register and NMI Mask (Hex 0070)

Warning: The operation following a write to hex 0070 should access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Bit 7 When this bit is set to 1, the NMI is masked off (the NMI is disabled). This bit is set to 1 by a power-on reset. This is a write-only bit.

Bit 6 Reserved.

Bits 5 - 0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This port is used in conjunction with the address register at hex 0070 to read and write the RT/CMOS RAM bytes.

Bit	Function
7 - 0	RT/CMOS Data

Figure 3-28. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts should be masked to prevent other interrupt routines from changing the CMOS Address register before data is read or written. After I/O operations, the RT/CMOS and NMI Mask register (hex 0070) should be left pointing to Status Register D (hex 00D).

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

The following steps are required to perform I/O operations to the RT/CMOS RAM addresses:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Write the data to address hex 0071.

Reading RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Read the data from address hex 0071.

Real-Time Clock Bytes (Hex 000-00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following figure.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second Alarm	1
002	Minutes	2
003	Minute Alarm	3
004	Hours	4
005	Hour Alarm	5
006	Day of Week	6
007	Date of Month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-29. Real-Time Clock Bytes

Note: The Setup program initializes status registers A, B, C, and D when the time and date are set. Interrupt hex 1A is the BIOS interface to read and set the time and date and it initializes the register the same way as the Setup program.

Status Register A (Hex 00A)

Bit	Function
7	Update in Progress
6 - 4	22-Stage Divider
3 - 0	Rate Selection Bits

Figure 3-30. Status Register A

Bit 7 When set to 1, this bit indicates the time-update cycle is in progress. When set to 0, it indicates the current date and time can be read.

Bits 6 - 4 These three divider-selection bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768 kHz time base. This is the only value supported by the system for proper time-keeping.

Bits 3 - 0 These bits allow the selection of a divider output frequency. The system initializes the rate selection bits to a binary 0110, which selects a 1.024 kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Periodic Interrupt Enable
5	Alarm Interrupt Enable
4	Update-Ended Interrupt Enabled
3	Square Wave Enabled
2	Date Mode
1	24-Hour Mode
0	Daylight Saving Enabled

Figure 3-31. Status Register B

Bit 7 When set to 0, this bit updates the cycle, normally by advancing the counts at a rate of one per second. When set to 1, this bit immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This bit is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

Bit 5 When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit indicates if the time-and-date calendar updates use binary or binary-coded-decimal (BCD) formats. When set to 1, this bit indicates a binary format. The system initializes this bit to 0.

Bit 1 This bit establishes if the hours byte is in the 24-hour or 12-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When set to 1, this bit enables the daylight saving time mode. When set to 0, it disables the mode, and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt Request Flag
6	Periodic Interrupt Flag
5	Alarm Interrupt Flag
4	Update-Ended Interrupt Flag
3 - 0	Reserved

Figure 3-32. Status Register C

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 This bit is used in conjunction with bits 6, 5, and 4. When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When set to 1, this bit indicates that a periodic interrupt occurred.

Bit 5 When set to 1, this bit indicates that an alarm interrupt occurred.

Bit 4 When set to 1, this bit indicates that an update-ended interrupt occurred.

Bits 3 - 0 Reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6 - 0	Reserved

Figure 3-33. Status Register D

Bit 7 This read-only bit monitors the power-sense pin. A low state of this pin indicates a loss of power to the real-time clock (dead battery). When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power.

Bits 6 - 0 Reserved.

CMOS RAM Configuration

The following shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-Time Clock Chip Power
6	Configuration Record and Checksum Status
5	Incorrect Configuration
4	Memory Size Miscompare
3	Fixed Disk Controller/Drive C Initialization Status
2	Time Status Indicator
1	Adapter Configuration Miscompare
0	Adapter ID Time-Out

Figure 3-34. Diagnostic Status Byte

Bit 7 When set to 1, this bit indicates the real-time clock chip lost power.

Bit 6 When this bit is set to 1, the checksum is incorrect.

Bit 5 This is a check, at power-on time, of the Equipment byte. When set to 1, the configuration information is incorrect. Power-on checks require that at least one diskette drive be installed (bit 0 of the Equipment byte, hex 014, is set to 1).

Bit 4 When set to 1, this bit indicates the power-on check determined that the memory size is not the same as in the configuration record.

Bit 3 When set to 1, this bit indicates that the controller or drive C failed initialization, which prevents the system from attempting a power-on reset.

Bit 2 When set to 0, this bit indicates the time is valid. When set to 1, this bit indicates the time is invalid.

Bit 1 This bit indicates if the installed adapters match the configuration information. When this bit is set to 1, the adapters do not match the configuration information.

Bit 0 When set to 1, this bit indicates a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7 - 4	First Diskette Drive Type
3 - 0	Second Diskette Drive Type (External storage device)

Figure 3-35. Diskette Drive Type Byte

Bits 7 - 4 These bits indicate the first diskette drive type, as shown in the following figure.

Bits 7 6 5 4	Function
0 0 0 0	No drive present
0 0 0 1	Double-sided diskette drive (48 tracks per inch, 360KB)
0 0 1 0	High-capacity diskette drive (1.2MB)
0 0 1 1	High-capacity diskette drive (720KB)
0 1 0 0	High-density diskette drive (1.44MB)

Note: All combinations that are not shown are reserved.

Figure 3-36. Diskette Drive Type Byte (Bits 7 - 4)

Bits 3 - 0 These bits indicate the second diskette drive type, as shown in the following figure.

Bits 3 2 1 0	Function
0 0 0 0	No drive present
0 0 0 1	Double-sided diskette drive (48 tracks per inch, 360KB)
0 0 1 0	High-capacity diskette drive (1.2MB)
0 0 1 1	High-capacity diskette drive (720KB)
0 1 0 0	High-density diskette drive (1.44MB)

Note: All combinations that are not shown are reserved.

Figure 3-37. Diskette Drive Type Byte (Bits 3 - 0)

First Fixed Disk Drive Type Byte (Hex 011): This byte defines the type of the first fixed disk drive (drive C). Hex 00 indicates that a fixed disk drive is *not* installed.

Note: For more information about fixed disk drive types, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*.

Reserved Bytes (Hex 012 and 013): These bytes are reserved.

Equipment Byte (Hex 014): The equipment byte defines the basic equipment in the system for the power-on diagnostic tests.

Bit	Function
7, 6	Number of Diskette Drives
5, 4	Display Operating Mode
3, 2	Reserved
1	Math Coprocessor Presence
0	Diskette Drive Presence

Figure 3-38. Equipment Byte

Bits 7, 6 These bits indicate the number of diskette drives installed, as shown in the following figure.

Bits 7 6	Number of Diskette Drives
0 0	One Drive
0 1	Two Drives
1 0	Reserved
1 1	Reserved

Figure 3-39. Equipment Byte (Bits 7, 6)

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port, as shown in the following figure.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-Column Mode
1 0	80-Column Mode
1 1	Monochrome Mode

Figure 3-40. Equipment Byte (Bits 5, 4)

Bits 3, 2 Reserved.

Bit 1 When set to 1, this bit indicates that a math coprocessor is installed.

Bit 0 When set to 1, this bit indicates that a diskette drive is installed.

Low and High Base Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 is equal to 640KB. The low byte is hex 15; the high byte is hex 16.

Low and High Expansion Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The hexadecimal values in these bytes represent the number of 1KB blocks of expansion memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 17; the high byte is hex 18.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 33; the high byte is hex 32.

Reserved Bytes (Hex 034 through 036): These bytes are reserved.

Date Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 through 03F): These bytes are reserved.

SCSI Port

This section briefly describes the function of the Model P75 Small Computer System Interface (SCSI) port. The SCSI port, which is built into the system board, allows SCSI devices (fixed disk drive, optical disk, tape drive, and others) to be attached to the Model P75 Micro Channel bus through the SCSI I/O device interface. The SCSI port acts only as an initiator and may not be selected as a target by another initiator.

The Model P75 has a 160MB or 400MB fixed disk drive installed internally through the SCSI. For further information about SCSI, see *IBM PS/2 Micro Channel SCSI Adapter Technical Reference*, S68X-2397.

Connector Pin Assignment

The Model P75 has two SCSI interface connectors. One is a 50-pin signal connection and is used to connect an internal fixed disk drive (160MB or 400MB). The other is a 60-pin signal connector. This connector is located at the rear of the system unit so that external SCSI devices can be connected.

The pin assignment of those connectors are as follows.

Pin	Signal	Pin	Signal
1	Ground	2	−DB(0)
3	Ground	4	−DB(1)
5	Ground	6	−DB(2)
7	Ground	8	−DB(3)
9	Ground	10	−DB(4)
11	Ground	12	−DB(5)
13	Ground	14	−DB(6)
15	Ground	16	−DB(7)
17	Ground	18	−DB(P)
19	Ground	20	Ground
21	Ground	22	Ground
23	Ground	24	Ground
25	Not Used	26	+TERMPWR
27	Ground	28	Ground
29	Ground	30	Ground
31	Ground	32	−ATN
33	Ground	34	Ground
35	Ground	36	−BSY
37	Ground	38	−ACK
39	Ground	40	−RST
41	Ground	42	−MSG
43	Ground	44	−SEL
45	Ground	46	−C/D
47	Ground	48	−REQ
49	Ground	50	−I/O

Figure 3-41. 50-pin SCSI Signal Connector

Pin	Signal	Pin	Signal
1	Ground	2	−DB(0)
3	Ground	4	−DB(1)
5	Ground	6	−DB(2)
7	Ground	8	−DB(3)
9	Ground	10	−DB(4)
11	Ground	12	−DB(5)
13	Ground	14	−DB(6)
15	Ground	16	−DB(7)
17	Ground	18	−DB(P)
19	Ground	20	Ground
21	Ground	22	Ground
23	Ground	24	Ground
25	Not Used	26	+TERMPWR
27	Ground	28	Ground
29	Ground	30	Ground
31	Ground	32	−ATN
33	Ground	34	Ground
35	Ground	36	−BSY
37	Ground	38	−ACK
39	Ground	40	−RST
41	Ground	42	−MSG
43	Ground	44	−SEL
45	Ground	46	−C/D
47	Ground	48	−REQ
49	Ground	50	−I/O
51	Not Used	52	Not Used
53	Not Used	54	Not Used
55	Not Used	56	Not Used
57	Not Used	58	Not Used
59	Not Used	60	Not Used

Figure 3-42. 60-pin SCSI Signal Connector

Termination Resistors

The termination resistors for single ended devices are mounted on the system board.

Miscellaneous System Functions

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system Watchdog time-out has occurred. The NMI stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts and the IRET instruction restores the interrupt flag to the state it was in prior to the interrupt. A system reset causes a reset of the NMI.

Nonmaskable interrupt requests from system board parity and channel check are subject to mask control with the NMI mask bit in the RT/CMOS Address register. The Watchdog Timer and system channel time-out are not masked by this bit. (See "RT/CMOS Address Register and NMI Mask (Hex 0070)" on page 3-32). The power-on default of the NMI mask is 1 (NMI disabled). Prior to enabling the NMI after a power-on reset, the parity check and channel check state are initialized by the POST.

Warning: The operation following a write to hex 0070 should access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the read and write functions of this port are shown in the following figures.

Bit	Function
7	Reset Timer 0 Output Latch (IRQ0)
6 - 4	Reserved
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-43. System Control Port B (Write)

Bit	Function
7	Parity Check
6	Channel Check
5	Timer 2 Output
4	Toggles with Each Refresh Request
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-44. System Control Port B (Read)

Bit 7 Setting this bit to 1 resets IRQ0. Reading this bit as a 1 indicates a parity check has occurred.

Bit 6 Reading this bit as a 1 indicates a channel check has occurred.

Bit 5 This bit indicates the condition of the 'timer/counter 2 output' signal.

Bit 4 This bit toggles for each refresh request.

Bit 3 Setting this bit to 0 enables channel check. This bit is set to 1 during a power-on reset. Setting this bit to 1 disables channel check and clears the channel check latch.

Bit 2 Setting this bit to 0 enables parity check. This bit is set to 1 during a power-on reset. To clear a parity error, set this bit to 1 and then to 0.

Bit 1 Setting this bit to 1 enables speaker data.

Bit 0 Setting this bit to 1 enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7, 6	Fixed-Disk Activity Light
5	Reserved
4	Watchdog Timer Status
3	Security Lock Latch
2	Reserved
1	Alternate Gate A20
0	Alternate Hot Reset

Figure 3-45. System Control Port A

Bits 7, 6 These bits control the fixed-disk activity light. Setting either bit to 1 turns the fixed-disk activity light on. Setting both bits to 0 turns the light off. The power-on reset condition of each bit is 0.

Bit 5 Reserved.

Bit 4 This read-only bit indicates the Watchdog Timer status. When this bit is set to 1, a Watchdog time-out has occurred. For more information about the Watchdog Timer, refer to the *Hardware Interface Technical Reference*.

Bit 3 This bit provides the security lock for the secured area of RT/CMOS. Setting this bit to 1 electrically locks the 8-byte, power-on password. Once this bit is set by POST, it can only be cleared by turning the system off.

Bit 2 Reserved.

Bit 1 This bit is ORed with bit 1 in the keyboard output port to enable the 'address 20' signal (A20). When both bits are set to 0, A20 is disabled and set to 0. This bit is set to 0 during a system reset.

Bit 0 This bit provides an alternate method of resetting the system microprocessor. This alternate method supports operating systems requiring faster operation than was provided on the IBM Personal Computer AT*. Resetting the system microprocessor switches the microprocessor from the protected mode to the real address mode. The alternate reset takes 13.4 microseconds.

This bit is set to 0 either by a system reset or a Write operation. When a Write operation changes this bit from 0 to 1, the alternate reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is 0, POST assumes the system was just powered on. If the bit is 1, POST assumes a switch from the protected mode to the real mode has taken place.

---

* IBM Personal Computer AT is a trademark of the International Business Machines Corporation.

Power-On Password

RT/CMOS RAM has 8 bytes reserved for the power-on password and its check character. The 8 bytes are initialized to hex 00. The microprocessor can only access these bytes during power-on self-test (POST). After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by a program. A power-on password can be from 1 to 7 characters.

During power-on password installation, the password (1 to 7 keyboard scan codes), is stored in the security space.

Power-on password installation is a function of a program contained on the Reference diskette. Once the power-on password utility has been installed, the password can be changed only during the POST. When the new power-on password is installed, changed, or removed, the password is not visible on the display.

The system unit cover can be physically locked to prevent unauthorized access to the battery. This helps prevent unauthorized battery removal and loss of power-on password and configuration information.

For information about the keyboard password, see the "Keyboard and Auxiliary Device Controller" section in the *IBM Personal System/2 Hardware Interface Technical Reference.*

Hardware Compatibility

The Model P75 maintains many of the interfaces used by the IBM Personal Computer AT. In most cases command and status organization of these interfaces is maintained.

The functional interfaces for the Model P75 are compatible with the following interfaces:

- The Intel** 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller-address/transfer counters, page registers and status fields only. The Command and Request registers are not supported. The rotate and mask functions are not supported. The Mode register is partially supported.
- The NS16450 serial port.
- The Intel 8088, 8086, 80286, and 80386SX** microprocessors.
- The Intel 8272 or equivalent diskette-drive controller.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The keyboard port at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.

** Intel is a trademark of the Intel Corporation.

** 80386SX is a trademark of the Intel Corporation.

** Motorola is a trademark of Motorola, Inc.

- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.
- Generally compatible with the Intel 8087, 80287, and 80387SX** math coprocessors.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.
- 9-PEL wide fonts are not supported on the plasma display because the display is limited to 640 total PELs.
- Border screen is not supported on the plasma display.

** 80387SX is a trademark of the Intel Corporation.

POST Error Codes

POST returns a message in the form of a number to indicate the type of test that failed. The following figure gives the failure indicated with the associated error code. For information on unlisted error codes, contact Developer Assistance at 1-800-IBM-7763 in the U.S. (this number is for developers who are registered with IBM).

Error Code	Description
101	Interrupt failure
102	Timer failure
103	Timer interrupt failure
104	Protected mode failure
105	Keyboard controller command failure
107	Hot NMI test
108	Timer bus test
109	Memory select
110	System board parity
111	I/O parity
112	Watchdog timeout
113	DMA arbitration timeout
114	External ROM checksum
160	System board ID not recognized
161	Bad battery or configuration
162	CMOS checksum or adapter ID mismatch
163	Date and time not set
164	Memory size mismatch
165	Adapter ID mismatch
166	Card busy
167	System clock not updating
201	Memory miscompare or parity
202	Memory address line error (address line: 00 - 15)
203	Memory address line error (address line: 16 - 31)
211	No memory module detected on the system board
215/216	Memory Base 512K on SIMM 1 or SIMM 2 failed
221	ROM to RAM copy
225	Wrong speed memory on system board
301	Keyboard interface
303	Keyboard or system board
304	Keyboard clock failure
305	Keyboard +5 V error
601	Diskette drive or controller
602	Diskette boot record
1101	Async error
8601	Mouse timeout
8602	Mouse interface
8603	Mouse interrupt
12901	Failed-processor portion of processor board test
12902	Failed-cache portion of processor board test
12903	NPX error
14901	Plasma-display adapter failure

Figure 3-46. POST Error Code Table

Section 4. Video Subsystem

Description 4-3
Plasma Display 4-3
Plasma Display Card 4-4
Overview 4-4
Video Mode 4-6
Distinctive-mapping 4-7
Half-toning (Dithering) 4-8
Connectors and Signals 4-8
System Interface Connector 4-8
Plasma display connector 4-12
External CRT Display Connector 4-12

Notes:

Description

The Model P75 has a monochrome plasma display, which is controlled by the plasma display card. Besides the plasma-display control section, the plasma display card includes an XGA Video Subsystem section. This permits an external PS/2 display to be attached to the Model P75 without an additional adapter.

With the XGA function, you can connect and use a high-resolution CRT display.

Note: When an external PS/2 display is attached, data can be displayed on both the plasma and the external displays at the same time as long as you change the configuration with the Reference Diskette.

Plasma Display

The plasma display is a flat panel monochrome display. Each PEL can display 16 shades of gray.

Its specification follows.

Screen size: 211.2 x 158.4 mm (8.31 x 6.24 inches)
Resolution: 640 x 480 PEL

Plasma Display Card

Overview

The plasma display card is plugged into the 32-bit channel connecter on the system board. This 32-bit channel connecter contains all signals on the 32-bit micro channel with Auxiliary Video Extension plus some additional signals necessary for the plasma display card.

The plasma display controller (PDC) emulates the PS/2 8503 monochrome display. Half-toning technology is used to implement mode hex 13, and distinctive-mapping is used on the remaining modes.

The XGA video subsystem provides resolutions up to 1024 rows by 768 lines with 256 colors. For more information about the XGA, refer to the "Video Subsystem" section of the *IBM Personal System/2 Hardware Interface Technical Reference.*

The following is the block diagram of the plasma display card.

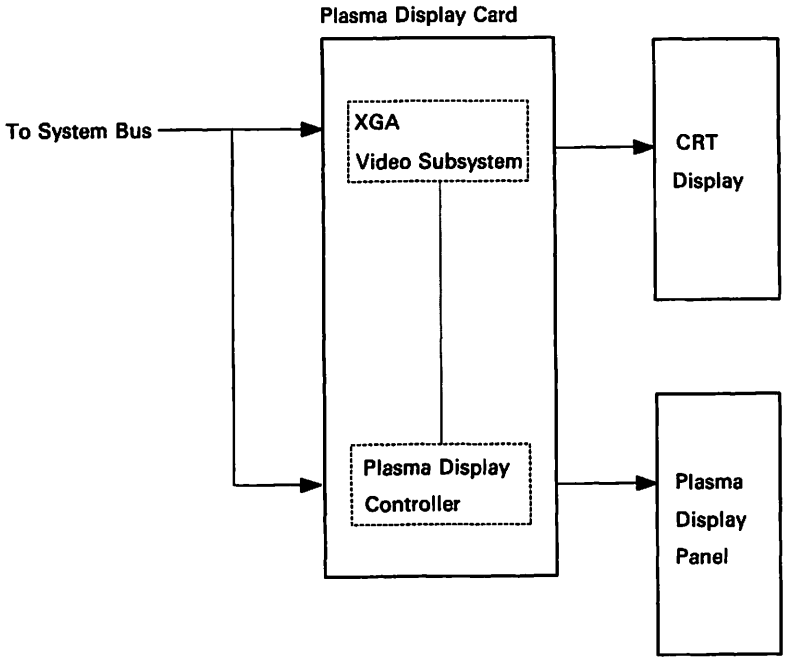


Figure 4-1. Block Diagram of the Plasma Display Card

Video Mode

Figure 4-2 shows hardware-specific video mode supported by the plasma display card. A/N modes (0+, 1+, 2+, 3+, 7, 7+) with 9-dot width font are supported only for the external PS/2 display. A/N modes (0#, 1#, 2#, 3#, 7*, 7#) are used only for the plasma display.

Note: The border screen is not supported for the plasma display.

Mode	Type	Colors to Program	Alpha Format	Font Box	Resolution to Program	Resolution on PDP	CRT Connected	PDP Enabled
0	A/N	B&W	40×25	8×8	320×200	640×400	S	S
0*	A/N	16/64	40×25	8×14	320×350	640×350	S	S
0+	A/N	16/256K	40×25	9×16	360×400	-	S	NS
0#	A/N	16/256K	40×25	8×16	320×400	640×400		S
1	A/N	16	40×25	8×8	320×200	640×400	S	S
1*	A/N	16/64	40×25	8×14	320×350	640×350	S	S
1+	A/N	16/256K	40×25	9×16	360×400	-	S	NS
1#	A/N	16/256K	40×25	8×16	320×400	640×400		S
2	A/N	B&W	80×25	8×8	640×200	640×400	S	S
2*	A/N	16/64	80×25	8×14	640×350	640×350	S	S
2+	A/N	16/256K	80×25	9×16	720×400	-	S	NS
2#	A/N	16/256K	80×25	8×16	640×400	640×400		S
3	A/N	16	80×25	8×8	640×200	640×400	S	S
3*	A/N	16/64	80×25	8×14	640×350	640×350	S	S
3+	A/N	16/256K	80×25	9×16	720×400	-	S	NS
3#	A/N	16/256K	80×25	8×16	640×400	640×400		S
4	APA	4/256K		8×16	320×200	640×400	S	S
5	APA	4/256K		8×16	320×200	640×400	S	S
6	APA	2/256K		8×16	640×200	640×400	S	S
7	A/N	B&W	80×25	9×14	720×350	-	S	NS
7*	A/N	B&W	80×25	8×14	640×350	640×350		S
7+	A/N	B&W	80×25	9×16	720×400	-	S	NS
7#	A/N	B&W	80×25	8×16	640×400	640×400		S
D	APA	16/256K		8×8	320×200	640×400	S	S
E	APA	16/256K		8×8	640×200	640×400	S	S
F	APA	2/256K		8×14	640×350	640×350	S	S
10	APA	16/256K		8×14	640×350	640×350	S	S
11	APA	2/256K		8×16	640×480	640×480	S	S
12	APA	16/256K		8×16	640×480	640×480	S	S
13	APA	256/256K		8×8	320×200	640×400(1)	S(2)	S(3)

Figure 4-2 (Part 1 of 2). Video Modes

Mode	Type	Colors to Program	Alpha Format	Font Box	Resolution to Program	Resolution on PDP	CRT Connected	PDP Enabled
XGA	A/N	16/256K	132x25	8x8	1056x200	-	S	NS
(132	A/N	16/256K	132x25	8x14	1056x350	-	S	NS
Col.)	A/N	16/256K	132x25	8x16	1056x400	-	S	NS
XGA	APA	256/256K			640x480	640x480	S(2)	NS(4)
XGA	APA	16/256K			1024x768	-	S(5)	NS(6)
XGA	APA	256/256K			1024x768	-	S(5)	NS(6)

Note:

S	Indicates supported screen mode.
NS	Indicates non-supported screen mode.
#	Indicates new screen mode for the flat panel, symbols are temporary.
1	4 dots are used per 1 pixel.
2	When monochrome display attached, only 64 gray scales can be displayed.
3	Same as monochrome display. Only 64 gray scales can be displayed on PDP using Dither pattern.
4	If this video mode is called, the PDP displays only 16 gray scales, and the image may not be legible.
5	To use this mode, an 8514 or equivalent resolution monitor is needed.
6	PDPC automatically disables the PDP.

Figure 4-2 (Part 2 of 2). Video Modes

Distinctive-mapping

The plasma display controller has unique distinctive-mapping hardware for use in video modes hex 0 to hex 12. This is a transparent technique to ensure that the plasma display correctly shows the shades requested from an application.

This mapping hardware takes the output of the color registers and identifies which 16 shades are currently in use by the application. It then assigns a corresponding brightness level for the plasma display and also makes sure each application color has 1 of 16 distinct plasma display brightness levels. Colors that are very similar on a CRT are adjusted to a unique brightness levels on the plasma display. The relative brightness positions are maintained during this process.

The result is a better image on the plasma display even when applications adjust the palette and color registers. The distinctive-mapping operation occurs during the vertical retrace interval and is automatic and transparent to the application.

If applications adjust the color registers, BIOS is recommended. The IBM PS/2 Monochrome Display 8503 and the plasma display use the DAC color registers for only the green output. BIOS will make the

appropriate weighted sum from the red, green, and blue register values for use with any IBM PS/2 display. For more information, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Half-toning (Dithering)

The plasma display can display 16 gray scales in each PEL, but the PS/2 8503 monochrome display identifies up to 64 gray scales in mode hex 13. The plasma display emulates 64 gray patterns with half-toning technology.

In the half-toning method, contiguous 2 x 2 PELs are treated as one logical dot because the resolution in mode hex 13 is 320 x 200 dots while the physical resolution is 640 x 400 PELs. The four PELs of 16 gray scales result in 64 gray patterns.

Connectors and Signals

The plasma display card has three connectors.

- System interface connector to the system board
- Plasma Display connector to the plasma display
- Display connector to the external PS/2 display.

System Interface Connector

The following figure shows the signal assignment of the system interface connector. The connector contains the same signal set as the 32-bit micro channel connector except two pins; the pin A11 is assigned with the signal '-VIDEO SETUP' and the pin B45 is assigned with the signal '-KEYSTROKE' for the plasma display.

Pin	Signal	Pin	Signal
B01	AUDIO GND	A01	–CD SETUP
B02	AUDIO	A02	MADE 24
B03	GND	A03	GND
B04	14.3 MHz OSC	A04	A 11
B05	GND	A05	A 10
B06	A 23	A06	A 09
B07	A 22	A07	+5Vdc
B08	A 21	A08	A 08
B09	GND	A09	A 07
B10	A 20	A10	A 06
B11	A 19	A11	–Video Setup
B12	A 18	A12	A 05
B13	GND	A13	A 04
B14	A 17	A14	A 03
B15	A 16	A15	+5Vdc
B16	A 15	A16	A 02
B17	GND	A17	A 01
B18	A 14	A18	A 00
B19	A 13	A19	+12Vdc
B20	A 12	A20	–ADL
B21	GND	A21	–PREEMPT
B22	–IRQ 09	A22	–BURST
B23	–IRQ 03	A23	–12Vdc
B24	–IRQ 04	A24	ARB 00
B25	GND	A25	ARB 01
B26	–IRQ 05	A26	ARB 02
B27	–IRQ 06	A27	–12Vdc
B28	–IRQ 07	A28	ARB 03
B29	GND	A29	ARB/–GNT
B30	Reserved	A30	–TC
B31	Reserved	A31	+5Vdc
B32	–CHCK	A32	–S0
B33	GND	A33	–S1
B34	–CMD	A34	M/–IO
B35	CHRDYRTN	A35	+12Vdc
B36	–CD SFDBK	A36	CD CHRDY
B37	GND	A37	D 00
B38	D 01	A38	D 02
B39	D 03	A39	+5Vdc
B40	D 04	A40	D 05
B41	GND	A41	D 06
B42	CHRESET	A42	D 07
B43	Reserved	A43	GND
B44	Reserved	A44	–DS 16 RTN
B45	–KEYSTROKE	A45	–REFRESH
B46	KEY	A46	KEY

Figure 4-3 (Part 1 of 2). System Interface Connector

Pin	Signal	Pin	Signal
B47	KEY	A47	KEY
B48	D 08	A48	+5Vdc
B49	D 09	A49	D 10
B50	GND	A50	D 11
B51	D 12	A51	D 13
B52	D 14	A52	+12Vdc
B53	D 15	A53	Reserved
B54	GND	A54	–SBHE
B55	–IRQ 10	A55	–CD DS 16
B56	–IRQ 11	A56	+5Vdc
B57	–IRQ 12	A57	–IRQ 14
B58	GND	A58	–IRQ 15

Figure 4-3 (Part 2 of 2). System Interface Connector

Pin	Signal	Pin	Signal
B59	Reserved	A59	Reserved
B60	Reserved	A60	Reserved
B61	Reserved	A61	GND
B62	Reserved	A62	Reserved
B63	GND	A63	Reserved
B64	D 16	A64	Reserved
B65	D 17	A65	+12Vdc
B66	D 18	A66	D 19
B67	GND	A67	D 20
B68	D 22	A68	D 21
B69	D 23	A69	+5Vdc
B70	Reserved	A70	D 24
B71	GND	A71	D 25
B72	D 27	A72	D 26
B73	D 28	A73	+5Vdc
B74	D 29	A74	D 30
B75	GND	A75	D 31
B76	–BE 0	A76	Reserved
B77	–BE 1	A77	+12Vdc
B78	–BE 2	A78	–BE 3
B79	GND	A79	–DS 32 RTN
B80	TR 32	A80	–CD DS 32
B81	A24	A81	+5Vdc
B82	A25	A82	A26
B83	GND	A83	A27
B84	A29	A84	A28
B85	A30	A85	+5Vdc
B86	A31	A86	Reserved
B87	GND	A87	Reserved
B88	Reserved	A88	Reserved
B89	Reserved	A89	GND

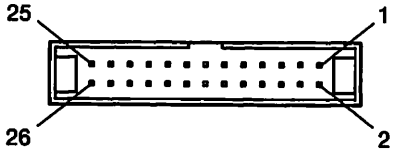
Figure 4-4. 32-bit Extension

Pin	Signal	Pin	Signal
B V10	ESYNC	A V10	VSYNC
B V9	GND	A V9	HSYNC
B V8	P5	A V8	BLANK
B V7	P4	A V7	GND
B V6	P3	A V6	P6
B V5	GND	A V5	EDCLK
B V4	P2	A V4	DCLK
B V3	P1	A V3	GND
B V2	P0	A V2	P7
B V1	GND	A V1	EVIDEO

Figure 4-5. Auxiliary Video Extension

Plasma display connector

The hardware interface to the plasma display uses a 26-pin connector. The following figure shows the signal assignment.



Pin	I/O	Signal	Pin	I/O	Signal
1	O	–Vsync	2	N/A	Ground
3	O	–Hsync	4	N/A	Ground
5	O	–Data 0	6	N/A	Ground
7	O	–Data 1	8	N/A	Ground
9	O	–Data 2	10	N/A	Ground
11	O	–Data 3	12	N/A	Ground
13	O	–Display Timing	14	N/A	Ground
15	O	–Dot Clock	16	N/A	Ground
17	O	+Disable	18	N/A	Ground
19	O	–Blanking	20	N/A	Ground
21	O	–Gamma Compensation	22	O	–Background Intensity
23	N/A	Ground	24	N/A	Ground
25	N/A	Ground	26	N/A	Ground

Figure 4-6. Plasma Display Connector

External CRT Display Connector

The hardware interface to the external display uses the standard PS/2 display connector. For more information, refer to the *IBM Personal System/2 Hardware Interface Technical Reference*.

Index

A

acoustic readings 1-11
activity light 3-48
adapter, fixed disk and diskette drive 3-6
address maps
  memory 3-22
  reassignment 3-16
  system 1-8
address 20 gate 3-48
alternate reset 3-49
arbiter programming 3-4
arbitration control point 3-3
arbitration level 3-3
arbitration register 3-5
arbitration, central control point 3-4

B

base memory bytes 3-42
battery 3-31
block diagram, system board 1-7
border screen 4-6
bus priority assignments 3-3

C

central arbitration control point 3-3
channel 1-6, 3-3
channel check enable 3-47
channel check latch 3-47
CMOS RAM 3-31
configuration CRC bytes 3-42
configuration, RT/CMOS 3-38
connectors 4-8
connectors, fixed disk and diskette drive 3-6
connector, display 4-12
connector, memory 3-29
connector, plasma display 4-12
connector, plasma display card 4-4, 4-8

D

date century byte 3-42
description
  memory 3-10
  NMI 3-46
  password 3-50
  real-time clock 3-31
  system 1-3
  system board 1-4
diagnostic status byte (RT/CMOS) 3-38
diagram, system board 1-7
diskette drive type byte 3-39
diskette overruns 3-4
distinctive-mapping 4-4, 4-7
DMA channels 3-4

E

enable NMI 3-32
enable, memory 3-17
equipment byte 3-41
error recovery 3-16
extended arbitration 3-5
extended graphics array 1-3
external storage device connector 3-8

F

fixed disk activity light 3-48
fixed disk connector 3-9

fixed disk drive initialization 3-38
fixed disk type byte 3-40

G

gate A20 3-48
gray patterns 4-8
gray scales 4-8

H

half-toning 4-4, 4-8
hard disk, see fixed disk

I

identifier, model 1-4
internal diskette drive
  connector 3-7
interrupts
  IRQ0 reset 3-47
  NMI reset 3-46
I/O address map 1-8

L

list of features 1-5

M

matched memory 3-3
math coprocessor
maximum current 1-10
measurements 1-10
memory
  connectors 3-29
  description 3-10
  enable bits 3-17
  error recovery 3-16
  performance 1-9
  reassigning 3-16
  refresh 3-4
  system memory maps 3-22
memory encoding registers 3-17
memory size miscompare 3-38
Micro Channel 1-6, 1-12, 3-3
microprocessor
  alternate reset 3-49
  mode switch compatibility 3-49
  performance 1-9
  real address mode 3-48
mode switching 3-49
model/submodel bytes 1-4

N

NMI mask 3-32
NMI service 3-4
NMI signal 3-4
noise readings 1-11
nonmaskable interrupt (NMI) 3-46

P

parity check enable 3-47
password, power-on 3-50
PDC 4-4
PEL, plasma display 4-3
performance 1-9, 3-3
plasma display 4-3
plasma display card 4-4
ports, system 3-46
power specifications 1-10
power supply 1-6
programmable option select (POS)
  system memory maps 3-22
programming, arbiter 3-4
protected mode switch 3-49

R

random access memory 3-11
read-only memory (ROM) 3-10
real mode switch 3-49
real-time clock bytes 3-34
refresh 3-4
refresh request 3-47

registers
memory encoding 3-17
miscellaneous system 3-46
RT/CMOS and NMI mask 3-32
RT/CMOS status registers 3-35
system control 3-46
resolution, plasma display 4-3
RT/CMOS address register 3-32
RT/CMOS RAM 3-31
password 3-50
secured area 3-48

S

SCSI 3-43
setup
system memory maps 3-22
shutdown status byte 3-39
signals 4-8
size 1-10
sound specifications 1-11
speaker data enable 3-47
specifications, system unit 1-10
status registers (RT/CMOS) 3-35
subsystems, memory 3-10
switch to real 3-49
system address map 1-8
system board 1-4
block diagram 1-7
features 1-4
memory connector 3-29
memory registers 3-17
model identifier 1-4
system control port A 3-48
system control ports 3-46
system description 1-3
system performance 1-9
system ports, miscellaneous 3-46
system reset 3-46
system unit specifications 1-10

T

time status indicator 3-38
type identifier 1-4

V

valid RAM bit 3-37
video mode 4-6

W

warnings
arbitration 3-4
central arbiter 3-5
NMI mask 3-46
real-time clock 3-32
reserved areas v
watchdog status 3-48

X

XGA 4-3, 4-4

Numerics

80386 performance 1-9

IBM Personal System/2 BIOS Interface Technical Reference Supplement for Model P75

This supplement contains programming considerations that apply to the BIOS section of the *IBM Personal System/2 and IBM Personal Computer BIOS Interface Technical Reference.*

This information should be used in addition to the material covered in the above manual.

File this page behind the *Supplements* tab in the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

System Identification

The IBM Personal System/2 Model P75 can have only one type of the system board. It has its own unique model and submodel byte. They can be read by a program that contains Interrupt hex 15, function code (AH) = hex C0. If the program is successfully executed, hex *08 F8 52 00 F6 78 000000* returns as the system response containing these bytes.

The following shows these bytes and system clock speed.

Model Byte	Submodel Byte	Revision Code	System Clock
F8	52	00	33MHz

Figure 1. System Identification

Programming Considerations for BIOS

The Model P75 is fully compatible with the BIOS and ABIOS in other Personal System/2 products.

Interrupt 10H - Video

(AH) = 00H - Set Mode: (AL) - Requested video mode

The following table lists hardware specific video mode characteristics:

Mode	Type	Colors to Program	Alpha Format	Font Box	Resolution to Program	Resolution on PDP	CRT Connected	PDP Enabled
0	A/N	B&W	40x25	8x8	320x200	640x400	S	S
0*	A/N	16/64	40x25	8x14	320x350	640x350	S	S
0+	A/N	16/256K	40x25	9x16	360x400	-	S	NS
0#	A/N	16/256K	40x25	8x16	320x400	640x400		S
1	A/N	16	40x25	8x8	320x200	640x400	S	S
1*	A/N	16/64	40x25	8x14	320x350	640x350	S	S
1+	A/N	16/256K	40x25	9x16	360x400	-	S	NS
1#	A/N	16/256K	40x25	8x16	320x400	640x400		S
2	A/N	B&W	80x25	8x8	640x200	640x400	S	S
2*	A/N	16/64	80x25	8x14	640x350	640x350	S	S
2+	A/N	16/256K	80x25	9x16	720x400	-	S	NS
2#	A/N	16/256K	80x25	8x16	640x400	640x400		S
3	A/N	16	80x25	8x8	640x200	640x400	S	S
3*	A/N	16/64	80x25	8x14	640x350	640x350	S	S
3+	A/N	16/256K	80x25	9x16	720x400	-	S	NS
3#	A/N	16/256K	80x25	8x16	640x400	640x400		S
4	APA	4/256K		8x16	320x200	640x400	S	S
5	APA	4/256K		8x16	320x200	640x400	S	S
6	APA	2/256K		8x16	640x200	640x400	S	S
7	A/N	B&W	80x25	9x14	720x350	-	S	NS
7*	A/N	B&W	80x25	8x14	640x350	640x350		S
7+	A/N	B&W	80x25	9x16	720x400	-	S	NS
7#	A/N	B&W	80x25	8x16	640x400	640x400		S
D	APA	16/256K		8x8	320x200	640x400	S	S
E	APA	16/256K		8x8	640x200	640x400	S	S
F	APA	2/256K		8x14	640x350	640x350	S	S
10	APA	16/256K		8x14	640x350	640x350	S	S
11	APA	2/256K		8x16	640x480	640x480	S	S
12	APA	16/256K		8x16	640x480	640x480	S	S
13	APA	256/256K		8x8	320x200	640x400(1)	S(2)	S(3)

Figure 2 (Part 1 of 2). Video Modes

Mode	Type	Colors to Program	Alpha Format	Font Box	Resolution to Program	Resolution on PDP	CRT Connected	PDP Enabled
XGA	A/N	16/256K	132x25	8x8	1056x200	-	S	NS
(132	A/N	16/256K	132x25	8x14	1056x350	-	S	NS
Col.)	A/N	16/256K	132x25	8x16	1056x400	-	S	NS
XGA	APA	256/256K			640x480	640x480	S(2)	NS(4)
XGA	APA	16/256K			1024x768	-	S(5)	NS(6)
XGA	APA	256/256K			1024x768	-	S(5)	NS(6)

Note:

S Indicates supported screen mode.
NS Indicates non-supported screen mode.
# Indicates new screen mode for the flat panel, symbols are temporary.
1 4 dots are used per 1 pixel.
2 When monochrome display attached, only 64 gray scales can be displayed.
3 Same as monochrome display. Only 64 gray scales can be displayed on PDP using Dither pattern.
4 If this video mode is called, the PDP displays only 16 gray scales, and the image may not be legible.
5 To use this mode, an 8514 or equivalent resolution monitor is needed.
6 PDPC automatically disables the PDP.

Figure 2 (Part 2 of 2). Video Modes

Notes:

1. The Plasma Display Panel works as an analog monochrome display.
2. When an external display is not attached, A/N 8 bit fonts only are available in modes 0#, 1#, 2#, 3#, 7#, and 7*.
3. The power-on default mode is 7# when an external PS/2 color display is not attached.
4. The power-on default mode is 3+ when an external PS/2 color display is attached.

(AH) =1BH - Return Functionality/State Information: For the Personal System/2 Model P75:

```
On Return:
   (DI+2DH) byte - Miscellaneous state information
                   Bit 7 - Reserved
                   Bit 6 = 1 - Plasma display active
                           (Without 9 dot width font)
                   Bit 5 = 0 - Background intensity
                         = 1 - Blinking
                   Bit 4 = 1 - Cursor emulation active
                   Bit 3 = 1 - Mode set default palette loading disabled
                   Bit 2 = 1 - Monochrome display attached
                   Bit 1 = 1 - Summing active
                   Bit 0 = 1 - All modes on all displays active
```

Notes:

1. When bit 6 is set to 1, the screen modes with 9-dot width font are not available. They are 0+, 1+, 2+, 3+, 7 and 7+.
2. If one of those modes is requested, BIOS automatically sets it to a mode with an 8-dot width font. They are 0#, 1#, 2#, 3#, 7#, and 7*.

```
On Return:
   (DI+2EH) byte - Advanced Function Information
                   Bit 7 - 3 - Reserved
                   Bit 2 = 1 - XGA present
                         = 0 - XGA not present
                   Bit 1 = 1 - XGA Driver not required
                         = 0 - XGA Driver required
                   Bit 0 = 1 - BIOS does not support
                               (XGA Information Return)
                         = 0 - BIOS supports
                               (XGA Information Return)
```

Video Supplement

This supplement contains programming considerations that apply to the Advanced BIOS section of the *IBM Personal System/2 and IBM Personal Computer BIOS Interface Technical Reference.*

This information should be used in addition to the material covered in the Advanced BIOS (ABIOS) section of the above manual.

Changes to Video ABIOS

The following are the model P75 video functions.

03H - Read Device Parameters

This function returns parameters that indicate the current video state.

Service Specific Output

SIZE	OFFSET	DESCRIPTION
Byte	+1B	Reserved
Byte	+1C	Number of scan lines on the screen 00H - 200 scan lines 01H - 350 scan lines 02H - 400 scan lines 03H - 480 scan lines 04H to FFH - Reserved
Word	+1E	Video mode setting
Word	+20	Type of monitor attached Bits 15 to 2 - Reserved Bit 1 - Plasma display 0 - Inactive 1 - Active Bit 0 - Color vs Monochrome 0 - Color display 1 - Monochrome display
Word	+22	Character height (bytes/character)
Word	+24	Character block specifier Bits 15 to 12 - Reserved Bits 11 to 8 - Character block select A Bits 7 to 4 - Reserved Bits 3 to 0 - Character block select B
Word	+2A	Size of data buffer required for the Return ROM Fonts function in bytes.
Word	+2E	Size of save/restore buffer header in bytes.
Word	+30	Size of save/restore hardware state in bytes.
Word	+32	Size of save/restore device block state in bytes.
Word	+34	Size of save/restore DAC state in bytes.

Notes:

1. When offset +20 bit 1 is set to 1, the screen modes with 9-dot width font are not available. They are 0+, 1+, 2+, 3+, 7 and 7+.
2. If one of those modes is requested, BIOS automatically sets it to a mode with 8-dot width font. They are 0#, 1#, 2#, 3#, 7#, and 7*.

Personal System/2
Model 76
Technical Reference

Note

Before using this information and the product it supports, be sure to read the general information under "Notices" on page vii.

First Edition (September 1992)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer of express or implied warranties in certain transactions, therefore, this statement may not apply to you.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Requests for technical information about IBM products should be made to your IBM Authorized Dealer or your IBM Marketing Representative.

© Copyright International Business Machines Corporation 1992. All rights reserved.
Note to U.S. Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Contents

Figures v

Notices vii
Trademarks and Service Marks vii

Preface ix

Section 1. System Overview 1-1
Description 1-3
System Board Devices and Features 1-4
System Board I/O Address Map 1-6
Micro Channel Compatibility 1-8
Specifications 1-9
Power Supply 1-12
Outputs 1-13
Output Protection 1-14
Voltage Sequencing 1-14
Power-Supply Connectors 1-14

Section 2. Programmable Option Select 2-1
Description 2-3
POS I/O Address Map 2-5
Card Selected Feedback Register (Hex 0091) 2-6
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-7
System Board Group 1 POS Register 2 (Hex 0102) 2-8
System Board Group 1 POS Register 3 (Hex 0103) 2-9
System Board Group 1 POS Register 4 (Hex 0104) 2-11
System Board Group 1 POS Register 5 (Hex 0105) 2-11
System Board Group 2 POS Register 2 (Hex 0102) 2-12
System Board Group 2 POS Register 3 (Hex 0103) 2-12
System Board Group 3 POS Register 2 (Hex 0102) 2-13
System Board Group 3 POS Register 3 (Hex 0103) 2-13
Adapter Enable/Setup Register (Hex 0096) 2-15

Section 3. System Board 3-1
Description 3-3
Microprocessor and Math Coprocessor 3-3
Micro Channel Architecture Implementation 3-3
The Central Arbiter 3-3
Arbitration Bus Priority Assignments 3-4
Central Arbiter Programming 3-5

© Copyright IBM Corp. 1992

The Bus Extension 3-6
Diskette Drive Connectors 3-7
System Board Memory Connectors 3-8
SCSI-Device Connector 3-9
Memory 3-10
ROM Subsystem 3-11
RAM Subsystem 3-11
Memory Subsystem Control 3-12
Memory-Presence Determination 3-12
Cached Memory Address Space 3-13
RT/CMOS RAM 3-16
Miscellaneous System Functions and Ports 3-25
Nonmaskable Interrupt 3-25
System Control Port B (Hex 0061) 3-26
System Control Port A (Hex 0092) 3-27
Power-On Password 3-28
Selectable Boot Sequence 3-29
Hardware Compatibility 3-29
Error Codes 3-30

Index X-1

Figures

1-1. Model and Submodel Bytes 1-3
1-2. System Board Devices and Features 1-4
1-3. System Board I/O Address Map 1-6
1-4. Performance Specifications—25 MHz 1-9
1-5. Performance Specifications—33 MHz 1-10
1-6. Physical Specifications 1-11
1-7. Declared Acoustical Noise Emission Values 1-12
1-8. Component Maximum Current 1-13
1-9. Channel Load Current 1-13
1-10. Voltage Assignments for the Internal Power-Supply Connectors 1-14
2-1. POS I/O Address Map 2-5
2-2. Card Selected Feedback Register (Hex 0091) 2-6
2-3. Devices Supported in Setup Mode 2-7
2-4. System Board Enable/Setup Register (Hex 0094) 2-7
2-5. System Board POS Register 2 (Hex 0102) 2-8
2-6. Parallel Port Select Bits 2-8
2-7. System Board Group 1 POS Register 3 (Hex 0103) 2-9
2-8. System Board POS Group 1 Register 3 (Hex 0103)—Index 00 2-10
2-9. System Board POS Group 1 Register 3 (Hex 0103)—Index 04 2-10
2-10. System Board POS Group 1 Register 3 (Hex 0103)—Index 01 2-10
2-11. System Board Group 1 POS Register 4 (Hex 0104) . . . 2-11
2-12. System Board Group 1 POS Register 5 (Hex 0105) . . . 2-11
2-13. System Board Group 2 POS Register 2 (Hex 0102) . . . 2-12
2-14. System Board Group 2 POS Register 3 (Hex 0103) . . . 2-12
2-15. Serial Port Addresses 2-12
2-16. System Board Group 3 POS Register 2 (Hex 0102) . . . 2-13
2-17. System Board Group 3 POS Register 3 (Hex 0103) . . . 2-13
2-18. System Board SCSI Controller ID 2-14
2-19. Adapter Enable/Setup Register (Hex 0096) 2-15
3-1. Arbitration Bus Priority Assignments 3-4
3-2. Arbitration Register (Hex 0090)—Write 3-5
3-3. Arbitration Register (Hex 0090)—Read 3-5
3-4. Diskette Drive Connectors 3-7
3-5. System Board Memory Connectors 3-8
3-6. Internal SCSI-Device Connector Pin Assignments 3-9
3-7. External SCSI-Device Connector Pin Assignments . . . 3-10
3-8. Presence-Detect Bits 3-12
3-9. Memory Map, Cached Regions—System Memory . . . 3-14

© Copyright IBM Corp. 1992

3-10. Memory Map, Cached Regions—Nonsystem Memory from 8MB to 16MB 3-15
3-11. RT/CMOS RAM Address Map 3-16
3-12. RT/CMOS Address and NMI Mask Register (Hex 0070) 3-17
3-13. RT/CMOS Data Register (Hex 0071) 3-17
3-14. Real-Time Clock Bytes (Hex 000–00D) 3-18
3-15. Status Register A (Hex 00A) 3-18
3-16. Status Register B (Hex 00B) 3-19
3-17. Status Register C (Hex 00C) 3-20
3-18. Status Register D (Hex 00D) 3-21
3-19. Diagnostic Status Byte (Hex 00E) 3-21
3-20. Diskette Drive Type Byte (Hex 010) 3-22
3-21. First Diskette Drive Type Bits 3-22
3-22. Second Diskette Drive Type Bits 3-22
3-23. Equipment Byte (Hex 014) 3-23
3-24. Installed Diskette Drive Bits 3-23
3-25. Display Operating Mode Bits 3-24
3-26. System Control Port B (Hex 0061)—Write 3-26
3-27. System Control Port B (Hex 0061)—Read 3-26
3-28. System Control Port A (Hex 0092) 3-27
3-29. POST Error Messages 3-31

Notices

References in this publication to IBM products, programs, or services do not imply that IBM intends to make these available in all countries in which IBM operates. Any reference to an IBM product, program or service is not intended to state or imply that only IBM's product, program, or service may be used. Any functionally equivalent product, program, or service that does not infringe any of IBM's intellectual property rights or other legally protectable rights may be used instead of the IBM product, program, or service. Evaluation and verification of operation in conjunction with other products, programs, or services, except those expressly designated by IBM, are the user's responsibility.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

Trademarks and Service Marks

The following terms, denoted by an asterisk (*) in this publication, are trademarks of the IBM Corporation in the United States and/or other countries:

IBM
Micro Channel
Personal Computer AT
Personal System/2
PS/2
XGA

The following terms, denoted by a double asterisk (**) in this publication, are trademarks of other companies as follows:

Intel	Intel Corporation
Motorola	Motorola, Incorporated
National Semiconductor	National Semiconductor Corporation

© Copyright IBM Corp. 1992

Notes:

Preface

The Technical Reference library is intended for those who develop hardware and software products for IBM Personal Computers and IBM Personal System/2 products. Users should understand computer architecture and programming concepts.

This manual consists of the following sections:

Section 1, "System Overview," describes the system, features, and specifications.

Section 2, "Programmable Option Select," describes the registers that are used for configuration.

Section 3, "System Board," describes the system-specific hardware implementations of the Micro Channel architecture.

This technical reference should be used with the following publications. These publications contain additional information about many of the subjects that are discussed in this technical reference.

IBM Personal System/2 Hardware Interface Technical Reference—Architectures

IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference

Information about diskette drives, fixed disk drives, adapters, and external options are in separate option technical references.

Warning: The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

© Copyright IBM Corp. 1992

Notes:

Section 1. System Overview

Description 1-3
System Board Devices and Features 1-4
System Board I/O Address Map 1-6
Micro Channel Compatibility 1-8
Specifications 1-9
Power Supply 1-12
  Outputs 1-13
  Output Protection 1-14
  Voltage Sequencing 1-14
  Power-Supply Connectors 1-14

© Copyright IBM Corp. 1992

Notes:

Description

The IBM* Personal System/2* (PS/2*) Model 76 computer is a self-contained desktop computer system with a keyboard. It supports up to three internal direct access storage devices (DASD). Two of these devices can be either removable-media DASD (such as diskette, tape, or optical) or nonremovable-media DASD. The third device is a hidden, nonremovable-media DASD.

Programs determine the type of system board by reading the model and submodel bytes. Interrupt 15H, Return System Configuration Parameters function ((AH)=C0H) returns the model byte, submodel byte, and BIOS revision code.

The following figure lists the model and submodel bytes, microprocessor types, and system-clock speeds for the Model 76 system board.

Model Byte (Hex)	Submodel Byte (Hex)	Microprocessor	System Clock
F8	41	80486SX	25 MHz
F8	41	80486DX2	25 MHz/50 MHz
F8	41	80486SX	33 MHz
F8	41	80486DX2	33 MHz/66 MHz

Figure 1-1. Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems.

* Trademark of the IBM Corporation.

System Board Devices and Features

The following figure lists the system board devices and features. The *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* describes, by type number, the devices that are common to PS/2 products.

Device	Type	Features
Microprocessor	—	80486SX—25 MHz or 80486SX—33 MHz - 32-bit address interface, 32-bit data interface
System Timers	1	Channel 0—System timer Channel 2—Tone generation for speaker Channel 3—Watchdog timer
ROM Subsystem	—	128KB logical ROM (KB equals 1024 bytes)
RAM Subsystem	—	Four connectors (2MB to 32MB) (MB equals 1048576 bytes)
CMOS RAM Subsystem	—	64-byte CMOS RAM with real-time clock, calendar, 8KB CMOS RAM extension, and battery backup
Audio Subsystem	1	Driven by - System-timer channel 2 - The 'audio sum node' signal
DMA Controller	1	Eight independent DMA channels Single or burst transfers with read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level sensitive

Figure 1-2 (Part 1 of 2). System Board Devices and Features

Device	Type	Features
Video Subsystem	2	XGA*-2 video with 1MB video memory - Supports refresh rates up to 75 MHz - Supports direct color mode (65536 colors) - Contains XGA-2 Display Adapter/A
Keyboard/Auxiliary Device Controller	2	Keyboard connector Auxiliary-device connector Password security
Diskette Drive Controller	2	Supports: - 3.5-in. diskette drive (1.44MB and 2.88MB) - 5.25-in. diskette drive (360KB and 1.2MB)
Serial Controller Port	4	RS-232C interface - Two 9-pin connectors - Programmable as serial ports 1–16 - DMA, FIFO, and character modes
Parallel Controller Port	3	Programmable as parallel ports 1–4 - Supports bidirectional input and output - Supports DMA operation
SCSI Controller	1	Supports two internal SCSI devices Supports up to seven SCSI devices
Micro Channel* Connectors	—	Three connectors for Type 3 adapters - One 32-bit connector with base-video extension (contains XGA-2 Display Adapter/A) - One 32-bit connector with auxiliary-video extension - One 32-bit connector with matched-memory support
Math Coprocessor Socket	—	Supports 80487SX math coprocessor option with the same clock speed as the system microprocessor; supports microprocessor upgrades 80486DX2—25 MHz/50 MHz and 80486DX2—33 MHz/66 MHz

Figure 1-2 (Part 2 of 2). System Board Devices and Features

* Trademark of the IBM Corporation.

System Board I/O Address Map

The following figure is the Model 76 system board I/O address map.

Address (Hex)	Device
0000–001F	DMA controller
0020, 0021	Interrupt controller
0040, 0042–0044, 0047	System timers
004B–004F	32-bit free-running timer
0060	Keyboard, auxiliary device
0061	System Control Port B
0064	Keyboard, auxiliary device
0066, 0067	Keyboard, auxiliary device
0070, 0071	RT/CMOS and NMI mask
0081–008F	DMA controller
0080	Central arbitration control point
0091	Card Selected Feedback register
0092	System Control Port A
0094	System Board Enable/Setup register
0096	Adapter Enable/Setup register
00A0, 00A1	Interrupt controller
00C0–00DF	DMA controller (4–7)
00E0–00E8	Memory controller
00F0–00FF	Math coprocessor
0100–0107	Programmable option select
0278–027D	Parallel port 3
02F8–02FF	Serial port 2
0378–037D	Parallel port 2
03B4, 03B5, 03BA	Video subsystem
03BC–03BF	Parallel port 1
03C0–03C5	Video subsystem
03C6–03C9	Video DAC
03CA, 03CC, 03CE, 03CF	Video subsystem
03D4, 03D5, 03DA	Video subsystem
03F0–03F7	Diskette drive controller
03F8–03FF	Serial port 1
1278–127D	Enhanced parallel port 1
1378–137D	Parallel port 4

Note: I/O addresses below hex 0100 that are not listed are reserved.

Figure 1-3 (Part 1 of 2). System Board I/O Address Map

Address (Hex)	Device
2100 – 210F	XGA video, instance 0
2110 – 211F	XGA video, instance 1
2120 – 212F	XGA video, instance 2
2130 – 213F	XGA video, instance 3
2140 – 214F	XGA video, instance 4
2150 – 215F	XGA video, instance 5
2160 – 216F	XGA video, instance 6
2170 – 217F	XGA video, instance 7
3220 – 3227	Serial port 3
3228 – 322F	Serial port 4
3540 – 3547	SCSI controller, instance 0
3548 – 354F	SCSI controller, instance 1
3550 – 3557	SCSI controller, instance 2
3558 – 355F	SCSI controller, instance 3
3560 – 3567	SCSI controller, instance 4
3568 – 356F	SCSI controller, instance 5
3570 – 3577	SCSI controller, instance 6
3578 – 357F	SCSI controller, instance 7
3A20 – 3A27	Serial port 9
3A28 – 3A2F	Serial port 10
3A30 – 3A37	Serial port 11
3A38 – 3A3F	Serial port 12
3A80 – 3A87	Serial port 13
3A88 – 3A8F	Serial port 14
3A90 – 3A97	Serial port 15
3A98 – 3A9F	Serial port 16
4220 – 4227	Serial port 5
4228 – 422F	Serial port 6
4620 – 462F	Serial port arbitration-level control
5220 – 5227	Serial port 7
5228 – 522F	Serial port 8
82F8 – 82FF	Enhanced serial port 2
83F8 – 83FF	Enhanced serial port 1
B220 – B227	Enhanced serial port 3
B228 – B22F	Enhanced serial port 4
BA20 – BA27	Enhanced serial port 9
BA28 – BA2F	Enhanced serial port 10
BA30 – BA37	Enhanced serial port 11
BA38 – BA3F	Enhanced serial port 12
BA80 – BA87	Enhanced serial port 13
BA88 – BA8F	Enhanced serial port 14
BA90 – BA97	Enhanced serial port 15
BA98 – BA9F	Enhanced serial port 16
C220 – C227	Enhanced serial port 5
C228 – C22F	Enhanced serial port 6
D220 – D227	Enhanced serial port 7
D228 – D22F	Enhanced serial port 8

Figure 1-3 (Part 2 of 2). System Board I/O Address Map

Micro Channel Compatibility

The following terms describe system limitations in the support of Micro Channel architecture.

Streaming Data

The system board supports 10-MHz streaming-data procedures involving data transfers between adapters; devices on the system board do not use streaming-data procedures. Data transfers default to the basic transfer procedure.

Data Parity

Data- and address-parity procedures are not supported in this system. Data transfers default to the basic transfer procedure.

Selected Feedback Return Signal

The system board supports the 'selected feedback return' signal, except for the I/O devices at addresses below hex 0100. These devices are controlled by the system master only and should not be accessed by bus masters.

Synchronous Channel Checks

Synchronous channel checks for errors other than Micro Channel data-parity errors are not supported in this system.

Synchronous channel checks for data-parity errors, which are typically issued by slaves, are the responsibility of the master that owned the channel and issued the access to the slave. However, in this system, these channel checks are detected by logic on the system board, resulting in a nonmaskable interrupt (NMI).

DMA

In this system, the DMA controller supports DMA slaves with 8-bit or 16-bit data widths.

Specifications

The following figure describes the performance specifications of the Model 76 running at 25 MHz.

Device	Cycle Time (ns)
Microprocessor (25 MHz, 40-ns clock)	
Access to system board RAM	
Memory read (internal cache miss)	
Page hit	280
Page miss	320/400
Memory write	
Page hit	120
Page miss	160/240
Access to channel	
Default transfer cycle	320
Synchronous transfer cycle	440
Refresh Rate (typically performed every 15.1 μs)	320
Bus-Master Access to System Board RAM	300 (min)
DMA Controller (10 MHz, 100-ns clock)	
Single transfer: 300 + (I/O access + memory access)	
Burst transfer: 300 + (I/O access + memory access)*n*†	
System board memory read	320 (min)
System board memory write	320 (min)
Access to channel	
Default transfer cycle	350 (min)
Synchronous transfer cycle	450 (min)

† *n* equals the number of data transfers in the burst.

Figure 1-4. Performance Specifications—25 MHz

The following figure describes the performance specifications of the Model 76 running at 33 MHz.

Device	Cycle Time (ns)
Microprocessor (33 MHz, 30-ns clock)	
Access to system board RAM	
Memory read (internal cache miss)	
Page hit	240
Page miss	270/330
Memory write	
Page hit	120
Page miss	150/210
Access to channel	
Default transfer cycle	300
Synchronous transfer cycle	420
Refresh Rate (typically performed every 15.1 μs)	400
Bus-Master Access to System Board RAM	300 (min)
DMA Controller (10 MHz, 100-ns clock)	
Single transfer: 300 + (I/O access + memory access)	
Burst transfer: 300 + (I/O access + memory access)*n*†	
System board memory read	300 (min)
System board memory write	300 (min)
Access to channel	
Default transfer cycle	300 (min)
Synchronous transfer cycle	420 (min)
† *n* equals the number of data transfers in the burst.	

Figure 1-5. Performance Specifications—33 MHz

The following figure describes the physical specifications of the Model 76.

Specification	Measurements
Size	
Width	360 mm (14.2 in.)
Depth	395 mm (15.6 in.)
Height	115 mm (4.5 in.)
Weight	
Minimum configuration	6.0 kg (13.8 lb)
Maximum configuration	10.9 kg (24.0 lb)
Cables	
Power cable	1.8 m (6 ft)
Keyboard cable	1.8 m (6 ft)
Air Temperature	
System on	
0 – 7000 ft altitude	10.0 to 35.0°C (50 to 95°F)
System off	10.0 to 43.0°C (50 to 110°F)
Humidity	
System on	8% to 85%
System off	5% to 85%
Maximum Altitude†	2133.6 m (7000 ft)
Heat Output	(135 watts) 460 BTU per hour
Acoustical Readings	See Figure 1-7 on page 1-12
Electrical	
Input voltage (range is automatically selected; sinewave input is required)	
Low range	90 (min) – 137 (max) V ac
High range	180 (min) – 265 (max) V ac
Input frequency	50 Hz ± 3 Hz or 60 Hz ± 3 Hz
Maximum current draw	
Low range	3.5 A
High range	1.75 A
Input, in kilovolt-ampere (kVA)	
Minimum configuration (as shipped by IBM)	0.06 kVA
Maximum configuration	0.35 kVA
Electromagnetic Compatibility	FCC Class B

† This is the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.

Figure 1-6. Physical Specifications

The following figure contains the acoustical readings of the Model 76.

Description	L_{WAd} in bels Operate	Idle	L_{pAm} in dB Operate	Idle	$<L_{pA}>_m$ in dB Operate	Idle
Model 76	5.0	5.0	40	40	38	38

Notes:

L_{WAd} The declared upper limit A-weighted sound power level for a random sample of machines

L_{pAm} The mean value of the A-weighted sound pressure level at the operator position (if any) for a random sample of machines

$<L_{pA}>_m$ The mean value of the A-weighted sound pressure levels at the one-meter (bystander) positions for a random sample of machines

All measurements are made in accordance with ANSI standard S12.10 and are reported in conformance with ISO DIS 9296.

These measurements are preliminary data and are subject to change.

Figure 1-7. Declared Acoustical Noise Emission Values

Power Supply

The power supply converts the ac input voltage to three dc output voltages and provides power for the following:

- System board
- Micro Channel adapters
- Internal DASD drives
- Auxiliary devices
- Keyboard

The power switch and two light-emitting diodes (LED) are on the front of the system unit. When the green LED is lit, it indicates that the power supply is operating properly. The amber LED is the fixed-disk-activity indicator.

Outputs

The power supply provides separate voltage sources for the system board and the internal fixed disk drives. The system board voltages are +5 V dc, +12 V dc, and −12 V dc. The drive voltages are +5 V dc and +12 V dc.

The following figure shows the maximum current that is provided for system components.

System Component	Maximum Current	
	+12 V dc	+5 V dc
Internal fixed disk drives†	2.8 A	2.71 A
Auxiliary-device port	None	300 mA
Keyboard port	None	275 mA
† Total for the two power-supply connectors		

Figure 1-8. Component Maximum Current

The following figure shows the maximum load currents that are allowed for each channel connector.

Supply Voltage	Maximum Load Current
+ 5.0 V dc	1.6 A
+12.0 V dc	0.175 A
−12.0 V dc	0.040 A

Figure 1-9. Channel Load Current

The formulas that are used to determine the power requirements and the voltage-regulation tolerances are in the Micro Channel architecture information in the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures.*

Output Protection

A short circuit that is placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state, with no damage to the power supply.

If an overvoltage fault occurs (in the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of the nominal value of the power supply.

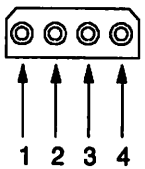
If either of these shutdown states occurs, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least 10 seconds.

Voltage Sequencing

At power-on time, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Power-Supply Connectors

The power supply provides two 4-pin connectors for internal devices. The total power that is used by both connectors must not exceed the amount shown in Figure 1-8 on page 1-13.



Pin	Signal	Pin	Signal
1	+12 V dc	3	dc return
2	dc return	4	+5 V dc

Figure 1-10. Voltage Assignments for the Internal Power-Supply Connectors

Section 2. Programmable Option Select

Description 2-3
POS I/O Address Map 2-5
Card Selected Feedback Register (Hex 0091) 2-6
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-7
System Board Group 1 POS Register 2 (Hex 0102) 2-8
System Board Group 1 POS Register 3 (Hex 0103) 2-9
System Board Group 1 POS Register 4 (Hex 0104) 2-11
System Board Group 1 POS Register 5 (Hex 0105) 2-11
System Board Group 2 POS Register 2 (Hex 0102) 2-12
System Board Group 2 POS Register 3 (Hex 0103) 2-12
System Board Group 3 POS Register 2 (Hex 0102) 2-13
System Board Group 3 POS Register 3 (Hex 0103) 2-13
Adapter Enable/Setup Register (Hex 0096) 2-15

© Copyright IBM Corp. 1992

Notes:

Description

Programmable Option Select (POS) eliminates the need for switches on the system board by replacing their function with programmable registers. This section describes the POS information that is used on the Model 76 system board. For additional information about POS, refer to the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures*.

Warning:

- Programmable options should be set only through the System Configuration utility programs. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignments of the same system resource, improper operation of the feature, loss of data, or damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention occurs, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- The channel-reset bit (bit 7) in the Adapter Enable/Setup register (hex 0096) must be set to 0 to program the adapters.
- The system board does not support 16-bit I/O operations to 8-bit POS registers. Using 16-bit I/O instructions on 8-bit POS registers causes incorrect data to be written to or read from the registers. Only 8-bit transfers are supported for setup operations.

Setup functions respond to I/O addresses hex 0100 through hex 0107 only when their unique setup signal is active. The following precautions must be taken before individual bits are set in the POS registers.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register must be set to 1 to allow adapter setup.
- Bits 7, 6, and 1 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system board functions.

System Board Setup Group 1:

- Bit 7 in the System Board Enable/Setup register must be set to 0 to enable setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bits 6 and 1 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system board functions.

System Board Setup Group 2:

- Bit 6 in the System Board Enable/Setup register must be set to 0 to enable setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bits 7 and 1 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system board functions.

System Board Setup Group 3:

- Bit 1 in the System Board Enable/Setup register must be set to 0 to enable setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bits 7 and 6 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem or other system board functions.

POS I/O Address Map

The following figure shows the organization of the I/O address space that is used by POS. Bit 0 of POS Register 2 and bits 6 and 7 of POS Register 5 are fixed. All other bits in POS Registers 2 through 5 are free-form.

Address (Hex)	Register
0094	System Board Enable/Setup register
0096	Adapter Enable/Setup register
0100	POS Register 0—Adapter Identification byte (low byte)
0101	POS Register 1—Adapter Identification byte (high byte)
0102	POS Register 2—Option Select Data byte 1 (bit 0 is card enable)
0103	POS Register 3—Option Select Data byte 2
0104	POS Register 4—Option Select Data byte 3
0105	POS Register 5—Option Select Data byte 4
0106	Reserved
0107	Reserved

Figure 2-1. POS I/O Address Map

Card Selected Feedback Register (Hex 0091)

Whenever an adapter is addressed, it responds by setting the '-card selected feedback' signal (-CD SFDBK) to active. This signal is derived from the address decode, driven by a totem-pole driver, and latched by the system board. It can be read through the Card Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs can use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and determine whether the system board I/O or an adapter is addressed and functioning.

Bit	Function
7–1	Reserved
0	Card selected feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7–1 These bits are reserved.

Bit 0 This bit is set to 1 when -CD SFDBK was active on a previous cycle or when a system board I/O function (diskette drive, serial port, or parallel port interface) is accessed by an I/O cycle. Reading this register resets this bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information in three sets of POS registers: Groups 1 through 3.

- The diskette drive controller, parallel port, and system board memory are configured through the Group 1 POS registers.
- The serial ports are configured through Group 2.
- The small computer system interface (SCSI) controller is configured through Group 3.

Figure 2-3 indicates the groups, POS register numbers, and I/O functions that are supported.

Group	POS Register	Device
1	2	Diskette drive controller Parallel port controllers
1	3	Memory connectors
1	4	Diskette arbitration level
1	5	Parallel port arbitration level
2	2, 3	Serial port controller
3	2, 3	SCSI controller

Figure 2-3. Devices Supported in Setup Mode

System Board Enable/Setup Register (Hex 0094)

This is a read/write register. All bits in this register default to 1 (enabled).

Bit	Function
7	Enable/setup system board group 1
6	Enable/setup system board group 2
5–2	Reserved
1	Enable/setup SCSI controller
0	Reserved

Figure 2-4. System Board Enable/Setup Register (Hex 0094)

Bit 7 When this bit is set to 0, the diskette drive controller, parallel port controllers, memory connectors, diskette arbitration level, and parallel port arbitration level are placed into setup mode.

When this bit is set to 1, the system board functions are enabled.

Bit 6 When this bit is set to 0, the system board serial controller is placed into setup mode. System Board Group 2 POS Register 2 (hex 0102) includes the serial port enable and interrupt-level selection. The serial port address selection is in System Board Group 2 POS Register 3 (hex 0103).

Bits 5–2 These bits are reserved.

Bit 1 When this bit is set to 0, the SCSI controller on the system board is placed into setup mode and is controlled through POS Register 2 (hex 0102). When this bit is set to 1 and bit 0 in POS Register 2 is set to 1, the SCSI controller on the system board is enabled.

Bit 0 This bit is reserved.

System Board Group 1 POS Register 2 (Hex 0102)

When the system board is in setup mode, this read/write register controls the diskette drive controller and parallel port. Reading this register returns the current state of the following system board functions.

Bit	Function
7	Disable parallel port extended mode
6, 5	Select parallel port
4	Enable parallel port
3	Reserved
2	Reserved
1	Enable diskette drive interface
0	Enable system board

Figure 2-5. System Board POS Register 2 (Hex 0102)

Bit 7 When this bit is set to 0, the parallel port is configured as an 8-bit, parallel, bidirectional (extended mode) interface. When this bit is set to 1, the parallel port is configured as an 8-bit, parallel, unidirectional interface (extended mode is disabled). This bit is set to 0 after the system is powered-on.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Address (Hex)	Interrupt Level
0 0	Parallel 1	03BC – 03BF†	7
0 1	Parallel 2	0378 – 037D	7
1 0	Parallel 3	0278 – 027D	7
1 1	Parallel 4	1378 – 137D	7

† The addresses are hex 1278 – 127D for the DMA operations.

Figure 2-6. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bits 3, 2 These bits are reserved.

Bit 1 When this bit and bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When this bit is set to 1, the individual device controllers on the system board can be enabled and disabled. When this bit is set to 0, the system board controllers for the diskette drive, serial port, and parallel port are disabled.

System Board Group 1 POS Register 3 (Hex 0103)

The system board has connectors for installing single inline memory modules (memory modules); for more information about these memory connectors, see "System Board Memory Connectors" on page 3-8.

Each memory module is defined by five signals: 'presence detect 0−3' and '-ECC memory.' The states of these signals are indicated by 3 bytes that are accessed through POS Register 3. To read each byte, write the appropriate index to POS Register 3, and then read POS Register 3.

The following figure shows the relationship of the index values to the memory connectors and the available data register information.

Index Value (Hex)	Function
00	Presence-detection information for memory connectors 3 and 1
04	-ECC memory for connectors 1 through 4
01	Presence-detection information for memory connectors 4 and 2

Note: Values that are not shown are reserved.

Figure 2-7. System Board Group 1 POS Register 3 (Hex 0103)

The following information is returned by reading POS Register 3 after the appropriate index value has been written to POS Register 3. For coding of the presence-detection signals, see Figure 3-8 on page 3-12.

Index 00 Bit	Function
7	Presence detect 3, memory connector 3
6	Presence detect 2, memory connector 3
5	Presence detect 1, memory connector 3
4	Presence detect 0, memory connector 3
3	Presence detect 3, memory connector 1
2	Presence detect 2, memory connector 1
1	Presence detect 1, memory connector 1
0	Presence detect 0, memory connector 1

Figure 2-8. System Board POS Group 1 Register 3 (Hex 0103)—Index 00

Index 04 Bit	Function
7	-Alternative microprocessor or math coprocessor installed (80486DX2 or 80487SX)
6	Base microprocessor speed (0=25 MHz, 1=33 MHz)
5	Current microprocessor speed (0=25 MHz, 1=33 MHz)
4	Reserved
3	-ECC memory, memory connector 4
2	-ECC memory, memory connector 3
1	-ECC memory, memory connector 2
0	-ECC memory, memory connector 1

Figure 2-9. System Board POS Group 1 Register 3 (Hex 0103)—Index 04

Index 01 Bit	Function
7	Presence detect 3, memory connector 4
6	Presence detect 2, memory connector 4
5	Presence detect 1, memory connector 4
4	Presence detect 0, memory connector 4
3	Presence detect 3, memory connector 2
2	Presence detect 2, memory connector 2
1	Presence detect 1, memory connector 2
0	Presence detect 0, memory connector 2

Figure 2-10. System Board POS Group 1 Register 3 (Hex 0103)—Index 01

System Board Group 1 POS Register 4 (Hex 0104)

This register is used to specify the diskette drive arbitration level.

Bit	Function
7–4	Reserved
3–0	Diskette drive arbitration level

Figure 2-11. System Board Group 1 POS Register 4 (Hex 0104)

Bits 7–4 These bits are reserved.

Bits 3–0 These bits are used to select the diskette drive arbitration level.

System Board Group 1 POS Register 5 (Hex 0105)

This register is used to specify the arbitration level that is used by the parallel port controller.

Bit	Function
7–4	Reserved
3–0	Parallel port arbitration level

Figure 2-12. System Board Group 1 POS Register 5 (Hex 0105)

Bits 7–4 These bits are reserved.

Bits 3–0 These bits are used to select the arbitration level that is used by the parallel port controller.

System Board Group 2 POS Register 2 (Hex 0102)

This register is used to enable the system board serial port.

Bit	Function
7–5	Reserved
4	Enable serial port B
3	Enable serial port A
2	Reserved
1	Select serial port B interrupt
0	Select serial port A interrupt

Figure 2-13. System Board Group 2 POS Register 2 (Hex 0102)

Bits 7–5 These bits are reserved.

Bit 4 When this bit is set to 1 and bit 0 in POS Register 2 (Group 1) is set to 1, serial port B is enabled.

Bit 3 When this bit is set to 1 and bit 0 in POS Register 2 (Group 1) is set to 1, serial port A is enabled.

Bit 2 This bit is reserved.

Bit 1 When this bit is set to 1, serial port B uses IRQ4. When this bit is set to 0, serial port B uses IRQ3.

Bit 0 When this bit is set to 1, serial port A uses IRQ4. When this bit is set to 0, serial port A uses IRQ3.

System Board Group 2 POS Register 3 (Hex 0103)

This register is used to select the addresses of the two serial ports.

Bit	Function
7–4	Serial port B address
3–0	Serial port A address

Figure 2-14. System Board Group 2 POS Register 3 (Hex 0103)

Bits 7–4 These bits are used to determine the address of serial port B (right).

Bits 3–0 These bits are used to determine the address of serial port A (left).

Bits 7 6 5 4 3 2 1 0	Assignment	Address (Hex)	
		Compatible	Extended
0 0 0 0	Serial 1	03F8 – 03FF	83F8 – 83FF
0 0 0 1	Serial 2	02F8 – 02FF	82F8 – 82FF
0 0 1 0	Serial 3	3220 – 3227	B220 – B227
0 0 1 1	Serial 4	3228 – 322F	B228 – B22F
0 1 0 0	Serial 5	4220 – 4227	C220 – C227
0 1 0 1	Serial 6	4228 – 422F	C228 – C22F
0 1 1 0	Serial 7	5220 – 5227	C220 – D227
0 1 1 1	Serial 8	5228 – 522F	D228 – D22F
1 0 0 0	Serial 9	3A20 – 3A27	BA20 – BA27
1 0 0 1	Serial 10	3A28 – 3A2F	BA28 – BA2F
1 0 1 0	Serial 11	3A30 – 3A37	BA30 – BA37
1 0 1 1	Serial 12	3A38 – 3A3F	BA38 – BA3F
1 1 0 0	Serial 13	3A80 – 3A87	BA80 – BA87
1 1 0 1	Serial 14	3A88 – 3A8F	BA88 – BA8F
1 1 1 0	Serial 15	3A90 – 3A97	BA90 – BA97
1 1 1 1	Serial 16	3A98 – 3A9F	BA98 – BA9F

Figure 2-15. Serial Port Addresses

System Board Group 3 POS Register 2 (Hex 0102)

This register is used to enable the SCSI controller on the system board.

Bit	Function
7 – 1	Reserved
0	Enable SCSI

Figure 2-16. System Board Group 3 POS Register 2 (Hex 0102)

Bits 7 – 1 These bits are reserved.

Bit 0 When this bit is set to 1, the SCSI controller on the system board is enabled.

System Board Group 3 POS Register 3 (Hex 0103)

This register is used to select the SCSI ID for the SCSI controller on the system board.

Bit	Function
7 – 5	SCSI ID
4 – 0	Reserved

Figure 2-17. System Board Group 3 POS Register 3 (Hex 0103)

Bits 7 – 5 These bits determine the SCSI ID for the SCSI controller on the system board.

Bits 7 6 5	System Board SCSI ID
0 0 0	0
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	4
1 0 1	5
1 1 0	6
1 1 1	7

Figure 2-18. System Board SCSI Controller ID

Bits 4 – 0 These bits are reserved.

Adapter Enable/Setup Register (Hex 0096)

This read/write register resets the channel, enables the '-card setup' signal, and configures the connectors.

Bit	Function
7	Channel reset
6–4	Reserved
3	Enable card setup
2–0	Channel select 2–0

Figure 2-19. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When this bit is set to 1, it activates the 'channel reset' signal to all connectors.

Bits 6–4 These bits are reserved and must be set to 0.

Bit 3 When this bit is set to 1, the '-card setup' signal that is selected by bits 2 through 0 is enabled.

Bits 2–0 These bits are the address bits for the '-card setup' signal to the connectors. Connectors 1 through 5 are addressed as 0 through 4. When bit 3 is set to 1, these bits select the connector or function for setup cycles.

Each channel connector has a unique '-card setup' signal (-CD SETUP) associated with it. This signal is used to select the adapters for setup cycles, allowing access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Note: -CD SETUP goes active only when an operation is performed in the I/O address range hex 0100 through 0107.

Section 3. System Board

Description 3-3
Microprocessor and Math Coprocessor 3-3
Micro Channel Architecture Implementation 3-3
  The Central Arbiter 3-3
  Arbitration Bus Priority Assignments 3-4
  Central Arbiter Programming 3-5
The Bus Extension 3-6
Diskette Drive Connectors 3-7
System Board Memory Connectors 3-8
SCSI-Device Connector 3-9
Memory 3-10
  ROM Subsystem 3-11
  RAM Subsystem 3-11
  Memory Subsystem Control 3-12
  Memory-Presence Determination 3-12
  Cached Memory Address Space 3-13
  RT/CMOS RAM 3-16
    RT/CMOS Address and NMI Mask Register (Hex 0070) . . 3-16
    RT/CMOS Data Register (Hex 0071) 3-17
    RT/CMOS RAM I/O Operations 3-17
    Real-Time Clock Bytes (Hex 000–00D) 3-18
    CMOS RAM Configuration 3-21
Miscellaneous System Functions and Ports 3-25
  Nonmaskable Interrupt 3-25
  System Control Port B (Hex 0061) 3-26
  System Control Port A (Hex 0092) 3-27
  Power-On Password 3-28
  Selectable Boot Sequence 3-29
Hardware Compatibility 3-29
Error Codes 3-30

© Copyright IBM Corp. 1992

Notes:

Description

This section describes the microprocessors, math coprocessor, channel differences, memory subsystems, and miscellaneous system ports, and connectors on the Model 76 system board. Additional information about these topics can be found in the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces.*

Microprocessor and Math Coprocessor

The Intel** 80486SX microprocessor in the Model 76 runs at 25 MHz or 33 MHz. It has a 32-bit address interface and a 32-bit data interface and is software-compatible with the 80386SX and 80386DX microprocessors. The Model 76 also supports the Intel 80486DX2 microprocessor, which runs at 25 MHz (system speed)/50 MHz (microprocessor speed) or 33 MHz (system speed)/66 MHz (microprocessor speed).

The 80487SX math coprocessor is matched to the speed of the system microprocessor and operates in synchronous mode. The 80487SX math coprocessor is software-compatible with the 80387DX math coprocessor.

Micro Channel Architecture Implementation

This section describes the implementation of the Micro Channel architecture in Model 76 systems. For general information about Micro Channel architecture, refer to the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures.*

The Central Arbiter

The central arbitration control point gives programmable subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. The central arbiter supports up to 15 arbitrating devices (levels hex 0 through E) and the system microprocessor (level hex F).

** Trademark of Intel Corporation.

Note: The system board small computer system interface (SCSI) controller performs cycles at arbitration level hex F if the Micro Channel arbitration level is F when the SCSI controller requests the bus.

Arbitration Bus Priority Assignments

The following figure shows the assignment of arbitration levels. The functions with the *lowest* arbitration level have the *highest* priority.

Arb. Level	Primary Assignment
-2	Memory refresh
-1	NMI
0	DMA channel 0 (programmable to any arbitration level)
1	DMA channel 1
2	DMA channel 2
3	DMA channel 3
4	DMA channel 4 (programmable to any arbitration level)
5	DMA channel 5
6	DMA channel 6
7	DMA channel 7
8–E	Available
F	System microprocessor

Figure 3-1. Arbitration Bus Priority Assignments

Note: Devices that are designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so that diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, which is normally on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation and by the previous controlling master. To prevent overruns, the diskette drive controller should not be held inactive for more than 12 microseconds.

Nonmaskable interrupt (NMI) service is executed at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal (ARB/-GNT) is in the arbitration state.

When the central arbitration control point receives a level -1 request (NMI, a system board internal signal), it activates -PREEMPT, waits for the end of the transfer, and then places ARB/-GNT into the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level -1 request

and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following figures.

Bit	Function
7	Enable system microprocessor cycle
6	Arbitration mask
5	Enable extended arbitration (not supported)
4–0	Reserved

Figure 3-2. Arbitration Register (Hex 0090)—Write

Bit	Function
7	Enable system microprocessor cycle
6	Arbitration masked by NMI
5	Bus time-out
4	Reserved
3–0	Value of arbitration bus during previous grant state

Figure 3-3. Arbitration Register (Hex 0090)—Read

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. The power-on self-test (POST) sets this bit to 1.

Reading this bit as a 1 indicates that the system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 enables extended arbitration. The minimum arbitration cycle is 300 nanoseconds; this bit extends that minimum to 600 nanoseconds. POST sets this bit to 0.

Reading this bit as a 1 indicates that a bus time-out has occurred and resets bit 6 in this register to 0.

Bit 4 This bit is reserved and must be set to 0.

Bits 3–0 These bits are undefined for a write operation and must be set to 0.

Reading these bits returns the arbitration level of the arbiter that controlled the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

The Bus Extension

The Model 76 system uses a bus extension that provides three channel connectors:

- One 32-bit connector with matched memory
- One 32-bit connector with auxiliary-video extension
- One 32-bit connector with base-video extension

The adapters are installed horizontally into the bus extension.

Diskette Drive Connectors

The diskette drive cable connects to the system board and provides three 2- by 17-pin connectors for attaching internal diskette drives. Each connector passes control and data signals between the diskette drive controller on the system board and the drives. It also provides the power to each drive.

The following figure shows the signal assignments and pin numbers for the diskette drive connectors.

Pin	Signal	Pin	Signal
1	Ground	2	Data rate select 1
3	+5 V dc	4	Drive type ID 1
5	Ground	6	+12 V dc
7	Ground	8	-Index
9	Drive type ID 0	10	Reserved
11	Ground	12	-Drive select
13	Ground	14	Reserved
15	Ground	16	-Motor enable
17	Media type ID 1	18	-Direction in
19	Ground	20	-Step
21	Ground	22	-Write data
23	Ground	24	-Write enable
25	Ground	26	-Track 0
27	Media type ID 0	28	-Write protect
29	Ground	30	-Read data
31	Ground	32	-Head 1 select
33	Data rate select 0	34	-Diskette change

Figure 3-4. Diskette Drive Connectors

System Board Memory Connectors

The Model 76 system board has four 72-pin connectors for installing memory modules. The following figure shows the pin assignments for the 1- by 72-pin memory connector. Refer to "Memory-Presence Determination" on page 3-12 for decoding of the 'presence detect' and '-ECC memory' signals.

Pin	Signal	Pin	Signal
1	Ground	37	Parity data 1
2	Data 0	38	Parity data 3
3	Data 16	39	Ground
4	Data 1	40	Column address strobe 0
5	Data 17	41	Column address strobe 2
6	Data 2	42	Column address strobe 3
7	Data 18	43	Column address strobe 1
8	Data 3	44	Row address strobe 0
9	Data 19	45	Row address strobe 1
10	+5 V dc	46	Block select 1
11	-Column address strobe P	47	Write enable
12	Address 0	48	Reserved
13	Address 1	49	Data 8
14	Address 2	50	Data 24
15	Address 3	51	Data 9
16	Address 4	52	Data 25
17	Address 5	53	Data 10
18	Address 6	54	Data 26
19	Reserved	55	Data 11
20	Data 4	56	Data 27
21	Data 20	57	Data 12
22	Data 5	58	Data 28
23	Data 21	59	+5 V dc
24	Data 6	60	Data 29
25	Data 22	61	Data 13
26	Data 7	62	Data 30
27	Data 23	63	Data 14
28	Address 7	64	Data 31
29	Block select 0	65	Data 15
30	+5 V dc	66	Block select 2
31	Address 8	67	Presence detect 0
32	Address 9	68	Presence detect 1
33	Row address strobe 3	69	Presence detect 2
34	Row address strobe 2	70	Presence detect 3
35	Parity data 2	71	Block select 3
36	Parity data 0	72	Ground

Figure 3-5. System Board Memory Connectors

SCSI-Device Connector

The system board provides two connectors for attaching SCSI devices: one internal connector with cable and one external connector.

The cable connects to the system board and provides two 2- by 25-pin connectors for attaching internal SCSI devices. The system board has one 2- by 30-pin connector for attaching external SCSI devices.

The following figure shows the pin assignments for the internal 2- by 25-pin SCSI connector.

Pin	Signal	Pin	Signal
1	Ground	26	+Terminal power
2	Data 0	27	Ground
3	Ground	28	Ground
4	Data 1	29	Ground
5	Ground	30	Ground
6	Data 2	31	Ground
7	Ground	32	-Attention
8	Data 3	33	Ground
9	Ground	34	Ground
10	Data 4	35	Ground
11	Ground	36	-Busy
12	Data 5	37	Ground
13	Ground	38	-Acknowledge
14	Data 6	39	Ground
15	Ground	40	-Reset
16	Data 7	41	Ground
17	Ground	42	-Message
18	Data P	43	Ground
19	Ground	44	-Select
20	Ground	45	Ground
21	Ground	46	-Control/data
22	Ground	47	Ground
23	Ground	48	-Request
24	Ground	49	Ground
25	Not connected	50	-Input/output

Figure 3-6. Internal SCSI-Device Connector Pin Assignments

The following figure shows the pin assignments for the 2- by 30-pin external SCSI connector.

Pin	Signal	Pin	Signal
1	Ground	31	Ground
2	Data 0	32	-Attention
3	Ground	33	Ground
4	Data 1	34	Ground
5	Ground	35	Ground
6	Data 2	36	-Busy
7	Ground	37	Ground
8	Data 3	38	-Acknowledge
9	Ground	39	Ground
10	Data 4	40	-Reset
11	Ground	41	Ground
12	Data 5	42	-Message
13	Ground	43	Ground
14	Data 6	44	-Select
15	Ground	45	Ground
16	Data 7	46	-Control/data
17	Ground	47	Ground
18	Data P	48	-Request
19	Ground	49	Ground
20	Ground	50	-Input/output
21	Ground	51	Ground
22	Ground	52	Reserved
23	Ground	53	Reserved
24	Ground	54	Reserved
25	Not connected	55	Reserved
26	+Terminal power	56	Reserved
27	Ground	57	Reserved
28	Ground	58	Reserved
29	Ground	59	Reserved
30	Ground	60	Reserved

Figure 3-7. External SCSI-Device Connector Pin Assignments

Memory

The Model 76 uses the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- Real-time clock and CMOS RAM (RT/CMOS RAM)
- Nonvolatile random access memory (NVRAM)

ROM Subsystem

The ROM subsystem consists of 128KB of physical memory. Mapped ROM is active at power-on time and is assigned to the top of the first and last 1MB of address space (hex 0E0000 to 0FFFFF and hex FE0000 to FFFFFF). After POST ensures that system memory is operating properly, the ROM code is copied to RAM at the same address space, and ROM is disabled.

Access to ROM or RAM at address space hex 0E0000 to 0FFFFF is controlled by the ROM-enable bit in the Memory-Controller Configuration register. When ROM is enabled, it is not parity-checked.

RAM Subsystem

The RAM subsystem on the system board starts at address hex 000000 of the address space. The RAM subsystem is 72 bits wide: 64 data bits and 8 parity bits. One parity bit is generated for each byte of data that is written. During a read operation, one parity bit is checked for each byte of data that is read by the device controlling the bus.

Three memory connectors are provided on the system board. Each connector can support 2MB, 4MB, or 8MB of 70-nanosecond memory.

The system enables and disables memory in 1MB blocks for 2MB memory modules, or 4MB blocks for 4MB or 8MB memory modules. Each 1MB block must start on a 1MB boundary. Because 128KB of I/O ROM, 128KB of system board ROM, and 128KB of video memory are mapped within the first 1MB of address space, the first physical 1MB of RAM cannot be mapped to contiguous addresses and is split at the 640KB boundary, creating a 384KB overflow. The high 128KB of the overflow is mapped to the system board ROM address space; the remaining 256KB, called the *split memory block*, is either reserved for system use or mapped to the first available address following the last full 1MB of activated system board memory. Split-memory-block remapping and disabling are controlled by the Memory-Controller Configuration register. The presence of the split memory block in the memory address space might be affected by nonsystem memory.

Memory Subsystem Control

Memory on the system board is parity-checked random access memory that can be interleaved or noninterleaved. To operate in the interleaved mode, the memory must be paired in connectors 1 and 2, or 3 and 4 (for memory connector information, see "System Board Memory Connectors" on page 3-8). The memory controller automatically interleaves memory between the even and odd banks. If more memory is in one bank than in the other, the difference is used as noninterleaved memory. For example, if 2MB is installed in connector 2 and 4MB is installed in connector 1, the 2MB in connector 2 is interleaved with 2MB of the 4MB in connector 1. The remaining 2MB in connector 1 is noninterleaved.

When operating in the interleaved mode, the microprocessor can perform burst cycles with two-way interleaved accesses. This allows the microprocessor to perform zero-wait-state transfers for alternating 32-bit transfers in the burst cycle.

Memory-Presence Determination

The presence-detect signals are used by the system to determine the size and speed of memory on the memory module. The pins are either not connected (1) or connected to ground (0).

A set of 4 bits shows the state of all presence-detect signals for a specific memory connector; the bit is set to 0 when the signal is connected to ground. The following figure shows the information that is indicated by these bits, as well as the bank size of the memory module. Combinations that are not shown are reserved.

Presence Detect 3 2 1 0	Single Inline Memory Module Definition	Bank Size
1 1 0 0	2MB 70-ns memory	1MB
0 1 0 0	4MB 70-ns memory	4MB
1 0 1 1	8MB 70-ns memory	4MB

Figure 3-8. Presence-Detect Bits

Cached Memory Address Space

The following memory maps show the memory addresses that can be cached; only system board memory can be cached. The Model 76 address space contains three cacheable regions:

- Region 1: Memory addresses from 0 to 1MB
- Region 2: Memory addresses from 1MB to 16MB
- Region 3: Memory addresses from 16MB to 40MB plus 256KB of split memory

All system board memory in regions 2 and 3 is cacheable. The Programmable Boundary register for region 2 controls the upper boundaries of the memory space that is to be cached. Region 3 has a fixed cacheable boundary at 2GB (GB equals 1073741824 bytes).

The Set Configuration utility program might assign nonsystem memory to these cached regions, depending on the system configuration. POST establishes these cached regions, and they must not be altered.

Nonsystem memory can be located as follows:

- Region 1: Between memory addresses hex 0C0000 and 0DFFFF
- Region 2: Memory addresses from 16MB down to system memory
- Region 3: Memory addresses from 4GB down to 2GB of system memory

Note: If nonsystem memory is present between 16MB and 2GB, the system disables the processor cache during POST, and system performance is reduced.

The following memory map shows the cached areas of system memory, with no nonsystem memory allocation outside of region 1.

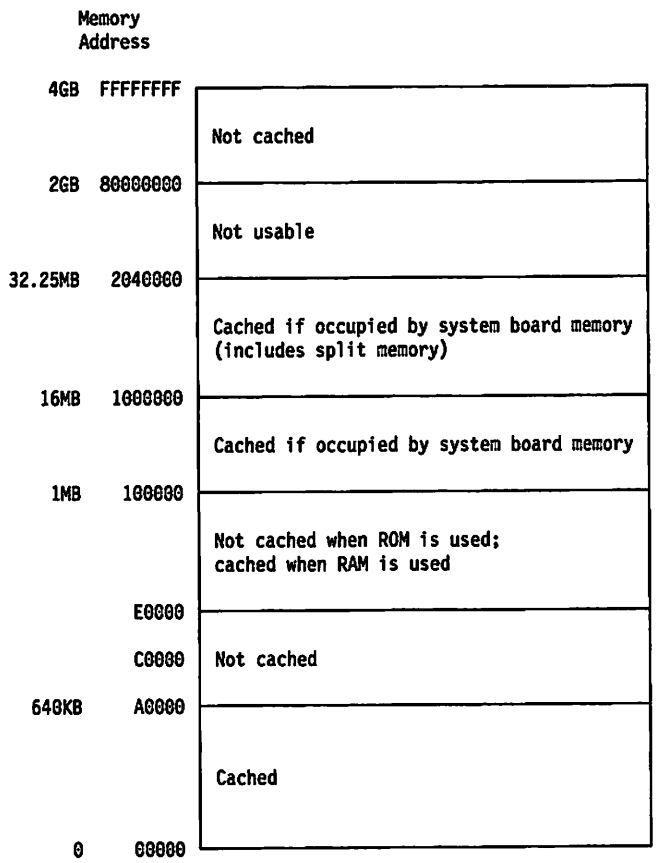


Figure 3-9. Memory Map, Cached Regions—System Memory

The following memory map shows the cached areas with 8MB of nonsystem memory present at 8MB to 16MB.

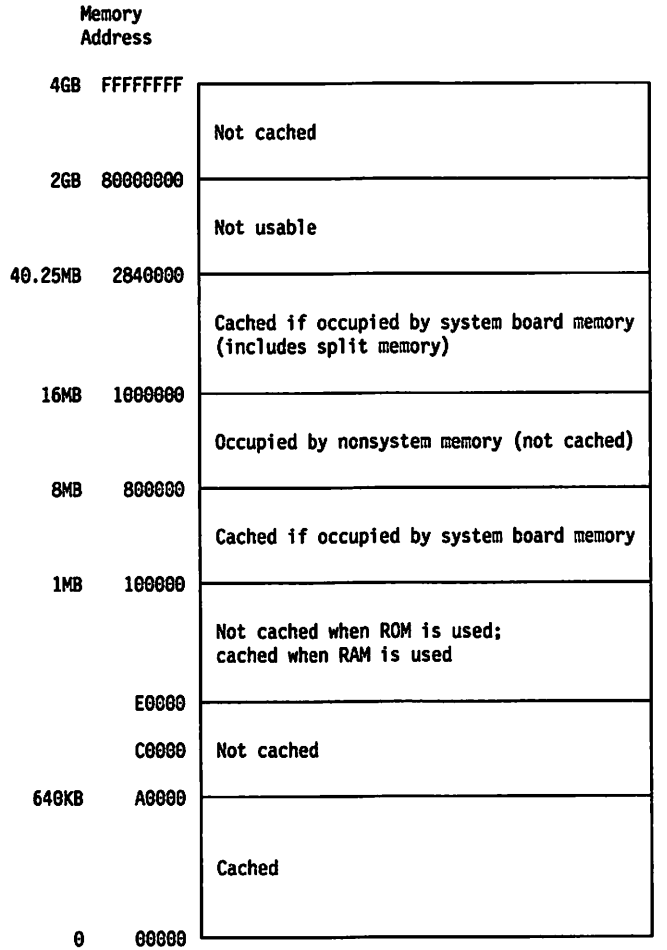


Figure 3-10. Memory Map, Cached Regions—Nonsystem Memory from 8MB to 16MB

RT/CMOS RAM

The RT/CMOS RAM (real-time clock/complementary metal-oxide semiconductor RAM) module contains the real-time clock and 64 bytes of CMOS RAM. The clock uses 14 bytes of this memory, and the rest is allocated to configuration and system-status information. A battery keeps the RT/CMOS RAM active when the power supply is off.

The system board has an additional 8KB CMOS RAM extension that is used to store configuration and other system information. This RAM extension is kept active by the battery.

The following figure shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000–00D	Real-Time Clock bytes
00E	Diagnostic Status byte
00F	Shutdown Status byte
010	Diskette Drive Type byte
011	Fixed Disk Drive Type byte
012	Reserved
013	Reserved
014	Equipment byte
015, 016	Low and high Base Memory bytes
017, 018	Low and high Expansion Memory bytes
019–031	Reserved
032, 033	Configuration CRC bytes
034	Reserved
035, 036	Low and high usable memory above 1MB
037	Date-Century byte
038–03F	Reserved

Figure 3-11. RT/CMOS RAM Address Map

RT/CMOS Address and NMI Mask Register (Hex 0070)

This register is used with the RT/CMOS Data register (hex 0071) to read from and write to the RT/CMOS RAM bytes.

Warning: The operation that follows a write operation to this register must access address hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS can occur.

Bit	Function
7	NMI mask
6	Reserved
5–0	RT/CMOS RAM address

Figure 3-12. RT/CMOS Address and NMI Mask Register (Hex 0070)

Bit 7 When this write-only bit is set to 1, the NMI is masked (disabled). This bit is set to 1 by a power-on reset.

Bit 6 This bit is reserved.

Bits 5–0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This register is used with the RT/CMOS Address and NMI Mask register to read from and write to the RT/CMOS RAM bytes.

Bit	Function
7–0	RT/CMOS data

Figure 3-13. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts must be masked to prevent other interrupt routines from changing the CMOS Address register before data is read or written.

Warning: The operation that follows a write operation to hex 0070 must access address hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Writing to RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS Address and NMI Mask register (hex 0070).
2. Write the data to address hex 0071.
3. Write the address hex 0F to the RT/CMOS Address and NMI Mask register; this leaves address hex 0070 pointing to the Shutdown Status byte (hex 0F).
4. Read from address hex 0071 to restore the RT/CMOS (see the warning above).

Reading from RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS Address and NMI Mask register (hex 0070).
2. Read the data from address hex 0071.
3. Write the address hex 0F to the RT/CMOS Address and NMI Mask register; this leaves address hex 0070 pointing to the Shutdown Status byte (hex 0F).
4. Read from address hex 0071 to restore the RT/CMOS.

Real-Time Clock Bytes (Hex 000 – 00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following figure.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second alarm	1
002	Minutes	2
003	Minute alarm	3
004	Hours	4
005	Hour alarm	5
006	Day of week	6
007	Date of month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-14. Real-Time Clock Bytes (Hex 000 – 00D)

Note: The system initializes Status Registers A and B when the time and date are set. Interrupt 1AH is the BIOS interface that is used to read and set the time and date; it initializes the registers in the same way that the system does.

Status Register A (Hex 00A)

Bit	Function
7	Update in progress
6 – 4	22-stage divider
3 – 0	Rate-selection bits

Figure 3-15. Status Register A (Hex 00A)

Bit 7 When this bit is set to 1, it indicates that the time-update cycle is in progress. When it is set to 0, it indicates that the current date and time can be read.

Bits 6–4 These bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768-kHz time base. This is the only value that is supported by the system for proper timekeeping.

Bits 3–0 These bits allow the selection of a divider output frequency. The system initializes the rate-selection bits to binary 0110, which selects a 1.024-kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Enable periodic interrupt
5	Enable alarm interrupt
4	Enable update-ended interrupt
3	Enable square-wave frequency
2	Date mode
1	24-hour mode
0	Enable daylight-saving-time mode

Figure 3-16. Status Register B (Hex 00B)

Bit 7 When this bit is set to 0, the cycle is updated by advancing the counts at a rate of one per second. When this bit is set to 1, any update cycle in progress ends immediately, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This is a read/write bit that enables an interrupt to occur at a rate that is specified by the rate and divider bits in Status Register A. When this bit is set to 1, the interrupt is enabled. The system initializes this bit to 0.

Bit 5 When this bit is set to 1, the alarm interrupt is enabled. The system initializes this bit to 0.

Bit 4 When this bit is set to 1, the update-ended interrupt is enabled. The system initializes this bit to 0.

Bit 3 When this bit is set to 1, the square-wave frequency is enabled as specified by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit is used to specify whether the binary-coded-decimal (BCD) or binary format is used for time-and-date calendar updates. When this bit is set to 1, it indicates the binary format. The system initializes this bit to 0.

Bit 1 This bit is used to specify whether the Hours byte is in 12-hour or 24-hour mode. When this bit is set to 1, it indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When this bit is set to 1, the daylight-saving-time mode is enabled. When this bit is set to 0, the daylight-saving-time mode is disabled, and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt-request flag
6	Periodic-interrupt flag
5	Alarm-interrupt flag
4	Update-ended interrupt flag
3–0	Reserved

Figure 3-17. Status Register C (Hex 00C)

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 When this bit is set to 1, it indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When this bit is set to 1, it indicates that a periodic interrupt occurred.

Bit 5 When this bit is set to 1, it indicates that an alarm interrupt occurred.

Bit 4 When this bit is set to 1, it indicates that an update-ended interrupt occurred.

Bits 3–0 These bits are reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6–0	Reserved

Figure 3-18. Status Register D (Hex 00D)

Bit 7 This read-only bit monitors the internal battery. When this bit is set to 1, it indicates that the real-time clock has power. When it is set to 0, it indicates that the real-time clock has lost power and the data in CMOS RAM is no longer valid.

Bits 6–0 These bits are reserved.

CMOS RAM Configuration

The following shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-time clock power
6	Configuration record and checksum status
5	Incorrect configuration
4	Memory-size mismatch
3	Fixed disk controller/drive C initialization status
2	Time status indicator
1	Adapter configuration miscompare
0	Adapter ID time-out

Figure 3-19. Diagnostic Status Byte (Hex 00E)

Bit 7 When this bit is set to 1, it indicates that the real-time clock has lost power.

Bit 6 When this bit is set to 1, it indicates that a checksum is incorrect.

Bit 5 When this bit is set to 1, it indicates that the configuration information is incorrect.

Bit 4 When this bit is set to 1, it indicates that the memory size does not match the configuration information.

Bit 3 When this bit is set to 1, it indicates that the controller or fixed disk drive failed initialization.

Bit 2 When this bit is set to 1, it indicates that the time and date are invalid.

Bit 1 When this bit is set to 1, it indicates that the adapters do not match the configuration information.

Bit 0 When this bit is set to 1, it indicates that a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is used by POST and BIOS.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive that is installed.

Bit	Function
7–4	First diskette drive type
3–0	Second diskette drive type

Figure 3-20. Diskette Drive Type Byte (Hex 010)

Bits 7–4 These bits indicate the type of the first diskette drive.

Bits 7 6 5 4	Function
0 0 0 0	No drive present
0 0 0 1	5.25-inch, 360KB diskette drive
0 0 1 0	5.25-inch, 1.2MB diskette drive
0 0 1 1	3.5-inch, 720KB diskette drive
0 1 0 0	3.5-inch, 1.44MB diskette drive
0 1 1 0	3.5-inch, 2.88MB diskette drive

Note: Combinations that are not shown are reserved.

Figure 3-21. First Diskette Drive Type Bits

Bits 3–0 These bits indicate the type of the second diskette drive.

Bits 3 2 1 0	Function
0 0 0 0	No drive present
0 0 0 1	5.25-inch, 360KB diskette drive
0 0 1 0	5.25-inch, 1.2MB diskette drive
0 0 1 1	3.5-inch, 720KB diskette drive
0 1 0 0	3.5-inch, 1.44MB diskette drive
0 1 1 0	3.5-inch, 2.88MB diskette drive

Note: Combinations that are not shown are reserved.

Figure 3-22. Second Diskette Drive Type Bits

Fixed Disk Drive Type Byte (Hex 011): This byte defines the type of fixed disk drive that is installed. A value of hex 000 indicates that no fixed disk drive is installed. This byte is not used for SCSI fixed disk drives.

Note: For more information about fixed disk drives, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Reserved Bytes (Hex 012 and 013): These bytes are reserved.

Equipment Byte (Hex 014): This byte defines the basic equipment in the system for the power-on diagnostic tests.

Bit	Function
7, 6	Number of diskette drives, other than physical drive 0
5, 4	Display operating mode
3, 2	Reserved
1	Math-coprocessor presence
0	Diskette drive 0 presence

Figure 3-23. Equipment Byte (Hex 014)

Bits 7, 6 These bits indicate the number of diskette drives that are installed, other than drive 0.

Bits 7 6	Number of Diskette Drives
0 0	No other drive
0 1	One other drive
1 0	Two other drives
1 1	Reserved

Figure 3-24. Installed Diskette Drive Bits

Bits 5, 4 These bits indicate the operating mode of the display that is attached to the video port.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-column mode
1 0	80-column mode
1 1	Monochrome mode

Figure 3-25. Display Operating Mode Bits

Bits 3, 2 These bits are reserved.

Bit 1 When this bit is set to 1, it indicates that a math coprocessor is installed.

Bit 0 When this bit is set to 1, it indicates that physical diskette drive 0 is installed.

Low and High Base-Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address.

The value of these bytes indicates the number of 1KB blocks of base memory. For example, hex 0280 indicates 640KB of base memory. The low byte is hex 015; the high byte is hex 016.

Low and High Expansion-Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address.

The value of these bytes indicates the number of 1KB blocks of expansion memory. For example, hex 0800 indicates 2048KB of expansion memory. The low byte is hex 017; the high byte is hex 018.

Reserved Bytes (Hex 019—031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check (CRC) data for bytes hex 010 through 031 of the 64-byte CMOS RAM. The low byte is hex 033; the high byte is hex 032.

Reserved Byte (Hex 034): This byte is reserved.

Low and High Usable-Memory Bytes (Hex 035 and 036): These bytes define the total amount of contiguous memory from 1MB to 16MB.

The value of these bytes indicates the number of 1KB blocks of usable memory. For example, hex 0800 indicates 2408KB of

contiguous usable memory. The low byte is hex 035; the high byte is hex 036.

Date-Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the Interrupt 1AH section of the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 – 03F): These bytes are reserved.

Miscellaneous System Functions and Ports

This section contains information about nonmaskable interrupt, system control ports, power-on password, and selectable boot sequence.

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals to the system microprocessor that a parity error, a channel check, a system channel time-out, or a system watchdog time-out has occurred. The NMI (other than cache parity errors) stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts, and the IRET instruction restores the interrupt flag to the state it was in before the interrupt. A system reset causes a reset of the NMI.

NMI requests that are caused by channel checks and system board memory-parity errors are subject to mask control by the NMI-mask bit in the RT/CMOS Address and NMI Mask register. The watchdog timer, system channel time-out, and cache parity error are not masked by this bit. See "RT/CMOS Address and NMI Mask Register (Hex 0070)" on page 3-16. The power-on default of the NMI mask is 1 (NMI disabled). Before the NMI is enabled after a power-on reset, the parity-error and channel-check states are initialized by POST.

Warning: The operation that follows a write operation to this register must access address hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the write and read functions of this port are shown in the following figures.

Bit	Function
7	Reset timer 0 output latch (IRQ0)
6–4	Reserved
3	Enable channel check
2	Enable parity check
1	Enable speaker data
0	Timer 2 gate to speaker

Figure 3-26. System Control Port B (Hex 0061)—Write

Bit	Function
7	Parity check
6	Channel check
5	Timer 2 output
4	Toggles with each refresh request
3	Enable channel check
2	Enable parity check
1	Enable speaker data
0	Timer 2 gate to speaker

Figure 3-27. System Control Port B (Hex 0061)—Read

Bit 7 When this bit is set to 1 during a write operation, IRQ0 is reset. When this bit is read as a 1, it indicates that a parity check has occurred.

Bit 6 When this bit is read as a 1, it indicates that a channel check has occurred.

Bit 5 This bit reflects the state of the timer/counter 2 'output' signal.

Bit 4 This bit toggles for each refresh request.

Bit 3 When this bit is set to 0, channel check is enabled. It is set to 1 during a power-on reset.

Bit 2 When this bit is set to 0, parity check is enabled. It is set to 1 during a power-on reset.

Bit 1 When this bit is set to 1, speaker data is enabled.

Bit 0 When this bit is set to 1, the timer 2 gate is enabled.

System Control Port A (Hex 0092)

Bit	Function
7–5	Reserved
4	Watchdog-timer status
3	Security lock latch
2	Reserved
1	Alternative gate A20
0	Alternative hot reset

Figure 3-28. System Control Port A (Hex 0092)

Bits 7–5 These bits are reserved.

Bit 4 This read-only bit indicates the watchdog-timer status. When this bit is set to 1, a watchdog time-out has occurred. For more information about the watchdog timer, refer to the "System Timers" section of the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces.*

Bit 3 This bit provides the security lock for the secured area of RT/CMOS RAM. When this bit is set to 1, the 8-byte power-on password is electronically locked. After this bit is set by POST, it can be cleared only by turning the system off.

Bit 2 This bit is reserved.

Bit 1 This bit is ORed with bit 1 of the Keyboard Output port to enable the 'address 20' signal (A20). When both bits are set to 0, A20 is disabled and set to 0. This bit is set to 0 during POST. See the "Keyboard and Auxiliary Device Controller" section of the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces.*

Bit 0 This bit provides an alternative method of resetting the system microprocessor. This alternative method supports operating systems that require faster operation than was provided on the IBM Personal Computer AT*. Resetting the system microprocessor switches the microprocessor from the protected mode to the real-address mode. The alternative reset takes 13.4 microseconds.

---

* Trademark of the IBM Corporation.

This bit is set to 0 by either a system reset or a write operation. When a write operation changes this bit from 0 to 1, the alternative reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If this bit is set to 0, POST assumes that the system has just been powered-on. If this bit is set to 1, POST assumes that the microprocessor has been switched from the protected mode to the real mode.

When bit 0 is used to reset the system microprocessor to the real mode, the following procedure must be used:

1. Disable all maskable and nonmaskable interrupts.
2. Reset the system microprocessor by setting bit 0 to 1.
3. Issue a Halt instruction to the system microprocessor.
4. Reenable all maskable and nonmaskable interrupts.

If this procedure is not followed, the results will be unpredictable.

Note: Whenever possible, advanced BIOS (ABIOS) should be used as an interface to reset the system microprocessor to real mode. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for more information about ABIOS.

Power-On Password

Eight bytes of RT/CMOS RAM are reserved for the power-on password and the check character. The 8 bytes are initialized to hex 00. The microprocessor can access these bytes only during the power-on self-test (POST). After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by any program. During power-on password installation, the password, which is from 1 to 7 characters, is stored in the security space.

Installing the password is a function of a program on the System Partition of the hard disk. The power-on password does not appear on the screen when it is installed, changed, or removed. After the power-on password has been installed, it can be changed or removed only during POST.

The Model 76 also supports a keyboard password. See the "Keyboard and Auxiliary Device Controller" section in the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* for more information.

Selectable Boot Sequence

The selectable boot sequence allows the user to specify the order in which devices are searched when looking for the boot record of an operating system. Diskette drives, fixed disk drives, and remote program load (RPL) can be part of the search sequence. Changing the sequence for selectable boot affects the drive-letter assignment each time the system is reset (either a power-on reset or a soft reset).

The user selects the sequence by using a program on the System Partition of the hard disk. The selected sequence is stored in nonvolatile RAM (NVRAM). After the system is reset, it searches, in the specified sequence, for a device that contains a boot record.

After the operating system is booted, the drive lettering is determined by where the boot record was found and by the search sequence.

Note: Selectable boot sequence affects adapters that use initialization programs. See the "Setup" section of the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures* for more details.

Hardware Compatibility

The Model 76 maintains many of the interfaces that are used by earlier PS/2 products. In most cases, the command and status organization of these interfaces is maintained.

The functional interfaces for the Model 76 are compatible with the following interfaces:

- The Intel 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timer, driven at 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller-address/transfer counters, page registers and status fields only. The Command and Request registers and the Rotate and Mask functions are not supported. The Mode register is partially supported.

- The National Semiconductor** NS16450 serial communication controller.
- The Intel 8088, 8086, 80286, and 80386 microprocessors.
- The Intel 8272 diskette drive controller.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The keyboard interface at address hex 0060.
- Display modes that are supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in DOS mode.
- Generally compatible with the Intel 80387, 80287, and 8087 math coprocessors.

Error Codes

POST returns a message in the form of a multiple-character code to indicate the type of test that failed. Two formats are used for these error messages:

- A 12-character code for all errors that *are* related to SCSI devices:
  - The first 4 characters identify the device type.
  - The next 8 characters identify specifics of the error.
- An 8-character error code for all errors that *are not* related to SCSI devices.

The 8-character error code consists of two 4-character elements: the major error code and the minor error code. The following figure lists the failures and their associated error codes.

** National Semiconductor is a trademark of the National Semiconductor Corporation, and Motorola is a trademark of Motorola, Incorporated.

Major Code	Minor Code	Description
0001		System bus errors—system board or microprocessor
	0100	Unexpected interrupt
	0200	Timer failure
	0300	Timer-interrupt failure
	0400	Protected-mode failure
	0500	Last keyboard command not accepted
	0600	Converting logic test
	0700	NMI test failed
	0800	Timer bus test failed
	0900	Low MB chip-select test failed
	10*xx*	System board memory-parity error
	11*xx*	I/O channel check error
	1200	Watchdog time-out
	1300	Micro Channel-related bus time-out
	1400	Adapter ROM checksum error
	1500	ROM checksum error or DMA error
	1600	System board port read/write failure
	1800	System board parity or L2-cache error during previous power-on
	1900	Down-level diskette controller (2.88MB diskette drive not supported)
	2000	Microprocessor test error
	6000	System board ID not recognized
	6100	Dead battery
	6300	Clock not updating
	6400	Memory configuration error
	6500	Adapter ID mismatch
	6600	Adapter busy error
	6700	Clock not updating
	6900	Microprocessor configuration error
	7100	Rolling bit test failure on CMOS Shutdown Address byte
	7200	Rolling bit test failure on NVRAM Diagnostic byte
	7300	Bad CMOS/NVRAM checksum
	7400	Bad configuration
	7900	NVRAM error log full
0002		Memory errors
	0*xxx*	Memory error
	1*xxx*	Irrecoverable error in first 1MB
	2100	ROM-to-RAM remapping error
	25*xx*	Unsupported memory type installed or memory-pair mismatch
	3500	Stuck data line on memory module, microprocessor or system board

Figure 3-29 (Part 1 of 2). POST Error Messages

Major Code	Minor Code	Description
0003		Keyboard errors
	0100	Keyboard error
	0200	Keyboard locked
	0300	Keyboard-to-system-board interface error
	0400	Keyboard clock high
	0500	No keyboard +5 V dc
0006		Diskette drive errors
	0100	Diskette drive or controller error
	0200	Diskette IPL boot record not valid
	0400	Non-media sense
0011	0100	Async error
0017		Fixed disk drive errors
	8000	Fixed disk drive 0 failed
	8100	Fixed disk drive 1 failed
	8200	Disk controller error
	9000	Fixed disk drive 0 error
	9100	Fixed disk drive 1 error
0024	0100	System board video error
0086		Mouse errors
	0100	System-bus error—keyboard/pointing-device interface
	0200	Pointing-device error
	0300	Pointing-device or system-bus error
0096	*xxxx*	SCSI-adapter (with cache) failure
0112	*xxxx*	SCSI-adapter (without cache) failure
0208 to 0241	*xxxx*	SCSI-device test failure
I999		Special instruction codes
	00*xx*	Initial machine load (IML) error
	03*xx*	No boot device
	04*xx*	IML-to-system mismatch
	06*xx*	IML error

Figure 3-29 (Part 2 of 2). POST Error Messages

Index

Numerics

80486DX2 microprocessor 1-9, 1-10, 3-3
80486SX microprocessor 1-9, 1-10, 3-3
80487SX math coprocessor 3-3

A

A20 3-27
acoustical noise emission values 1-12
adapter
  bus extension 3-6
  enable/setup register 2-15
  setup 2-4
address 20 gate 3-27
address and NMI mask register, RT/CMOS 3-16
address map
  memory 3-13
  POS I/O 2-5
  RT/CMOS RAM 3-16
  system board I/O 1-6
alarm interrupt 3-19, 3-20
alternative reset 3-27
altitude 1-11
ARB/-GNT 3-4
arbiter programming 3-5
arbitration control point, central 3-5
arbitration levels 3-4
arbitration register 3-5
arbitration, extended 3-6
audio subsystem 1-4
auxiliary-device controller 1-5

B

base-memory bytes 3-24
battery 3-21
boot sequence, selectable 3-29
bus contention 2-3
bus extension 3-6
bus priority assignments 3-4

C

cables 1-11
cache map 3-13
cacheable memory 3-13
card selected feedback register 2-6
-CD SETUP 2-15
-CD SFDBK 2-6
central arbitration control point 3-5
channel 3-3
  check enable 3-26
  check latch 3-26
  connector 3-6
  DMA 3-4
channel checks, synchronous 1-8
clock speed 1-3
clock, real-time 3-16, 3-18
CMOS RAM 1-4, 3-16—3-25
compatibility, hardware 3-29
compatibility, Micro Channel 1-8
configuration
  CRC bytes 3-24
  incorrect information 3-21
  RT/CMOS 3-21
connector
  channel 3-6
  diskette drive 3-7
  memory 3-8
  Micro Channel 1-5
  power supply 1-14
  SCSI device 3-9
contention, bus 2-3
control ports, system 3-26—3-27
controller
  diskette drive 1-5
  DMA 1-4
  interrupt 1-4

© Copyright IBM Corp. 1992

controller *(continued)*
keyboard and auxiliary device 1-5
parallel 1-5
parallel port, arbitration level 2-11
SCSI 1-5
serial 1-5
coprocessor, math 1-5, 3-3, 3-24
current, electrical 1-11
currents, maximum load 1-13
cyclic-redundancy-check (CRC) bytes 3-24

D

data parity 1-8
data register, RT/CMOS 3-17
date status indicator 3-22
date-century byte 3-25
depth, system unit 1-11
diagnostic status byte (RT/CMOS) 3-21
dimensions, system unit 1-11
diskette drive
arbitration level 2-11
connectors 3-7
controller 1-5
controller, control of 2-8
number installed 3-23
type byte 3-22
diskette overruns 3-4
display operating mode 3-24
divider output frequency 3-19
DMA
channels 3-4
controller 1-4
performance 1-9, 1-10
support 1-8

E

enable NMI 3-16
equipment byte 3-23
error codes, POST 3-30
expansion-memory bytes 3-24
extended arbitration 3-6

F

failures and messages, POST 3-30
fault, overvoltage 1-14
feedback, card selected 2-6
figures
adapter enable/setup register 2-15
arbitration bus priority assignments 3-4
arbitration register—read 3-5
arbitration register—write 3-5
card selected feedback register 2-6
channel load current 1-13
component maximum current 1-13
declared acoustical noise emission values 1-12
devices supported in setup mode 2-7
diagnostic status byte 3-21
diskette drive connectors 3-7
diskette drive type byte 3-22
display operating mode bits 3-24
equipment byte 3-23
external SCSI-device connector pin assignments 3-10
first diskette drive type bits 3-22
installed diskette drive bits 3-23
internal SCSI-device connector pin assignments 3-9
memory map, cached regions—nonsystem memory from 8MB to 16MB 3-15
memory map, cached regions—system memory 3-14
model and submodel bytes 1-3
performance specifications—25 MHz 1-9
performance specifications—33 MHz 1-10
physical specifications 1-11
POS I/O address map 2-5

figures *(continued)*
presence-detect bits 3-12
real-time clock bytes 3-18
RT/CMOS address and NMI mask register 3-17
RT/CMOS address map 3-16
RT/CMOS data register 3-17
second diskette drive type bits 3-23
status register A 3-18
status register B 3-19
status register c 3-20
status register D 3-21
system board devices and features 1-4
system board enable/setup register 2-7
system board group 1 POS register 3—write 2-9
system board group 1 POS register 3—write, index 00 2-10
system board group 1 POS register 3—write, index 01 2-10
system board group 1 POS register 3—write, index 04 2-10
system board group 1 POS register 4 2-11
system board group 1 POS register 5 2-11
system board group 2 POS register 2 2-12
system board group 2 POS register 3 2-12
system board group 3 POS register 2 2-13
system board group 3 POS register 3 2-13
system board I/O address map 1-6
system board memory connectors 3-8
system board POS register 2 2-8
system control port A 3-27
figures *(continued)*
system control port B—read 3-26
system control port B—write 3-26
voltage assignments for power-supply connectors 1-14
fixed disk drive
initialization failed 3-22
type byte 3-23
frequency, input 1-11

G

gate A20 3-27

H

heat output 1-11
height, system unit 1-11
humidity 1-11

I

I/O
address map 1-6
RT/CMOS RAM operations 3-17
input frequency 1-11
input voltage 1-11
interleaved memory 3-12
interrupt
alarm 3-19, 3-20
controller 1-4
IRQ0 reset 3-26
NMI reset 3-25
periodic 3-19, 3-20
update-ended 3-19, 3-20
IRQ0 3-26
IRQ3 2-12
IRQ4 2-12

K

keyboard
cable 1-11
password 3-29

M

math coprocessor 1-5, 3-3, 3-24
measurements, system unit 1-11
memory
  bytes 3-24
  cacheable 3-13
  CMOS RAM 1-4
  connectors 3-8
  control 3-12
  description 3-10
  interleaved 3-12
  noncacheable 3-13
  noninterleaved 3-12
  performance 1-9, 1-10
  presence determination 2-9, 3-12
  RAM 3-11
  RAM subsystem 1-4
  random access 3-11
  read operation 1-9, 1-10
  read-only 3-11
  refresh 3-4
  ROM 3-11
  ROM subsystem 1-4
  RT/CMOS RAM 3-16
  size miscompare 3-21
  write operation 1-9, 1-10
memory-presence detect signals 3-12
messages, POST error 3-30
Micro Channel architecture
  arbitration control point, central 3-5
  bus extension 3-6
  compatibility 1-8
  connectors 1-5
  general information 3-3
microprocessor
  80486DX2 3-3
  80486SX 3-3
  alternative reset 3-27
  burst cycles 3-12
  mode switch compatibility 3-27
  performance 1-9, 1-10
model byte 1-3

N

NMI mask register 3-16
NMI service 3-4
NMI signal 3-4
noise emission 1-12
noncacheable memory 3-13
noninterleaved memory 3-12
nonmaskable interrupt (NMI) 3-25

O

operating-system boot sequence 3-29
output protection, power supply 1-14
output voltage 1-13
output voltage sequencing 1-14
outputs, power supply 1-13
overvoltage fault 1-14

P

page hit 1-9, 1-10
page miss 1-9, 1-10
parallel controller port 1-5
parallel port 1-5
parallel port controller, arbitration level 2-11
parallel port select 2-8
parallel port, control of 2-8
parity check enable 3-26
password
  keyboard 3-29
  power-on 3-27, 3-28
performance, system 1-9, 1-10
periodic interrupt 3-19, 3-20
port
  parallel 1-5
  serial 1-5
POS
  See programmable option select (POS)
POST (power-on self-test) 3-11
POST error codes 3-30
power
  cable 1-11

power *(continued)*
loss 3-21
specifications 1-11
power supply, description 1-12
power-on password 3-27, 3-28
power-on self-test (POST) 3-11
power-supply connectors 1-14
power-supply output protection 1-14
power-supply outputs 1-13
-PREEMPT 3-4
presence determination, memory 2-9
programmable option select (POS)
adapter enable/setup 2-15
address map 2-5
card selected feedback register 2-6
description 2-3
diskette drive 2-11
group 1, register 2 2-8
group 1, register 3 2-9
group 1, register 4 2-11
group 1, register 5 2-11
group 2, register 2 2-12
group 2, register 3 2-12
group 3, register 2 2-13
group 3, register 3 2-13
I/O address map 2-5
memory information 2-9
parallel port controller 2-11
register groups 2-6
SCSI controller, enable 2-13
SCSI ID selection 2-13
setup procedures 2-4
system board enable/setup register 2-7
system board groups 2-4
system board serial port address 2-12
system board serial port, enable 2-12
system board setup 2-6
system configuration utility programs 2-3
warning 2-3
programming, arbiter 3-5
protected mode, switch from 3-27
protection, power supply 1-14

R

RAM (random access memory) 3-11
RAM subsystem 1-4
random access memory (RAM) 3-11
read-only memory (ROM) 3-11
real mode, switch to 3-27
real-time clock 3-16, 3-18, 3-21
refresh request 1-9, 1-10, 3-26
register
adapter enable/setup 2-15
arbitration 3-5
card selected feedback 2-6
group 1 POS register 2 2-8
group 1 POS register 3 2-9
group 1 POS register 4 2-11
group 1 POS register 5 2-11
group 2 POS register 2 2-12
group 2 POS register 3 2-12
group 3 POS register 2 2-13
group 3 POS register 3 2-13
miscellaneous system 3-25
RT/CMOS address and NMI mask 3-16
RT/CMOS data 3-17
RT/CMOS status 3-18—3-21
system board enable/setup 2-7
system board POS 2-5
system control port B 3-26
reserved, definition ix
reset, alternative 3-27
ROM (read-only memory) 3-11
ROM subsystem 1-4
RT/CMOS RAM
address and NMI mask register 3-16
address map 3-16
configuration bytes 3-21
data register 3-17
description 3-16
diagnostic status byte 3-21

RT/CMOS RAM *(continued)*
I/O operations 3-17
power-on password 3-28
reading from 3-18
secured area 3-27
status registers 3-18—3-21
writing to 3-17

S

SCSI controller 1-5
SCSI controller, enable 2-13
SCSI ID selection 2-13
SCSI-device connector 3-9
selectable boot sequence 3-29
selected feedback return 1-8
sequencing, output voltage 1-14
serial controller port 1-5
serial port 1-5
serial port address 2-12
serial port, enable 2-12
set configuration 3-29
setup
bus contention 2-3
POS procedures 2-4
system board 2-6
shutdown status byte 3-22
signal
address 20 3-27
arbitrate/-grant 3-4
audio sum node 1-4
-card selected feedback 2-6
-card setup 2-15
channel reset 2-15
-ECC memory 2-9, 3-8
NMI 3-4
output 3-26
-preempt 3-4
presence detect 0—3 2-9, 3-8, 3-12
selected feedback return 1-8
setup 2-4
size, system unit 1-11
speaker data enable 3-26
specifications
performance 1-9, 1-10
physical 1-11
speed, clock 1-3
square-wave frequency 3-20
startup sequence 3-29
status registers
(RT/CMOS) 3-18—3-21
streaming data 1-8
submodel byte 1-3
synchronous channel checks 1-8
system
clock speed 1-3
configuration utility programs 2-3
control ports 3-26—3-27
description 1-3
functions, miscellaneous 3-25
performance 1-9, 1-10
reset 3-25
specifications 1-11
timers 1-4
system board
address map 1-6
enable/setup register 2-7
group 1 POS register 2 2-8
group 1 POS register 4 2-11
group 1 POS register 5 2-11
group 2 POS register 2 2-12
group 2 POS register 3 2-12
group 3 POS register 2 2-13
group 3 POS register 3 2-13
memory connectors 3-8
POS I/O address map 2-5
SCSI controller, enable 2-13
SCSI ID selection 2-13
SCSI-device connector 3-9
serial port address 2-12
serial port, enable 2-12
setup 2-4, 2-6

T

temperature 1-11
time status indicator 3-22
time-and-date updates 3-20
time-base frequency 3-19
time-update cycle 3-19
timers, system 1-4

U

update-ended interrupt 3-19, 3-20
usable-memory bytes 3-24

V

video subsystem 1-5
voltage, input 1-11
voltage, output 1-13

W

warning
  central arbiter 3-5
  NMI 3-25
  POS 2-3
  reserved areas ix
  RT/CMOS 3-16
  RT/CMOS RAM I/O
    operations 3-17
watchdog-timer status 3-27
weight, system unit 1-11
width, system unit 1-11

X

XGA-2 video 1-5

Personal System/2
Model 77
Technical Reference

Note

Before using this information and the product it supports, be sure to read the general information under "Notices" on page vii.

First Edition (September 1992)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer of express or implied warranties in certain transactions, therefore, this statement may not apply to you.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Requests for technical information about IBM products should be made to your IBM Authorized Dealer or your IBM Marketing Representative.

© Copyright International Business Machines Corporation 1992. All rights reserved.
Note to U.S. Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Contents

Figures v

Notices vii
Trademarks and Service Marks vii

Preface ix

Section 1. System Overview 1-1
Description 1-3
System Board Devices and Features 1-4
System Board I/O Address Map 1-6
Micro Channel Compatibility 1-8
Specifications 1-9
Power Supply 1-12
Outputs 1-13
Output Protection 1-14
Voltage Sequencing 1-14
Power-Supply Connectors 1-14

Section 2. Programmable Option Select 2-1
Description 2-3
POS I/O Address Map 2-5
Card Selected Feedback Register (Hex 0091) 2-6
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-7
System Board Group 1 POS Register 2 (Hex 0102) 2-8
System Board Group 1 POS Register 3 (Hex 0103) 2-9
System Board Group 1 POS Register 4 (Hex 0104) 2-11
System Board Group 1 POS Register 5 (Hex 0105) 2-11
System Board Group 2 POS Register 2 (Hex 0102) 2-12
System Board Group 2 POS Register 3 (Hex 0103) 2-12
System Board Group 3 POS Register 2 (Hex 0102) 2-13
System Board Group 3 POS Register 3 (Hex 0103) 2-13
Adapter Enable/Setup Register (Hex 0096) 2-15

Section 3. System Board 3-1
Description 3-3
Microprocessor and Math Coprocessor 3-3
Micro Channel Architecture Implementation 3-3
The Central Arbiter 3-3
Arbitration Bus Priority Assignments 3-4
Central Arbiter Programming 3-5

© Copyright IBM Corp. 1992

The Bus Extension 3-6
Diskette Drive Connectors 3-7
System Board Memory Connectors 3-8
SCSI-Device Connector 3-9
Memory 3-10
ROM Subsystem 3-11
RAM Subsystem 3-11
Memory Subsystem Control 3-12
Memory-Presence Determination 3-12
Cached Memory Address Space 3-13
RT/CMOS RAM 3-16
Miscellaneous System Functions and Ports 3-25
Nonmaskable Interrupt 3-25
System Control Port B (Hex 0061) 3-26
System Control Port A (Hex 0092) 3-27
Power-On Password 3-28
Selectable Boot Sequence 3-29
Hardware Compatibility 3-29
Error Codes 3-30

Index X-1

Figures

1-1. Model and Submodel Bytes 1-3
1-2. System Board Devices and Features 1-4
1-3. System Board I/O Address Map 1-6
1-4. Performance Specifications—25 MHz 1-9
1-5. Performance Specifications—33 MHz 1-10
1-6. Physical Specifications 1-11
1-7. Declared Acoustical Noise Emission Values 1-12
1-8. Component Maximum Current 1-13
1-9. Channel Load Current 1-13
1-10. Voltage Assignments for the Internal Power-Supply Connectors 1-14
2-1. POS I/O Address Map 2-5
2-2. Card Selected Feedback Register (Hex 0091) 2-6
2-3. Devices Supported in Setup Mode 2-7
2-4. System Board Enable/Setup Register (Hex 0094) 2-7
2-5. System Board POS Register 2 (Hex 0102) 2-8
2-6. Parallel Port Select Bits 2-8
2-7. System Board Group 1 POS Register 3 (Hex 0103) 2-9
2-8. System Board POS Group 1 Register 3 (Hex 0103)—Index 00 2-10
2-9. System Board POS Group 1 Register 3 (Hex 0103)—Index 04 2-10
2-10. System Board POS Group 1 Register 3 (Hex 0103)—Index 01 2-10
2-11. System Board Group 1 POS Register 4 (Hex 0104) . . . 2-11
2-12. System Board Group 1 POS Register 5 (Hex 0105) . . . 2-11
2-13. System Board Group 2 POS Register 2 (Hex 0102) . . . 2-12
2-14. System Board Group 2 POS Register 3 (Hex 0103) . . . 2-12
2-15. Serial Port Addresses 2-12
2-16. System Board Group 3 POS Register 2 (Hex 0102) . . . 2-13
2-17. System Board Group 3 POS Register 3 (Hex 0103) . . . 2-13
2-18. System Board SCSI Controller ID 2-14
2-19. Adapter Enable/Setup Register (Hex 0096) 2-15
3-1. Arbitration Bus Priority Assignments 3-4
3-2. Arbitration Register (Hex 0090)—Write 3-5
3-3. Arbitration Register (Hex 0090)—Read 3-5
3-4. Diskette Drive Connectors 3-7
3-5. System Board Memory Connectors 3-8
3-6. Internal SCSI-Device Connector Pin Assignments 3-9
3-7. External SCSI-Device Connector Pin Assignments . . . 3-10
3-8. Presence-Detect Bits 3-12
3-9. Memory Map, Cached Regions—System Memory . . . 3-14

© Copyright IBM Corp. 1992

3-10. Memory Map, Cached Regions—Nonsystem Memory from 8MB to 16MB 3-15
3-11. RT/CMOS RAM Address Map 3-16
3-12. RT/CMOS Address and NMI Mask Register (Hex 0070) 3-17
3-13. RT/CMOS Data Register (Hex 0071) 3-17
3-14. Real-Time Clock Bytes (Hex 000—00D) 3-18
3-15. Status Register A (Hex 00A) 3-18
3-16. Status Register B (Hex 00B) 3-19
3-17. Status Register C (Hex 00C) 3-20
3-18. Status Register D (Hex 00D) 3-21
3-19. Diagnostic Status Byte (Hex 00E) 3-21
3-20. Diskette Drive Type Byte (Hex 010) 3-22
3-21. First Diskette Drive Type Bits 3-22
3-22. Second Diskette Drive Type Bits 3-22
3-23. Equipment Byte (Hex 014) 3-23
3-24. Installed Diskette Drive Bits 3-23
3-25. Display Operating Mode Bits 3-24
3-26. System Control Port B (Hex 0061)—Write 3-26
3-27. System Control Port B (Hex 0061)—Read 3-26
3-28. System Control Port A (Hex 0092) 3-27
3-29. POST Error Messages 3-31

Notices

References in this publication to IBM products, programs, or services do not imply that IBM intends to make these available in all countries in which IBM operates. Any reference to an IBM product, program or service is not intended to state or imply that only IBM's product, program, or service may be used. Any functionally equivalent product, program, or service that does not infringe any of IBM's intellectual property rights or other legally protectable rights may be used instead of the IBM product, program, or service. Evaluation and verification of operation in conjunction with other products, programs, or services, except those expressly designated by IBM, are the user's responsibility.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

Trademarks and Service Marks

The following terms, denoted by an asterisk (*) in this publication, are trademarks of the IBM Corporation in the United States and/or other countries:

IBM
Micro Channel
Personal Computer AT
Personal System/2
PS/2
Ultimedia
XGA

The following terms, denoted by a double asterisk (**) in this publication, are trademarks of other companies as follows:

Intel	Intel Corporation
Motorola	Motorola, Incorporated
National Semiconductor	National Semiconductor Corporation

© Copyright IBM Corp. 1992

Notes:

Preface

The Technical Reference library is intended for those who develop hardware and software products for IBM Personal Computers and IBM Personal System/2 products. Users should understand computer architecture and programming concepts.

This manual consists of the following sections:

Section 1, "System Overview," describes the system, features, and specifications.

Section 2, "Programmable Option Select," describes the registers that are used for configuration.

Section 3, "System Board," describes the system-specific hardware implementations of the Micro Channel architecture.

This technical reference should be used with the following publications. These publications contain additional information about many of the subjects that are discussed in this technical reference.

IBM Personal System/2 Hardware Interface Technical Reference—Architectures

IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference

M-Audio Capture and Playback Adapter Installation and Technical Reference Manual

Information about diskette drives, fixed disk drives, adapters, and external options are in separate option technical references.

Warning: The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

© Copyright IBM Corp. 1992

Notes:

Section 1. System Overview

Description 1-3
System Board Devices and Features 1-4
System Board I/O Address Map 1-6
Micro Channel Compatibility 1-8
Specifications 1-9
Power Supply 1-12
  Outputs 1-13
  Output Protection 1-14
  Voltage Sequencing 1-14
  Power-Supply Connectors 1-14

© Copyright IBM Corp. 1992

Notes:

Description

The IBM* Personal System/2* (PS/2*) Model 77 computer is a self-contained desktop computer system with a keyboard. It supports up to four internal direct access storage devices (DASD). Three of these devices can be removable-media DASD (such as diskette, tape, or optical), or three can be nonremovable-media DASD.

Programs determine the type of system board by reading the model and submodel bytes. Interrupt 15H, Return System Configuration Parameters function ((AH)=C0H) returns the model byte, submodel byte, and BIOS revision code.

The following figure lists the model and submodel bytes, microprocessor types, and system-clock speeds for the Model 77 system board.

Model Byte (Hex)	Submodel Byte (Hex)	Microprocessor	System Clock
F8	41	80486SX	25 MHz
F8	41	80486DX2	25 MHz/50 MHz
F8	41	80486SX	33 MHz
F8	41	80486DX2	33 MHz/66 MHz

Figure 1-1. Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems.

* Trademark of the IBM Corporation.

System Board Devices and Features

The following figure lists the system board devices and features. The *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* describes, by type number, the devices that are common to PS/2 products.

Device	Type	Features
Microprocessor	—	80486SX—25 MHz or 80486SX—33 MHz - 32-bit address interface, 32-bit data interface
System Timers	1	Channel 0—System timer Channel 2—Tone generation for speaker Channel 3—Watchdog timer
ROM Subsystem	—	128KB logical ROM (KB equals 1024 bytes)
RAM Subsystem	—	Four connectors (2MB to 32MB) (MB equals 1048576 bytes)
CMOS RAM Subsystem	—	64-byte CMOS RAM with real-time clock, calendar, 8KB CMOS RAM extension, and battery backup
Audio Subsystem	1	Driven by - System-timer channel 2 - The 'audio sum node' signal **In the PS/2 Ultimedia* Model M77:** M-Audio Capture and Playback Adapter† Multimedia front panel - Stereo headphone output - Monaural microphone input - Enhanced speaker
DMA Controller	1	Eight independent DMA channels Single or burst transfers with read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level sensitive

† For information about the M-Audio Capture and Playback Adapter, see the *M-Audio Capture and Playback Adapter Installation and Technical Reference Manual.*

Figure 1-2 (Part 1 of 2). System Board Devices and Features

* Trademark of the IBM Corporation.

Device	Type	Features
Video Subsystem	2	XGA*-2 video with 1MB video memory - Supports refresh rates up to 75 MHz - Supports direct color mode (65536 colors) - Contains XGA-2 Display Adapter/A
Keyboard/Auxiliary Device Controller	2	Keyboard connector Auxiliary-device connector Password security
Diskette Drive Controller	2	Supports: - 3.5-in. diskette drive (1.44MB and 2.88MB) - 5.25-in. diskette drive (360KB and 1.2MB)
CD-ROM (for Model M77)	—	CD-ROM-II† - 600MB capacity - Supports digital-audio, CD-ROM, and CD-XA formats - 330-ms average access time
Serial Controller Port	4	RS-232C interface - Two 9-pin connectors - Programmable as serial ports 1–16 - DMA, FIFO, and character modes
Parallel Controller Port	3	Programmable as parallel ports 1–4 - Supports bidirectional input and output - Supports DMA operation
SCSI Controller	1	Supports up to three internal SCSI devices Supports up to seven SCSI devices
Micro Channel* Connectors	—	Five connectors for Type 3 adapters - One 32-bit connector with base-video extension (contains XGA-2 Display Adapter/A) - One 32-bit connector with auxiliary-video extension - Three 32-bit connectors with matched-memory support
Math Coprocessor Socket	—	Supports 80487SX math coprocessor option with the same clock speed as the system microprocessor; supports microprocessor upgrades 80486DX2—25 MHz/50 MHz and 80486DX2—33 MHz/66 MHz

† For information about the M-Audio Capture and Playback Adapter, see the *M-Audio Capture and Playback Adapter Installation and Technical Reference Manual.*

Figure 1-2 (Part 2 of 2). System Board Devices and Features

* Trademark of the IBM Corporation.

System Board I/O Address Map

The following figure is the Model 77 system board I/O address map.

Address (Hex)	Device
0000–001F	DMA controller
0020, 0021	Interrupt controller
0040, 0042–0044, 0047	System timers
004B–004F	32-bit free-running timer
0060	Keyboard, auxiliary device
0061	System Control Port B
0064	Keyboard, auxiliary device
0066, 0067	Keyboard, auxiliary device
0070, 0071	RT/CMOS and NMI mask
0081–008F	DMA controller
0090	Central arbitration control point
0091	Card Selected Feedback register
0092	System Control Port A
0094	System Board Enable/Setup register
0096	Adapter Enable/Setup register
00A0, 00A1	Interrupt controller
00C0–00DF	DMA controller (4–7)
00E0–00E8	Memory controller
00F0–00FF	Math coprocessor
0100–0107	Programmable option select
0278–027D	Parallel port 3
02F8–02FF	Serial port 2
0378–037D	Parallel port 2
03B4, 03B5, 03BA	Video subsystem
03BC–03BF	Parallel port 1
03C0–03C5	Video subsystem
03C6–03C9	Video DAC
03CA, 03CC, 03CE, 03CF	Video subsystem
03D4, 03D5, 03DA	Video subsystem
03F0–03F7	Diskette drive controller
03F8–03FF	Serial port 1
1278–127D	Enhanced parallel port 1
1378–137D	Parallel port 4

Note: I/O addresses below hex 0100 that are not listed are reserved.

Figure 1-3 (Part 1 of 2). System Board I/O Address Map

Address (Hex)	Device
2100 – 210F	XGA video, instance 0
2110 – 211F	XGA video, instance 1
2120 – 212F	XGA video, instance 2
2130 – 213F	XGA video, instance 3
2140 – 214F	XGA video, instance 4
2150 – 215F	XGA video, instance 5
2160 – 216F	XGA video, instance 6
2170 – 217F	XGA video, instance 7
3220 – 3227	Serial port 3
3228 – 322F	Serial port 4
3540 – 3547	SCSI controller, instance 0
3548 – 354F	SCSI controller, instance 1
3550 – 3557	SCSI controller, instance 2
3558 – 355F	SCSI controller, instance 3
3560 – 3567	SCSI controller, instance 4
3568 – 356F	SCSI controller, instance 5
3570 – 3577	SCSI controller, instance 6
3578 – 357F	SCSI controller, instance 7
3A20 – 3A27	Serial port 9
3A28 – 3A2F	Serial port 10
3A30 – 3A37	Serial port 11
3A38 – 3A3F	Serial port 12
3A80 – 3A87	Serial port 13
3A88 – 3A8F	Serial port 14
3A90 – 3A97	Serial port 15
3A98 – 3A9F	Serial port 16
4220 – 4227	Serial port 5
4228 – 422F	Serial port 6
4620 – 462F	Serial port arbitration-level control
5220 – 5227	Serial port 7
5228 – 522F	Serial port 8
82F8 – 82FF	Enhanced serial port 2
83F8 – 83FF	Enhanced serial port 1
B220 – B227	Enhanced serial port 3
B228 – B22F	Enhanced serial port 4
BA20 – BA27	Enhanced serial port 9
BA28 – BA2F	Enhanced serial port 10
BA30 – BA37	Enhanced serial port 11
BA38 – BA3F	Enhanced serial port 12
BA80 – BA87	Enhanced serial port 13
BA88 – BA8F	Enhanced serial port 14
BA90 – BA97	Enhanced serial port 15
BA98 – BA9F	Enhanced serial port 16
C220 – C227	Enhanced serial port 5
C228 – C22F	Enhanced serial port 6
D220 – D227	Enhanced serial port 7
D228 – D22F	Enhanced serial port 8

Figure 1-3 (Part 2 of 2). System Board I/O Address Map

Micro Channel Compatibility

The following terms describe system limitations in the support of Micro Channel architecture.

Streaming Data

The system board supports 10-MHz streaming-data procedures involving data transfers between adapters; devices on the system board do not use streaming-data procedures. Data transfers default to the basic transfer procedure.

Data Parity

Data- and address-parity procedures are not supported in this system. Data transfers default to the basic transfer procedure.

Selected Feedback Return Signal

The system board supports the 'selected feedback return' signal, except for the I/O devices at addresses below hex 0100. These devices are controlled by the system master only and should not be accessed by bus masters.

Synchronous Channel Checks

Synchronous channel checks for errors other than Micro Channel data-parity errors are not supported in this system.

Synchronous channel checks for data-parity errors, which are typically issued by slaves, are the responsibility of the master that owned the channel and issued the access to the slave. However, in this system, these channel checks are detected by logic on the system board, resulting in a nonmaskable interrupt (NMI).

DMA

In this system, the DMA controller supports DMA slaves with 8-bit or 16-bit data widths.

Specifications

The following figure describes the performance specifications of the Model 77 running at 25 MHz.

Device	Cycle Time (ns)
Microprocessor (25 MHz, 40-ns clock)	
Access to system board RAM	
Memory read (internal cache miss)	
Page hit	280
Page miss	320/400
Memory write	
Page hit	120
Page miss	160/240
Access to channel	
Default transfer cycle	320
Synchronous transfer cycle	440
Refresh Rate (typically performed every 15.1 μs)	320
Bus-Master Access to System Board RAM	300 (min)
DMA Controller (10 MHz, 100-ns clock)	
Single transfer: 300 + (I/O access + memory access)	
Burst transfer: 300 + (I/O access + memory access)*n*†	
System board memory read	320 (min)
System board memory write	320 (min)
Access to channel	
Default transfer cycle	350 (min)
Synchronous transfer cycle	450 (min)

† *n* equals the number of data transfers in the burst.

Figure 1-4. Performance Specifications—25 MHz

The following figure describes the performance specifications of the Model 77. running at 33 MHz.

Device	Cycle Time (ns)
Microprocessor (33 MHz, 30-ns clock)	
Access to system board RAM	
Memory read (internal cache miss)	
Page hit	240
Page miss	270/330
Memory write	
Page hit	120
Page miss	150/210
Access to channel	
Default transfer cycle	300
Synchronous transfer cycle	420
Refresh Rate (typically performed every 15.1 μs)	400
Bus-Master Access to System Board RAM	300 (min)
DMA Controller (10 MHz, 100-ns clock)	
Single transfer: 300 + (I/O access + memory access)	
Burst transfer: 300 + (I/O access + memory access)*n*†	
System board memory read	300 (min)
System board memory write	300 (min)
Access to channel	
Default transfer cycle	300 (min)
Synchronous transfer cycle	420 (min)

† *n* equals the number of data transfers in the burst.

Figure 1-5. Performance Specifications—33 MHz

The following figure describes the physical specifications of the Model 77 and the Model M77.

Specification	Measurements
Size	
Width	440 mm (17.3 in.)
Depth	394 mm (15.5 in.)
Height	168 mm (6.6 in.)
Weight	
Minimum configuration	12.0 kg (26 lb)
Maximum configuration	15.9 kg (35 lb)
Cables	
Power cable	1.8 m (6 ft)
Keyboard cable	1.8 m (6 ft)
Air Temperature	
System on	
0 – 7000 ft altitude	10.0 to 35.0°C (50 to 95°F)
System off	10.0 to 43.0°C (50 to 110°F)
Humidity	
System on	8% to 85%
System off	5% to 85%
Maximum Altitude†	2133.6 m (7000 ft)
Heat Output	(300 watts) 1030 BTU per hour
Acoustical Readings	See Figure 1-7 on page 1-12
Electrical	
Input voltage (range is automatically selected; sinewave input is required)	
Low range	90 (min) – 137 (max) V ac
High range	180 (min) – 265 (max) V ac
Input frequency	50 Hz ± 3 Hz or 60 Hz ± 3 Hz
Maximum current draw	
Low range	4.6 A
High range	2.0 A
Input, in kilovolt-ampere (kVA)	
Minimum configuration (as shipped by IBM)	0.07 kVA
Maximum configuration	0.50 kVA
Electromagnetic Compatibility	FCC Class B

† This is the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.

Figure 1-6. Physical Specifications

The following figure contains the acoustical readings of the Model 77.

Description	L_{WAd} in bels Operate	Idle	L_{pAm} in dB Operate	Idle	$<L_{pA}>_m$ in dB Operate	Idle
Model 77	5.0	5.0	41	41	36	35

Notes:

L_{WAd}	The declared upper limit A-weighted sound power level for a random sample of machines
L_{pAm}	The mean value of the A-weighted sound pressure level at the operator position (if any) for a random sample of machines
$<L_{pA}>_m$	The mean value of the A-weighted sound pressure levels at the one-meter (bystander) positions for a random sample of machines

All measurements are made in accordance with ANSI standard S12.10 and are reported in conformance with ISO DIS 9296.

These measurements are preliminary data and are subject to change.

Figure 1-7. Declared Acoustical Noise Emission Values

Power Supply

The power supply converts the ac input voltage to three dc output voltages and provides power for the following:

- System board
- Micro Channel adapters
- Internal DASD drives
- Auxiliary devices
- Keyboard
- Multimedia control panel (for the Model M77 only)

The power switch and two light-emitting diodes (LED) are on the front of the system unit. When the green LED is lit, it indicates that the power supply is operating properly. The amber LED is the fixed-disk-activity indicator.

Outputs

The power supply provides separate voltage sources for the system board and the internal fixed disk drives. The system board voltages are +5 V dc, +12 V dc, and −12 V dc. The drive voltages are +5 V dc and +12 V dc.

The following figure shows the maximum current that is provided for system components.

System Component	Maximum Current	
	+12 V dc	+5 V dc
Internal fixed disk drives†	4.5 A	5.0 A
Auxiliary-device port	None	300 mA
Keyboard port	None	275 mA
† Total for the two power-supply connectors		

Figure 1-8. Component Maximum Current

The following figure shows the maximum load currents that are allowed for each channel connector.

Supply Voltage	Maximum Load Current
+ 5.0 V dc	1.6 A
+12.0 V dc	0.175 A
−12.0 V dc	0.040 A

Figure 1-9. Channel Load Current

The formulas that are used to determine the power requirements and the voltage-regulation tolerances are in the Micro Channel architecture information in the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures.*

Output Protection

A short circuit that is placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state, with no damage to the power supply.

If an overvoltage fault occurs (in the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of the nominal value of the power supply.

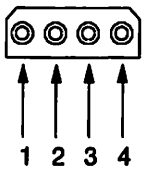
If either of these shutdown states occurs, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least 10 seconds.

Voltage Sequencing

At power-on time, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Power-Supply Connectors

The power supply provides two 4-pin connectors for internal devices. The total power that is used by both connectors must not exceed the amount shown in Figure 1-8 on page 1-13.



Pin	Signal	Pin	Signal
1	+12 V dc	3	dc return
2	dc return	4	+5 V dc

Figure 1-10. Voltage Assignments for the Internal Power-Supply Connectors

Section 2. Programmable Option Select

Description 2-3
POS I/O Address Map 2-5
Card Selected Feedback Register (Hex 0091) 2-6
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-7
System Board Group 1 POS Register 2 (Hex 0102) 2-8
System Board Group 1 POS Register 3 (Hex 0103) 2-9
System Board Group 1 POS Register 4 (Hex 0104) 2-11
System Board Group 1 POS Register 5 (Hex 0105) 2-11
System Board Group 2 POS Register 2 (Hex 0102) 2-12
System Board Group 2 POS Register 3 (Hex 0103) 2-12
System Board Group 3 POS Register 2 (Hex 0102) 2-13
System Board Group 3 POS Register 3 (Hex 0103) 2-13
Adapter Enable/Setup Register (Hex 0096) 2-15

© Copyright IBM Corp. 1992

Notes:

Description

Programmable Option Select (POS) eliminates the need for switches on the system board by replacing their function with programmable registers. This section describes the POS information that is used on the Model 77 system board. For additional information about POS, refer to the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures.*

Note: For the Model M77, there is additional POS information for the M-Audio Capture and Playback Adapter. Refer to the *M-Audio Capture and Playback Adapter Installation and Technical Reference Manual* for more information.

Warning:

- Programmable options should be set only through the System Configuration utility programs. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignments of the same system resource, improper operation of the feature, loss of data, or damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention occurs, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- The channel-reset bit (bit 7) in the Adapter Enable/Setup register (hex 0096) must be set to 0 to program the adapters.
- The system board does not support 16-bit I/O operations to 8-bit POS registers. Using 16-bit I/O instructions on 8-bit POS registers causes incorrect data to be written to or read from the registers. Only 8-bit transfers are supported for setup operations.

Setup functions respond to I/O addresses hex 0100 through hex 0107 only when their unique setup signal is active. The following precautions must be taken before individual bits are set in the POS registers.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register must be set to 1 to allow adapter setup.
- Bits 7, 6, and 1 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system board functions.

System Board Setup Group 1:

- Bit 7 in the System Board Enable/Setup register must be set to 0 to enable setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bits 6 and 1 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system board functions.

System Board Setup Group 2:

- Bit 6 in the System Board Enable/Setup register must be set to 0 to enable setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bits 7 and 1 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system board functions.

System Board Setup Group 3:

- Bit 1 in the System Board Enable/Setup register must be set to 0 to enable setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bits 7 and 6 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem or other system board functions.

POS I/O Address Map

The following figure shows the organization of the I/O address space that is used by POS. Bit 0 of POS Register 2 and bits 6 and 7 of POS Register 5 are fixed. All other bits in POS Registers 2 through 5 are free-form.

Address (Hex)	Register
0094	System Board Enable/Setup register
0096	Adapter Enable/Setup register
0100	POS Register 0—Adapter Identification byte (low byte)
0101	POS Register 1—Adapter Identification byte (high byte)
0102	POS Register 2—Option Select Data byte 1 (bit 0 is card enable)
0103	POS Register 3—Option Select Data byte 2
0104	POS Register 4—Option Select Data byte 3
0105	POS Register 5—Option Select Data byte 4
0106	Reserved
0107	Reserved

Figure 2-1. POS I/O Address Map

Card Selected Feedback Register (Hex 0091)

Whenever an adapter is addressed, it responds by setting the '-card selected feedback' signal (-CD SFDBK) to active. This signal is derived from the address decode, driven by a totem-pole driver, and latched by the system board. It can be read through the Card Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs can use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and determine whether the system board I/O or an adapter is addressed and functioning.

Bit	Function
7–1	Reserved
0	Card selected feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7–1 These bits are reserved.

Bit 0 This bit is set to 1 when -CD SFDBK was active on a previous cycle or when a system board I/O function (diskette drive, serial port, or parallel port interface) is accessed by an I/O cycle. Reading this register resets this bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information in three sets of POS registers: Groups 1 through 3.

- The diskette drive controller, parallel port, and system board memory are configured through the Group 1 POS registers.
- The serial ports are configured through Group 2.
- The SCSI controller is configured through Group 3.

Figure 2-3 indicates the groups, POS register numbers, and I/O functions that are supported.

Group	POS Register	Device
1	2	Diskette drive controller Parallel port controllers
1	3	Memory connectors
1	4	Diskette arbitration level
1	5	Parallel port arbitration level
2	2, 3	Serial port controller
3	2, 3	SCSI controller

Figure 2-3. Devices Supported in Setup Mode

System Board Enable/Setup Register (Hex 0094)

This is a read/write register. All bits in this register default to 1 (enabled).

Bit	Function
7	Enable/setup system board group 1
6	Enable/setup system board group 2
5–2	Reserved
1	Enable/setup SCSI controller
0	Reserved

Figure 2-4. System Board Enable/Setup Register (Hex 0094)

Bit 7 When this bit is set to 0, the diskette drive controller, parallel port controllers, memory connectors, diskette arbitration level, and parallel port arbitration level are placed into setup mode.

When this bit is set to 1, the system board functions are enabled.

Bit 6 When this bit is set to 0, the system board serial controller is placed into setup mode. System Board Group 2 POS Register 2 (hex 0102) includes the serial port enable and interrupt-level selection. The serial port address selection is in System Board Group 2 POS Register 3 (hex 0103).

Bits 5–2 These bits are reserved.

Bit 1 When this bit is set to 0, the SCSI controller on the system board is placed into setup mode and is controlled through POS Register 2 (hex 0102). When this bit is set to 1 and bit 0 in POS Register 2 is set to 1, the SCSI controller on the system board is enabled.

Bit 0 This bit is reserved.

System Board Group 1 POS Register 2 (Hex 0102)

When the system board is in setup mode, this read/write register controls the diskette drive controller and parallel port. Reading this register returns the current state of the following system board functions.

Bit	Function
7	Disable parallel port extended mode
6, 5	Select parallel port
4	Enable parallel port
3	Reserved
2	Reserved
1	Enable diskette drive interface
0	Enable system board

Figure 2-5. System Board POS Register 2 (Hex 0102)

Bit 7 When this bit is set to 0, the parallel port is configured as an 8-bit, parallel, bidirectional (extended mode) interface. When this bit is set to 1, the parallel port is configured as an 8-bit, parallel, unidirectional interface (extended mode is disabled). This bit is set to 0 after the system is powered-on.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Address (Hex)	Interrupt Level
0 0	Parallel 1	03BC–03BF†	7
0 1	Parallel 2	0378–037D	7
1 0	Parallel 3	0278–027D	7
1 1	Parallel 4	1378–137D	7

† The addresses are hex 1278–127D for the DMA operations.

Figure 2-6. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bits 3, 2 These bits are reserved.

Bit 1 When this bit and bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When this bit is set to 1, the individual device controllers on the system board can be enabled and disabled. When this bit is set to 0, the system board controllers for the diskette drive, serial port, and parallel port are disabled.

System Board Group 1 POS Register 3 (Hex 0103)

The system board has connectors for installing single inline memory modules (memory modules); for more information about these memory connectors, see "System Board Memory Connectors" on page 3-8.

Each memory module is defined by five signals: 'presence detect 0−3' and '-ECC memory.' The states of these signals are indicated by 3 bytes that are accessed through POS Register 3. To read each byte, write the appropriate index to POS Register 3, and then read POS Register 3.

The following figure shows the relationship of the index values to the memory connectors and the available data register information.

Index Value (Hex)	Function
00	Presence-detection information for memory connectors 3 and 1
04	-ECC memory for connectors 1 through 4
01	Presence-detection information for memory connectors 4 and 2

Note: Values that are not shown are reserved.

Figure 2-7. System Board Group 1 POS Register 3 (Hex 0103)

The following information is returned by reading POS Register 3 after the appropriate index value has been written to POS Register 3. For coding of the presence-detection signals, see Figure 3-8 on page 3-12.

Index 00 Bit	Function
7	Presence detect 3, memory connector 3
6	Presence detect 2, memory connector 3
5	Presence detect 1, memory connector 3
4	Presence detect 0, memory connector 3
3	Presence detect 3, memory connector 1
2	Presence detect 2, memory connector 1
1	Presence detect 1, memory connector 1
0	Presence detect 0, memory connector 1

Figure 2-8. System Board POS Group 1 Register 3 (Hex 0103)—Index 00

Index 04 Bit	Function
7	-Alternative microprocessor or math coprocessor installed (80486DX2 or 80487SX)
6	Base microprocessor speed (0=25 MHz, 1=33 MHz)
5	Current microprocessor speed (0=25 MHz, 1=33 MHz)
4	Reserved
3	-ECC memory, memory connector 4
2	-ECC memory, memory connector 3
1	-ECC memory, memory connector 2
0	-ECC memory, memory connector 1

Figure 2-9. System Board POS Group 1 Register 3 (Hex 0103)—Index 04

Index 01 Bit	Function
7	Presence detect 3, memory connector 4
6	Presence detect 2, memory connector 4
5	Presence detect 1, memory connector 4
4	Presence detect 0, memory connector 4
3	Presence detect 3, memory connector 2
2	Presence detect 2, memory connector 2
1	Presence detect 1, memory connector 2
0	Presence detect 0, memory connector 2

Figure 2-10. System Board POS Group 1 Register 3 (Hex 0103)—Index 01

System Board Group 1 POS Register 4 (Hex 0104)

This register is used to specify the diskette drive arbitration level.

Bit	Function
7–4	Reserved
3–0	Diskette drive arbitration level

Figure 2-11. System Board Group 1 POS Register 4 (Hex 0104)

Bits 7–4 These bits are reserved.

Bits 3–0 These bits are used to select the diskette drive arbitration level.

System Board Group 1 POS Register 5 (Hex 0105)

This register is used to specify the arbitration level that is used by the parallel port controller.

Bit	Function
7–4	Reserved
3–0	Parallel port arbitration level

Figure 2-12. System Board Group 1 POS Register 5 (Hex 0105)

Bits 7–4 These bits are reserved.

Bits 3–0 These bits are used to select the arbitration level that is used by the parallel port controller.

System Board Group 2 POS Register 2 (Hex 0102)

This register is used to enable the two serial ports on the system board. The two serial ports are identified as serial port A and serial port B; serial port A is the connector on the left, as viewed from the front of the system.

Bit	Function
7–5	Reserved
4	Enable serial port B
3	Enable serial port A
2	Reserved
1	Select serial port B interrupt
0	Select serial port A interrupt

Figure 2-13. System Board Group 2 POS Register 2 (Hex 0102)

Bits 7–5 These bits are reserved.

Bit 4 When this bit is set to 1 and bit 0 in POS Register 2 (Group 1) is set to 1, serial port B is enabled.

Bit 3 When this bit is set to 1 and bit 0 in POS Register 2 (Group 1) is set to 1, serial port A is enabled.

Bit 2 This bit is reserved.

Bit 1 When this bit is set to 1, serial port B uses IRQ4. When this bit is set to 0, serial port B uses IRQ3.

Bit 0 When this bit is set to 1, serial port A uses IRQ4. When this bit is set to 0, serial port A uses IRQ3.

System Board Group 2 POS Register 3 (Hex 0103)

This register is used to select the addresses of the two serial ports.

Bit	Function
7–4	Serial port B address
3–0	Serial port A address

Figure 2-14. System Board Group 2 POS Register 3 (Hex 0103)

Bits 7–4 These bits are used to determine the address of serial port B (right).

Bits 3–0 These bits are used to determine the address of serial port A (left).

Bits 7654 3210	Assignment	Address (Hex)	
		Compatible	Extended
0000	Serial 1	03F8–03FF	83F8–83FF
0001	Serial 2	02F8–02FF	82F8–82FF
0010	Serial 3	3220–3227	B220–B227
0011	Serial 4	3228–322F	B228–B22F
0100	Serial 5	4220–4227	C220–C227
0101	Serial 6	4228–422F	C228–C22F
0110	Serial 7	5220–5227	C220–D227
0111	Serial 8	5228–522F	D228–D22F
1000	Serial 9	3A20–3A27	BA20–BA27
1001	Serial 10	3A28–3A2F	BA28–BA2F
1010	Serial 11	3A30–3A37	BA30–BA37
1011	Serial 12	3A38–3A3F	BA38–BA3F
1100	Serial 13	3A80–3A87	BA80–BA87
1101	Serial 14	3A88–3A8F	BA88–BA8F
1110	Serial 15	3A90–3A97	BA90–BA97
1111	Serial 16	3A98–3A9F	BA98–BA9F

Figure 2-15. Serial Port Addresses

System Board Group 3 POS Register 2 (Hex 0102)

This register is used to enable the SCSI controller on the system board.

Bit	Function
7–1	Reserved
0	Enable SCSI

Figure 2-16. System Board Group 3 POS Register 2 (Hex 0102)

Bits 7–1 These bits are reserved.

Bit 0 When this bit is set to 1, the SCSI controller on the system board is enabled.

System Board Group 3 POS Register 3 (Hex 0103)

This register is used to select the SCSI ID for the SCSI controller on the system board.

Bit	Function
7–5	SCSI ID
4–0	Reserved

Figure 2-17. System Board Group 3 POS Register 3 (Hex 0103)

Bits 7–5 These bits determine the SCSI ID for the SCSI controller on the system board.

Bits 7 6 5	System Board SCSI ID
0 0 0	0
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	4
1 0 1	5
1 1 0	6
1 1 1	7

Figure 2-18. System Board SCSI Controller ID

Bits 4–0 These bits are reserved.

Adapter Enable/Setup Register (Hex 0096)

This read/write register resets the channel, enables the '-card setup' signal, and configures the connectors.

Bit	Function
7	Channel reset
6–4	Reserved
3	Enable card setup
2–0	Channel select 2–0

Figure 2-19. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When this bit is set to 1, it activates the 'channel reset' signal to all connectors.

Bits 6–4 These bits are reserved and must be set to 0.

Bit 3 When this bit is set to 1, the '-card setup' signal that is selected by bits 2 through 0 is enabled.

Bits 2–0 These bits are the address bits for the '-card setup' signal to the connectors. Connectors 1 through 5 are addressed as 0 through 4. When bit 3 is set to 1, these bits select the connector or function for setup cycles.

Each channel connector has a unique '-card setup' signal (-CD SETUP) associated with it. This signal is used to select the adapters for setup cycles, allowing access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Note: -CD SETUP goes active only when an operation is performed in the I/O address range hex 0100 through 0107.

Section 3. System Board

Description 3-3
Microprocessor and Math Coprocessor 3-3
Micro Channel Architecture Implementation 3-3
  The Central Arbiter 3-3
  Arbitration Bus Priority Assignments 3-4
  Central Arbiter Programming 3-5
The Bus Extension 3-6
Diskette Drive Connectors 3-7
System Board Memory Connectors 3-8
SCSI-Device Connector 3-9
Memory 3-10
  ROM Subsystem 3-11
  RAM Subsystem 3-11
  Memory Subsystem Control 3-12
  Memory-Presence Determination 3-12
  Cached Memory Address Space 3-13
  RT/CMOS RAM 3-16
    RT/CMOS Address and NMI Mask Register (Hex 0070) . . 3-16
    RT/CMOS Data Register (Hex 0071) 3-17
    RT/CMOS RAM I/O Operations 3-17
    Real-Time Clock Bytes (Hex 000–00D) 3-18
    CMOS RAM Configuration 3-21
Miscellaneous System Functions and Ports 3-25
  Nonmaskable Interrupt 3-25
  System Control Port B (Hex 0061) 3-26
  System Control Port A (Hex 0092) 3-27
  Power-On Password 3-28
  Selectable Boot Sequence 3-29
Hardware Compatibility 3-29
Error Codes 3-30

© Copyright IBM Corp. 1992

Notes:

Description

This section describes the microprocessors, math coprocessor, channel differences, memory subsystems, and miscellaneous system ports, and connectors on the Model 77 system board. Additional information about these topics can be found in the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces.*

Microprocessor and Math Coprocessor

The Intel** 80486SX microprocessor in the Model 77 runs at 25 MHz or 33 MHz. It has a 32-bit address interface and a 32-bit data interface and is software-compatible with the 80386SX and 80386DX microprocessors. The Model 77 also supports the Intel 80486DX2 microprocessor, which runs at 25 MHz (system speed)/50 MHz (microprocessor speed) or 33 MHz (system speed)/66 MHz (microprocessor speed).

The 80487SX math coprocessor is matched to the speed of the system microprocessor and operates in synchronous mode. The 80487SX math coprocessor is software-compatible with the 80387DX math coprocessor.

Micro Channel Architecture Implementation

This section describes the implementation of the Micro Channel architecture in Model 77 systems. For general information about Micro Channel architecture, refer to the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures.*

The Central Arbiter

The central arbitration control point gives programmable subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. The central arbiter supports up to 15 arbitrating devices (levels hex 0 through E) and the system microprocessor (level hex F).

** Trademark of Intel Corporation.

Note: The system board small computer system interface (SCSI) controller performs cycles at arbitration level hex F if the Micro Channel arbitration level is F when the SCSI controller requests the bus.

Arbitration Bus Priority Assignments

The following figure shows the assignment of arbitration levels. The functions with the *lowest* arbitration level have the *highest* priority.

Arb. Level	Primary Assignment
-2	Memory refresh
-1	NMI
0	DMA channel 0 (programmable to any arbitration level)
1	DMA channel 1
2	DMA channel 2
3	DMA channel 3
4	DMA channel 4 (programmable to any arbitration level)
5	DMA channel 5
6	DMA channel 6
7	DMA channel 7
8–E	Available
F	System microprocessor

Figure 3-1. Arbitration Bus Priority Assignments

Note: Devices that are designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so that diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, which is normally on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation and by the previous controlling master. To prevent overruns, the diskette drive controller should not be held inactive for more than 12 microseconds.

Nonmaskable interrupt (NMI) service is executed at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal (ARB/-GNT) is in the arbitration state.

When the central arbitration control point receives a level -1 request (NMI, a system board internal signal), it activates -PREEMPT, waits for the end of the transfer, and then places ARB/-GNT into the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level -1 request

and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following figures.

Bit	Function
7	Enable system microprocessor cycle
6	Arbitration mask
5	Enable extended arbitration (not supported)
4–0	Reserved

Figure 3-2. Arbitration Register (Hex 0090)—Write

Bit	Function
7	Enable system microprocessor cycle
6	Arbitration masked by NMI
5	Bus time-out
4	Reserved
3–0	Value of arbitration bus during previous grant state

Figure 3-3. Arbitration Register (Hex 0090)—Read

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. The power-on self-test (POST) sets this bit to 1.

Reading this bit as a 1 indicates that the system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 enables extended arbitration. The minimum arbitration cycle is 300 nanoseconds; this bit extends that minimum to 600 nanoseconds. POST sets this bit to 0.

Reading this bit as a 1 indicates that a bus time-out has occurred and resets bit 6 in this register to 0.

Bit 4 This bit is reserved and must be set to 0.

Bits 3–0 These bits are undefined for a write operation and must be set to 0.

Reading these bits returns the arbitration level of the arbiter that controlled the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

The Bus Extension

The Model 77 system uses a bus extension that provides five channel connectors:

- Three 32-bit connector with matched memory
- One 32-bit connector with auxiliary-video extension
- One 32-bit connector with base-video extension

The adapters are installed horizontally into the bus extension.

Diskette Drive Connectors

The diskette drive cable connects to the system board and provides three 2- by 17-pin connectors for attaching internal diskette drives. Each connector passes control and data signals between the diskette drive controller on the system board and the drives. It also provides the power to each drive.

The following figure shows the signal assignments and pin numbers for the diskette drive connectors.

Pin	Signal	Pin	Signal
1	Ground	2	Data rate select 1
3	+5 V dc	4	Drive type ID 1
5	Ground	6	+12 V dc
7	Ground	8	-Index
9	Drive type ID 0	10	Reserved
11	Ground	12	-Drive select
13	Ground	14	Reserved
15	Ground	16	-Motor enable
17	Media type ID 1	18	-Direction in
19	Ground	20	-Step
21	Ground	22	-Write data
23	Ground	24	-Write enable
25	Ground	26	-Track 0
27	Media type ID 0	28	-Write protect
29	Ground	30	-Read data
31	Ground	32	-Head 1 select
33	Data rate select 0	34	-Diskette change

Figure 3-4. Diskette Drive Connectors

System Board Memory Connectors

The Model 77 system board has four 72-pin connectors for installing memory modules. The following figure shows the pin assignments for the 1- by 72-pin memory connector. Refer to "Memory-Presence Determination" on page 3-12 for decoding of the 'presence detect' and '-ECC memory' signals.

Pin	Signal	Pin	Signal
1	Ground	37	Parity data 1
2	Data 0	38	Parity data 3
3	Data 16	39	Ground
4	Data 1	40	Column address strobe 0
5	Data 17	41	Column address strobe 2
6	Data 2	42	Column address strobe 3
7	Data 18	43	Column address strobe 1
8	Data 3	44	Row address strobe 0
9	Data 19	45	Row address strobe 1
10	+5 V dc	46	Block select 1
11	-Column address strobe P	47	Write enable
12	Address 0	48	Reserved
13	Address 1	49	Data 8
14	Address 2	50	Data 24
15	Address 3	51	Data 9
16	Address 4	52	Data 25
17	Address 5	53	Data 10
18	Address 6	54	Data 26
19	Reserved	55	Data 11
20	Data 4	56	Data 27
21	Data 20	57	Data 12
22	Data 5	58	Data 28
23	Data 21	59	+5 V dc
24	Data 6	60	Data 29
25	Data 22	61	Data 13
26	Data 7	62	Data 30
27	Data 23	63	Data 14
28	Address 7	64	Data 31
29	Block select 0	65	Data 15
30	+5 V dc	66	Block select 2
31	Address 8	67	Presence detect 0
32	Address 9	68	Presence detect 1
33	Row address strobe 3	69	Presence detect 2
34	Row address strobe 2	70	Presence detect 3
35	Parity data 2	71	Block select 3
36	Parity data 0	72	Ground

Figure 3-5. System Board Memory Connectors

SCSI-Device Connector

The system board provides two connectors for attaching SCSI devices: one internal connector with cable and one external connector.

The cable connects to the system board and provides three 2- by 25-pin connectors for attaching internal SCSI devices. The system board has one 2- by 30-pin connector for attaching external SCSI devices.

The following figure shows the pin assignments for the internal 2- by 25-pin SCSI connector.

Pin	Signal	Pin	Signal
1	Ground	26	+Terminal power
2	Data 0	27	Ground
3	Ground	28	Ground
4	Data 1	29	Ground
5	Ground	30	Ground
6	Data 2	31	Ground
7	Ground	32	-Attention
8	Data 3	33	Ground
9	Ground	34	Ground
10	Data 4	35	Ground
11	Ground	36	-Busy
12	Data 5	37	Ground
13	Ground	38	-Acknowledge
14	Data 6	39	Ground
15	Ground	40	-Reset
16	Data 7	41	Ground
17	Ground	42	-Message
18	Data P	43	Ground
19	Ground	44	-Select
20	Ground	45	Ground
21	Ground	46	-Control/data
22	Ground	47	Ground
23	Ground	48	-Request
24	Ground	49	Ground
25	Not connected	50	-Input/output

Figure 3-6. Internal SCSI-Device Connector Pin Assignments

The following figure shows the pin assignments for the 2- by 30-pin external SCSI connector.

Pin	Signal	Pin	Signal
1	Ground	31	Ground
2	Data 0	32	-Attention
3	Ground	33	Ground
4	Data 1	34	Ground
5	Ground	35	Ground
6	Data 2	36	-Busy
7	Ground	37	Ground
8	Data 3	38	-Acknowledge
9	Ground	39	Ground
10	Data 4	40	-Reset
11	Ground	41	Ground
12	Data 5	42	-Message
13	Ground	43	Ground
14	Data 6	44	-Select
15	Ground	45	Ground
16	Data 7	46	-Control/data
17	Ground	47	Ground
18	Data P	48	-Request
19	Ground	49	Ground
20	Ground	50	-Input/output
21	Ground	51	Ground
22	Ground	52	Reserved
23	Ground	53	Reserved
24	Ground	54	Reserved
25	Not connected	55	Reserved
26	+Terminal power	56	Reserved
27	Ground	57	Reserved
28	Ground	58	Reserved
29	Ground	59	Reserved
30	Ground	60	Reserved

Figure 3-7. External SCSI-Device Connector Pin Assignments

Memory

The Model 77 uses the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- Real-time clock and CMOS RAM (RT/CMOS RAM)
- Nonvolatile random access memory (NVRAM)

ROM Subsystem

The ROM subsystem consists of 128KB of physical memory. Mapped ROM is active at power-on time and is assigned to the top of the first and last 1MB of address space (hex 0E0000 to 0FFFFF and hex FE0000 to FFFFFF). After POST ensures that system memory is operating properly, the ROM code is copied to RAM at the same address space, and ROM is disabled.

Access to ROM or RAM at address space hex 0E0000 to 0FFFFF is controlled by the ROM-enable bit in the Memory-Controller Configuration register. When ROM is enabled, it is not parity-checked.

RAM Subsystem

The RAM subsystem on the system board starts at address hex 000000 of the address space. The RAM subsystem is 72 bits wide: 64 data bits and 8 parity bits. One parity bit is generated for each byte of data that is written. During a read operation, one parity bit is checked for each byte of data that is read by the device controlling the bus.

Three memory connectors are provided on the system board. Each connector can support 2MB, 4MB, or 8MB of 70-nanosecond memory.

The system enables and disables memory in 1MB blocks for 2MB memory modules, or 4MB blocks for 4MB or 8MB memory modules. Each 1MB block must start on a 1MB boundary. Because 128KB of I/O ROM, 128KB of system board ROM, and 128KB of video memory are mapped within the first 1MB of address space, the first physical 1MB of RAM cannot be mapped to contiguous addresses and is split at the 640KB boundary, creating a 384KB overflow. The high 128KB of the overflow is mapped to the system board ROM address space; the remaining 256KB, called the *split memory block*, is either reserved for system use or mapped to the first available address following the last full 1MB of activated system board memory. Split-memory-block remapping and disabling are controlled by the Memory-Controller Configuration register. The presence of the split memory block in the memory address space might be affected by nonsystem memory.

Memory Subsystem Control

Memory on the system board is parity-checked random access memory that can be interleaved or noninterleaved. To operate in the interleaved mode, the memory must be paired in connectors 1 and 2, or 3 and 4 (for memory connector information, see "System Board Memory Connectors" on page 3-8). The memory controller automatically interleaves memory between the even and odd banks. If more memory is in one bank than in the other, the difference is used as noninterleaved memory. For example, if 2MB is installed in connector 2 and 4MB is installed in connector 1, the 2MB in connector 2 is interleaved with 2MB of the 4MB in connector 1. The remaining 2MB in connector 1 is noninterleaved.

When operating in the interleaved mode, the microprocessor can perform burst cycles with two-way interleaved accesses. This allows the microprocessor to perform zero-wait-state transfers for alternating 32-bit transfers in the burst cycle.

Memory-Presence Determination

The presence-detect signals are used by the system to determine the size and speed of memory on the memory module. The pins are either not connected (1) or connected to ground (0).

A set of 4 bits shows the state of all presence-detect signals for a specific memory connector; the bit is set to 0 when the signal is connected to ground. The following figure shows the information that is indicated by these bits, as well as the bank size of the memory module. Combinations that are not shown are reserved.

Presence Detect 3 2 1 0	Single Inline Memory Module Definition	Bank Size
1 1 0 0	2MB 70-ns memory	1MB
0 1 0 0	4MB 70-ns memory	4MB
1 0 1 1	8MB 70-ns memory	4MB

Figure 3-8. Presence-Detect Bits

Cached Memory Address Space

The following memory maps show the memory addresses that can be cached; only system board memory can be cached. The Model 77 address space contains three cacheable regions:

- Region 1: Memory addresses from 0 to 1MB
- Region 2: Memory addresses from 1MB to 16MB
- Region 3: Memory addresses from 16MB to 40MB plus 256KB of split memory

All system board memory in regions 2 and 3 is cacheable. The Programmable Boundary register for region 2 controls the upper boundaries of the memory space that is to be cached. Region 3 has a fixed cacheable boundary at 2GB (GB equals 1073741824 bytes).

The Set Configuration utility program might assign nonsystem memory to these cached regions, depending on the system configuration. POST establishes these cached regions, and they must not be altered.

Nonsystem memory can be located as follows:

- Region 1: Between memory addresses hex 0C0000 and 0DFFFF
- Region 2: Memory addresses from 16MB down to system memory
- Region 3: Memory addresses from 4GB down to 2GB of system memory

Note: If nonsystem memory is present between 16MB and 2GB, the system disables the processor cache during POST, and system performance is reduced.

The following memory map shows the cached areas of system memory, with no nonsystem memory allocation outside of region 1.

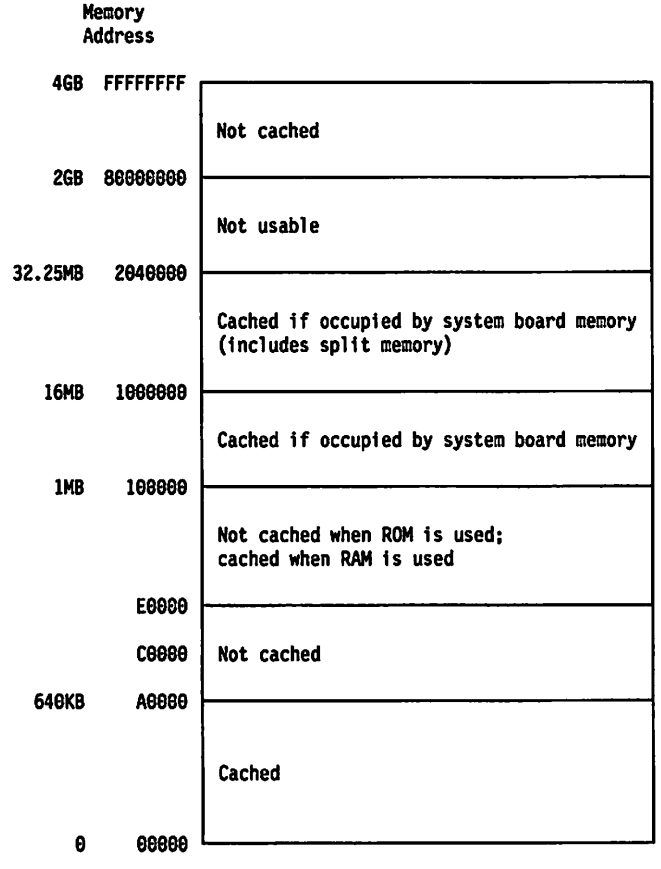


Figure 3-9. Memory Map, Cached Regions—System Memory

The following memory map shows the cached areas with 8MB of nonsystem memory present at 8MB to 16MB.

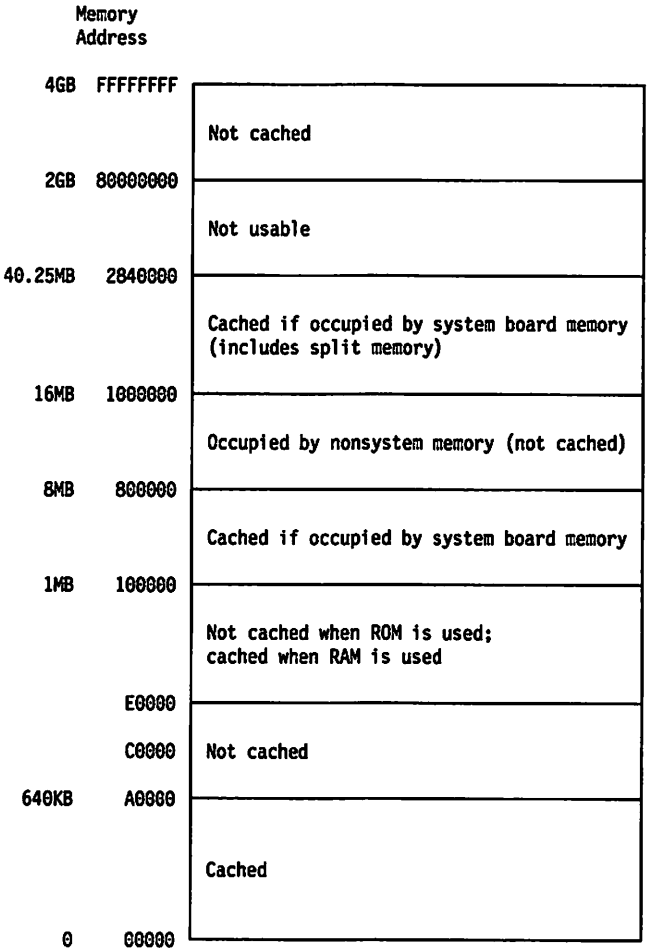


Figure 3-10. Memory Map, Cached Regions—Nonsystem Memory from 8MB to 16MB

RT/CMOS RAM

The RT/CMOS RAM (real-time clock/complementary metal-oxide semiconductor RAM) module contains the real-time clock and 64 bytes of CMOS RAM. The clock uses 14 bytes of this memory, and the rest is allocated to configuration and system-status information. A battery keeps the RT/CMOS RAM active when the power supply is off.

The system board has an additional 8KB CMOS RAM extension that is used to store configuration and other system information. This RAM extension is kept active by the battery.

The following figure shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000–00D	Real-Time Clock bytes
00E	Diagnostic Status byte
00F	Shutdown Status byte
010	Diskette Drive Type byte
011	Fixed Disk Drive Type byte
012	Reserved
013	Reserved
014	Equipment byte
015, 016	Low and high Base Memory bytes
017, 018	Low and high Expansion Memory bytes
019–031	Reserved
032, 033	Configuration CRC bytes
034	Reserved
035, 036	Low and high usable memory above 1MB
037	Date-Century byte
038–03F	Reserved

Figure 3-11. RT/CMOS RAM Address Map

RT/CMOS Address and NMI Mask Register (Hex 0070)

This register is used with the RT/CMOS Data register (hex 0071) to read from and write to the RT/CMOS RAM bytes.

Warning: The operation that follows a write operation to this register must access address hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS can occur.

Bit	Function
7	NMI mask
6	Reserved
5–0	RT/CMOS RAM address

Figure 3-12. RT/CMOS Address and NMI Mask Register (Hex 0070)

Bit 7 When this write-only bit is set to 1, the NMI is masked (disabled). This bit is set to 1 by a power-on reset.

Bit 6 This bit is reserved.

Bits 5–0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This register is used with the RT/CMOS Address and NMI Mask register to read from and write to the RT/CMOS RAM bytes.

Bit	Function
7–0	RT/CMOS data

Figure 3-13. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts must be masked to prevent other interrupt routines from changing the CMOS Address register before data is read or written.

Warning: The operation that follows a write operation to hex 0070 must access address hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Writing to RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS Address and NMI Mask register (hex 0070).
2. Write the data to address hex 0071.
3. Write the address hex 0F to the RT/CMOS Address and NMI Mask register; this leaves address hex 0070 pointing to the Shutdown Status byte (hex 0F).
4. Read from address hex 0071 to restore the RT/CMOS (see the warning above).

Reading from RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS Address and NMI Mask register (hex 0070).
2. Read the data from address hex 0071.
3. Write the address hex 0F to the RT/CMOS Address and NMI Mask register; this leaves address hex 0070 pointing to the Shutdown Status byte (hex 0F).
4. Read from address hex 0071 to restore the RT/CMOS.

Real-Time Clock Bytes (Hex 000–00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following figure.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second alarm	1
002	Minutes	2
003	Minute alarm	3
004	Hours	4
005	Hour alarm	5
006	Day of week	6
007	Date of month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-14. Real-Time Clock Bytes (Hex 000–00D)

Note: The system initializes Status Registers A and B when the time and date are set. Interrupt 1AH is the BIOS interface that is used to read and set the time and date; it initializes the registers in the same way that the system does.

Status Register A (Hex 00A)

Bit	Function
7	Update in progress
6–4	22-stage divider
3–0	Rate-selection bits

Figure 3-15. Status Register A (Hex 00A)

Bit 7 When this bit is set to 1, it indicates that the time-update cycle is in progress. When it is set to 0, it indicates that the current date and time can be read.

Bits 6–4 These bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768-kHz time base. This is the only value that is supported by the system for proper timekeeping.

Bits 3–0 These bits allow the selection of a divider output frequency. The system initializes the rate-selection bits to binary 0110, which selects a 1.024-kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Enable periodic interrupt
5	Enable alarm interrupt
4	Enable update-ended interrupt
3	Enable square-wave frequency
2	Date mode
1	24-hour mode
0	Enable daylight-saving-time mode

Figure 3-16. Status Register B (Hex 00B)

Bit 7 When this bit is set to 0, the cycle is updated by advancing the counts at a rate of one per second. When this bit is set to 1, any update cycle in progress ends immediately, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This is a read/write bit that enables an interrupt to occur at a rate that is specified by the rate and divider bits in Status Register A. When this bit is set to 1, the interrupt is enabled. The system initializes this bit to 0.

Bit 5 When this bit is set to 1, the alarm interrupt is enabled. The system initializes this bit to 0.

Bit 4 When this bit is set to 1, the update-ended interrupt is enabled. The system initializes this bit to 0.

Bit 3 When this bit is set to 1, the square-wave frequency is enabled as specified by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit is used to specify whether the binary-coded-decimal (BCD) or binary format is used for time-and-date calendar updates. When this bit is set to 1, it indicates the binary format. The system initializes this bit to 0.

Bit 1 This bit is used to specify whether the Hours byte is in 12-hour or 24-hour mode. When this bit is set to 1, it indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When this bit is set to 1, the daylight-saving-time mode is enabled. When this bit is set to 0, the daylight-saving-time mode is disabled, and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt-request flag
6	Periodic-interrupt flag
5	Alarm-interrupt flag
4	Update-ended interrupt flag
3–0	Reserved

Figure 3-17. Status Register C (Hex 00C)

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 When this bit is set to 1, it indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When this bit is set to 1, it indicates that a periodic interrupt occurred.

Bit 5 When this bit is set to 1, it indicates that an alarm interrupt occurred.

Bit 4 When this bit is set to 1, it indicates that an update-ended interrupt occurred.

Bits 3–0 These bits are reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6–0	Reserved

Figure 3-18. Status Register D (Hex 00D)

Bit 7 This read-only bit monitors the internal battery. When this bit is set to 1, it indicates that the real-time clock has power. When it is set to 0, it indicates that the real-time clock has lost power and the data in CMOS RAM is no longer valid.

Bits 6–0 These bits are reserved.

CMOS RAM Configuration

The following shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-time clock power
6	Configuration record and checksum status
5	Incorrect configuration
4	Memory-size mismatch
3	Fixed disk controller/drive C initialization status
2	Time status indicator
1	Adapter configuration miscompare
0	Adapter ID time-out

Figure 3-19. Diagnostic Status Byte (Hex 00E)

Bit 7 When this bit is set to 1, it indicates that the real-time clock has lost power.

Bit 6 When this bit is set to 1, it indicates that a checksum is incorrect.

Bit 5 When this bit is set to 1, it indicates that the configuration information is incorrect.

Bit 4 When this bit is set to 1, it indicates that the memory size does not match the configuration information.

Bit 3 When this bit is set to 1, it indicates that the controller or fixed disk drive failed initialization.

Bit 2 When this bit is set to 1, it indicates that the time and date are invalid.

Bit 1 When this bit is set to 1, it indicates that the adapters do not match the configuration information.

Bit 0 When this bit is set to 1, it indicates that a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is used by POST and BIOS.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive that is installed.

Bit	Function
7–4	First diskette drive type
3–0	Second diskette drive type

Figure 3-20. Diskette Drive Type Byte (Hex 010)

Bits 7–4 These bits indicate the type of the first diskette drive.

Bits 7 6 5 4	Function
0 0 0 0	No drive present
0 0 0 1	5.25-inch, 360KB diskette drive
0 0 1 0	5.25-inch, 1.2MB diskette drive
0 0 1 1	3.5-inch, 720KB diskette drive
0 1 0 0	3.5-inch, 1.44MB diskette drive
0 1 1 0	3.5-inch, 2.88MB diskette drive

Note: Combinations that are not shown are reserved.

Figure 3-21. First Diskette Drive Type Bits

Bits 3–0 These bits indicate the type of the second diskette drive.

Bits 3 2 1 0	Function
0 0 0 0	No drive present
0 0 0 1	5.25-inch, 360KB diskette drive
0 0 1 0	5.25-inch, 1.2MB diskette drive
0 0 1 1	3.5-inch, 720KB diskette drive
0 1 0 0	3.5-inch, 1.44MB diskette drive
0 1 1 0	3.5-inch, 2.88MB diskette drive

Note: Combinations that are not shown are reserved.

Figure 3-22. Second Diskette Drive Type Bits

Fixed Disk Drive Type Byte (Hex 011): This byte defines the type of fixed disk drive that is installed. A value of hex 000 indicates that no fixed disk drive is installed. This byte is not used for SCSI fixed disk drives.

Note: For more information about fixed disk drives, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Reserved Bytes (Hex 012 and 013): These bytes are reserved.

Equipment Byte (Hex 014): This byte defines the basic equipment in the system for the power-on diagnostic tests.

Bit	Function
7, 6	Number of diskette drives, other than physical drive 0
5, 4	Display operating mode
3, 2	Reserved
1	Math-coprocessor presence
0	Diskette drive 0 presence

Figure 3-23. Equipment Byte (Hex 014)

Bits 7, 6 These bits indicate the number of diskette drives that are installed, other than drive 0.

Bits 7 6	Number of Diskette Drives
0 0	No other drive
0 1	One other drive
1 0	Two other drives
1 1	Reserved

Figure 3-24. Installed Diskette Drive Bits

Bits 5, 4 These bits indicate the operating mode of the display that is attached to the video port.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-column mode
1 0	80-column mode
1 1	Monochrome mode

Figure 3-25. Display Operating Mode Bits

Bits 3, 2 These bits are reserved.

Bit 1 When this bit is set to 1, it indicates that a math coprocessor is installed.

Bit 0 When this bit is set to 1, it indicates that physical diskette drive 0 is installed.

Low and High Base-Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address.

The value of these bytes indicates the number of 1KB blocks of base memory. For example, hex 0280 indicates 640KB of base memory. The low byte is hex 015; the high byte is hex 016.

Low and High Expansion-Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address.

The value of these bytes indicates the number of 1KB blocks of expansion memory. For example, hex 0800 indicates 2048KB of expansion memory. The low byte is hex 017; the high byte is hex 018.

Reserved Bytes (Hex 019 – 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check (CRC) data for bytes hex 010 through 031 of the 64-byte CMOS RAM. The low byte is hex 033; the high byte is hex 032.

Reserved Byte (Hex 034): This byte is reserved.

Low and High Usable-Memory Bytes (Hex 035 and 036): These bytes define the total amount of contiguous memory from 1MB to 16MB.

The value of these bytes indicates the number of 1KB blocks of usable memory. For example, hex 0800 indicates 2408KB of

contiguous usable memory. The low byte is hex 035; the high byte is hex 036.

Date-Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the Interrupt 1AH section of the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 – 03F): These bytes are reserved.

Miscellaneous System Functions and Ports

This section contains information about nonmaskable interrupt, system control ports, power-on password, and selectable boot sequence.

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals to the system microprocessor that a parity error, a channel check, a system channel time-out, or a system watchdog time-out has occurred. The NMI (other than cache parity errors) stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts, and the IRET instruction restores the interrupt flag to the state it was in before the interrupt. A system reset causes a reset of the NMI.

NMI requests that are caused by channel checks and system board memory-parity errors are subject to mask control by the NMI-mask bit in the RT/CMOS Address and NMI Mask register. The watchdog timer, system channel time-out, and cache parity error are not masked by this bit. See "RT/CMOS Address and NMI Mask Register (Hex 0070)" on page 3-16. The power-on default of the NMI mask is 1 (NMI disabled). Before the NMI is enabled after a power-on reset, the parity-error and channel-check states are initialized by POST.

Warning: The operation that follows a write operation to this register must access address hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the write and read functions of this port are shown in the following figures.

Bit	Function
7	Reset timer 0 output latch (IRQ0)
6–4	Reserved
3	Enable channel check
2	Enable parity check
1	Enable speaker data
0	Timer 2 gate to speaker

Figure 3-26. System Control Port B (Hex 0061)—Write

Bit	Function
7	Parity check
6	Channel check
5	Timer 2 output
4	Toggles with each refresh request
3	Enable channel check
2	Enable parity check
1	Enable speaker data
0	Timer 2 gate to speaker

Figure 3-27. System Control Port B (Hex 0061)—Read

Bit 7 When this bit is set to 1 during a write operation, IRQ0 is reset. When this bit is read as a 1, it indicates that a parity check has occurred.

Bit 6 When this bit is read as a 1, it indicates that a channel check has occurred.

Bit 5 This bit reflects the state of the timer/counter 2 'output' signal.

Bit 4 This bit toggles for each refresh request.

Bit 3 When this bit is set to 0, channel check is enabled. It is set to 1 during a power-on reset.

Bit 2 When this bit is set to 0, parity check is enabled. It is set to 1 during a power-on reset.

Bit 1 When this bit is set to 1, speaker data is enabled.

Bit 0 When this bit is set to 1, the timer 2 gate is enabled.

System Control Port A (Hex 0092)

Bit	Function
7–5	Reserved
4	Watchdog-timer status
3	Security lock latch
2	Reserved
1	Alternative gate A20
0	Alternative hot reset

Figure 3-28. System Control Port A (Hex 0092)

Bits 7–5 These bits are reserved.

Bit 4 This read-only bit indicates the watchdog-timer status. When this bit is set to 1, a watchdog time-out has occurred. For more information about the watchdog timer, refer to the "System Timers" section of the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces.*

Bit 3 This bit provides the security lock for the secured area of RT/CMOS RAM. When this bit is set to 1, the 8-byte power-on password is electronically locked. After this bit is set by POST, it can be cleared only by turning the system off.

Bit 2 This bit is reserved.

Bit 1 This bit is ORed with bit 1 of the Keyboard Output port to enable the 'address 20' signal (A20). When both bits are set to 0, A20 is disabled and set to 0. This bit is set to 0 during POST. See the "Keyboard and Auxiliary Device Controller" section of the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces.*

Bit 0 This bit provides an alternative method of resetting the system microprocessor. This alternative method supports operating systems that require faster operation than was provided on the IBM Personal Computer AT*. Resetting the system microprocessor switches the microprocessor from the protected mode to the real-address mode. The alternative reset takes 13.4 microseconds.

* Trademark of the IBM Corporation.

This bit is set to 0 by either a system reset or a write operation. When a write operation changes this bit from 0 to 1, the alternative reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If this bit is set to 0, POST assumes that the system has just been powered-on. If this bit is set to 1, POST assumes that the microprocessor has been switched from the protected mode to the real mode.

When bit 0 is used to reset the system microprocessor to the real mode, the following procedure must be used:

1. Disable all maskable and nonmaskable interrupts.
2. Reset the system microprocessor by setting bit 0 to 1.
3. Issue a Halt instruction to the system microprocessor.
4. Reenable all maskable and nonmaskable interrupts.

If this procedure is not followed, the results will be unpredictable.

Note: Whenever possible, advanced BIOS (ABIOS) should be used as an interface to reset the system microprocessor to real mode. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for more information about ABIOS.

Power-On Password

Eight bytes of RT/CMOS RAM are reserved for the power-on password and the check character. The 8 bytes are initialized to hex 00. The microprocessor can access these bytes only during the power-on self-test (POST). After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by any program. During power-on password installation, the password, which is from 1 to 7 characters, is stored in the security space.

Installing the password is a function of a program on the System Partition of the hard disk. The power-on password does not appear on the screen when it is installed, changed, or removed. After the power-on password has been installed, it can be changed or removed only during POST.

The Model 77 also supports a keyboard password. See the "Keyboard and Auxiliary Device Controller" section in the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* for more information.

Selectable Boot Sequence

The selectable boot sequence allows the user to specify the order in which devices are searched when looking for the boot record of an operating system. Diskette drives, fixed disk drives, and remote program load (RPL) can be part of the search sequence. Changing the sequence for selectable boot affects the drive-letter assignment each time the system is reset (either a power-on reset or a soft reset).

The user selects the sequence by using a program on the System Partition of the hard disk. The selected sequence is stored in nonvolatile RAM (NVRAM). After the system is reset, it searches, in the specified sequence, for a device that contains a boot record.

After the operating system is booted, the drive lettering is determined by where the boot record was found and by the search sequence.

Note: Selectable boot sequence affects adapters that use initialization programs. See the "Setup" section of the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures* for more details.

Hardware Compatibility

The Model 77 maintains many of the interfaces that are used by earlier PS/2 products. In most cases, the command and status organization of these interfaces is maintained.

The functional interfaces for the Model 77 are compatible with the following interfaces:

- The Intel 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timer, driven at 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller-address/transfer counters, page registers and status fields only. The Command and Request registers and the Rotate and Mask functions are not supported. The Mode register is partially supported.

- The National Semiconductor** NS16450 serial communication controller.
- The Intel 8088, 8086, 80286, and 80386 microprocessors.
- The Intel 8272 diskette drive controller.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The keyboard interface at address hex 0060.
- Display modes that are supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in DOS mode.
- Generally compatible with the Intel 80387, 80287, and 8087 math coprocessors.

Error Codes

POST returns a message in the form of a multiple-character code to indicate the type of test that failed. Two formats are used for these error messages:

- A 12-character code for all errors that *are* related to SCSI devices:
  - The first 4 characters identify the device type.
  - The next 8 characters identify specifics of the error.
- An 8-character error code for all errors that *are not* related to SCSI devices.

The 8-character error code consists of two 4-character elements: the major error code and the minor error code. The following figure lists the failures and their associated error codes.

** National Semiconductor is a trademark of the National Semiconductor Corporation, and Motorola is a trademark of Motorola, Incorporated.

Major Code	Minor Code	Description
0001		System bus errors—system board or microprocessor
	0100	Unexpected interrupt
	0200	Timer failure
	0300	Timer-interrupt failure
	0400	Protected-mode failure
	0500	Last keyboard command not accepted
	0600	Converting logic test
	0700	NMI test failed
	0800	Timer bus test failed
	0900	Low MB chip-select test failed
	10*xx*	System board memory-parity error
	11*xx*	I/O channel check error
	1200	Watchdog time-out
	1300	Micro Channel-related bus time-out
	1400	Adapter ROM checksum error
	1500	ROM checksum error or DMA error
	1600	System board port read/write failure
	1800	System board parity or L2-cache error during previous power-on
	1900	Down-level diskette controller (2.88MB diskette drive not supported)
	2000	Microprocessor test error
	6000	System board ID not recognized
	6100	Dead battery
	6300	Clock not updating
	6400	Memory configuration error
	6500	Adapter ID mismatch
	6600	Adapter busy error
	6700	Clock not updating
	6900	Microprocessor configuration error
	7100	Rolling bit test failure on CMOS Shutdown Address byte
	7200	Rolling bit test failure on NVRAM Diagnostic byte
	7300	Bad CMOS/NVRAM checksum
	7400	Bad configuration
	7900	NVRAM error log full
0002		Memory errors
	0*xxx*	Memory error
	1*xxx*	Irrecoverable error in first 1MB
	2100	ROM-to-RAM remapping error
	25*xx*	Unsupported memory type installed or memory-pair mismatch
	3500	Stuck data line on memory module, microprocessor or system board

Figure 3-29 (Part 1 of 2). POST Error Messages

Major Code	Minor Code	Description
0003		Keyboard errors
	0100	Keyboard error
	0200	Keyboard locked
	0300	Keyboard-to-system-board interface error
	0400	Keyboard clock high
	0500	No keyboard +5 V dc
0006		Diskette drive errors
	0100	Diskette drive or controller error
	0200	Diskette IPL boot record not valid
	0400	Non-media sense
0011	0100	Async error
0017		Fixed disk drive errors
	8000	Fixed disk drive 0 failed
	8100	Fixed disk drive 1 failed
	8200	Disk controller error
	9000	Fixed disk drive 0 error
	9100	Fixed disk drive 1 error
0024	0100	System board video error
0086		Mouse errors
	0100	System-bus error—keyboard/pointing-device interface
	0200	Pointing-device error
	0300	Pointing-device or system-bus error
0096	xxxx	SCSI-adapter (with cache) failure
0112	xxxx	SCSI-adapter (without cache) failure
0208 to 0241	xxxx	SCSI-device test failure
1999		Special instruction codes
	00xx	Initial machine load (IML) error
	03xx	No boot device
	04xx	IML-to-system mismatch
	06xx	IML error

Figure 3-29 (Part 2 of 2). POST Error Messages

Index

Numerics

80486DX2 microprocessor 1-9, 1-10, 3-3
80486SX microprocessor 1-9, 1-10, 3-3
80487SX math coprocessor 3-3

A

A20 3-27
acoustical noise emission values 1-12
adapter
  bus extension 3-6
  enable/setup register 2-15
  setup 2-4
address 20 gate 3-27
address and NMI mask register, RT/CMOS 3-16
address map
  memory 3-13
  POS I/O 2-5
  RT/CMOS RAM 3-16
  system board I/O 1-6
alarm interrupt 3-19, 3-20
alternative reset 3-27
altitude 1-11
ARB/-GNT 3-4
arbiter programming 3-5
arbitration control point, central 3-5
arbitration levels 3-4
arbitration register 3-5
arbitration, extended 3-6
audio subsystem 1-4
auxiliary-device controller 1-5

B

base-memory bytes 3-24
battery 3-21
boot sequence, selectable 3-29
bus contention 2-3
bus extension 3-6
bus priority assignments 3-4

C

cables 1-11
cache map 3-13
cacheable memory 3-13
card selected feedback register 2-6
-CD SETUP 2-15
-CD SFDBK 2-6
CD-ROM 1-5
central arbitration control point 3-5
channel 3-3
  check enable 3-26
  check latch 3-26
  connector 3-6
  DMA 3-4
channel checks, synchronous 1-8
clock speed 1-3
clock, real-time 3-16, 3-18
CMOS RAM 1-4, 3-16—3-25
compatibility, hardware 3-29
compatibility, Micro Channel 1-8
configuration
  CRC bytes 3-24
  incorrect information 3-21
  RT/CMOS 3-21
connector
  channel 3-6
  diskette drive 3-7
  memory 3-8
  Micro Channel 1-5
  power supply 1-14
  SCSI device 3-9
contention, bus 2-3
control ports, system 3-26—3-27
controller
  diskette drive 1-5
  DMA 1-4

© Copyright IBM Corp. 1992

controller *(continued)*
interrupt 1-4
keyboard and auxiliary device 1-5
parallel 1-5
parallel port, arbitration level 2-11
SCSI 1-5
serial 1-5
coprocessor, math 1-5, 3-3, 3-24
current, electrical 1-11
currents, maximum load 1-13
cyclic-redundancy-check (CRC) bytes 3-24

D

data parity 1-8
data register, RT/CMOS 3-17
date status indicator 3-22
date-century byte 3-25
depth, system unit 1-11
diagnostic status byte (RT/CMOS) 3-21
dimensions, system unit 1-11
diskette drive
arbitration level 2-11
connectors 3-7
controller 1-5
controller, control of 2-8
number installed 3-23
type byte 3-22
diskette overruns 3-4
display operating mode 3-24
divider output frequency 3-19
DMA
channels 3-4
controller 1-4
performance 1-9, 1-10
support 1-8

E

enable NMI 3-16
equipment byte 3-23
error codes, POST 3-30
expansion-memory bytes 3-24
extended arbitration 3-6

F

failures and messages, POST 3-30
fault, overvoltage 1-14
feedback, card selected 2-6
figures
adapter enable/setup register 2-15
arbitration bus priority assignments 3-4
arbitration register—read 3-5
arbitration register—write 3-5
card selected feedback register 2-6
channel load current 1-13
component maximum current 1-13
declared acoustical noise emission values 1-12
devices supported in setup mode 2-7
diagnostic status byte 3-21
diskette drive connectors 3-7
diskette drive type byte 3-22
display operating mode bits 3-24
equipment byte 3-23
external SCSI-device connector pin assignments 3-10
first diskette drive type bits 3-22
installed diskette drive bits 3-23
internal SCSI-device connector pin assignments 3-9
memory map, cached regions—nonsystem memory from 8MB to 16MB 3-15
memory map, cached regions—system memory 3-14
model and submodel bytes 1-3
performance specifications—25 MHz 1-9
performance specifications—33 MHz 1-10
physical specifications 1-11

figures *(continued)*
POS I/O address map 2-5
presence-detect bits 3-12
real-time clock bytes 3-18
RT/CMOS address and NMI mask register 3-17
RT/CMOS address map 3-16
RT/CMOS data register 3-17
second diskette drive type bits 3-23
status register A 3-18
status register B 3-19
status register c 3-20
status register D 3-21
system board devices and features 1-4
system board enable/setup register 2-7
system board group 1 POS register 3—write 2-9
system board group 1 POS register 3—write, index 00 2-10
system board group 1 POS register 3—write, index 01 2-10
system board group 1 POS register 3—write, index 04 2-10
system board group 1 POS register 4 2-11
system board group 1 POS register 5 2-11
system board group 2 POS register 2 2-12
system board group 2 POS register 3 2-12
system board group 3 POS register 2 2-13
system board group 3 POS register 3 2-13
system board I/O address map 1-6
system board memory connectors 3-8
system board POS register 2 2-8
figures *(continued)*
system control port A 3-27
system control port B—read 3-26
system control port B—write 3-26
voltage assignments for power-supply connectors 1-14
fixed disk drive
initialization failed 3-22
type byte 3-23
frequency, input 1-11

G

gate A20 3-27

H

heat output 1-11
height, system unit 1-11
humidity 1-11

I

I/O
address map 1-6
RT/CMOS RAM operations 3-17
input frequency 1-11
input voltage 1-11
interleaved memory 3-12
interrupt
alarm 3-19, 3-20
controller 1-4
IRQ0 reset 3-26
NMI reset 3-25
periodic 3-19, 3-20
update-ended 3-19, 3-20
IRQ0 3-26

K

keyboard
cable 1-11
password 3-29

M

M-audio capture and playback adapter 2-3
math coprocessor 1-5, 3-3, 3-24
measurements, system unit 1-11
memory
  bytes 3-24
  cacheable 3-13
  CMOS RAM 1-4
  connectors 3-8
  control 3-12
  description 3-10
  interleaved 3-12
  noncacheable 3-13
  noninterleaved 3-12
  performance 1-9, 1-10
  presence determination 2-9, 3-12
  RAM 3-11
  RAM subsystem 1-4
  random access 3-11
  read operation 1-9, 1-10
  read-only 3-11
  refresh 3-4
  ROM 3-11
  ROM subsystem 1-4
  RT/CMOS RAM 3-16
  size miscompare 3-21
  write operation 1-9, 1-10
memory-presence detect signals 3-12
messages, POST error 3-30
Micro Channel architecture
  arbitration control point, central 3-5
  bus extension 3-6
  compatibility 1-8
  connectors 1-5
  general information 3-3
microprocessor
  80486DX2 3-3
  80486SX 3-3
  alternative reset 3-27
  burst cycles 3-12
  mode switch compatibility 3-27
  performance 1-9, 1-10
model byte 1-3
multimedia
  audio subsystem 1-4
  CD-ROM 1-5
  M-audio capture and playback adapter 2-3

N

NMI mask register 3-16
NMI service 3-4
NMI signal 3-4
noise emission 1-12
noncacheable memory 3-13
noninterleaved memory 3-12
nonmaskable interrupt (NMI) 3-25

O

operating-system boot sequence 3-29
output protection, power supply 1-14
output voltage 1-13
output voltage sequencing 1-14
outputs, power supply 1-13
overvoltage fault 1-14

P

page hit 1-9, 1-10
page miss 1-9, 1-10
parallel controller port 1-5
parallel port 1-5
parallel port controller, arbitration level 2-11
parallel port select 2-8
parallel port, control of 2-8
parity check enable 3-26
password
  keyboard 3-29
  power-on 3-27, 3-28
performance, system 1-9, 1-10
periodic interrupt 3-19, 3-20
port
  parallel 1-5
  serial 1-5

POS
See programmable option select (POS)
POST (power-on self-test) 3-11
POST error codes 3-30
power
cable 1-11
loss 3-21
specifications 1-11
power supply, description 1-12
power-on password 3-27, 3-28
power-on self-test (POST) 3-11
power-supply connectors 1-14
power-supply output protection 1-14
power-supply outputs 1-13
-PREEMPT 3-4
presence determination, memory 2-9
programmable option select (POS)
adapter enable/setup 2-15
address map 2-5
card selected feedback register 2-6
description 2-3
diskette drive 2-11
group 1, register 2 2-8
group 1, register 3 2-9
group 1, register 4 2-11
group 1, register 5 2-11
group 2, register 2 2-12
group 2, register 3 2-12
group 3, register 2 2-13
group 3, register 3 2-13
I/O address map 2-5
memory information 2-9
parallel port controller 2-11
register groups 2-6
SCSI controller, enable 2-13
SCSI ID selection 2-13
setup procedures 2-4
system board enable/setup register 2-7
system board groups 2-4
system board serial port address 2-12
system board serial port, enable 2-12
programmable option select (POS) *(continued)*
system board setup 2-6
system configuration utility programs 2-3
warning 2-3
programming, arbiter 3-5
protected mode, switch from 3-27
protection, power supply 1-14

R

RAM (random access memory) 3-11
RAM subsystem 1-4
random access memory (RAM) 3-11
read-only memory (ROM) 3-11
real mode, switch to 3-27
real-time clock 3-16, 3-18, 3-21
refresh request 1-9, 1-10, 3-26
register
adapter enable/setup 2-15
arbitration 3-5
card selected feedback 2-6
group 1 POS register 2 2-8
group 1 POS register 3 2-9
group 1 POS register 4 2-11
group 1 POS register 5 2-11
group 2 POS register 2 2-12
group 2 POS register 3 2-12
group 3 POS register 2 2-13
group 3 POS register 3 2-13
miscellaneous system 3-25
RT/CMOS address and NMI mask 3-16
RT/CMOS data 3-17
RT/CMOS status 3-18—3-21
system board enable/setup 2-7
system board POS 2-5
system control port B 3-26
reserved, definition ix
reset, alternative 3-27
ROM (read-only memory) 3-11
ROM subsystem 1-4
RT/CMOS RAM
address and NMI mask register 3-16

RT/CMOS RAM *(continued)*
address map 3-16
configuration bytes 3-21
data register 3-17
description 3-16
diagnostic status byte 3-21
I/O operations 3-17
power-on password 3-28
reading from 3-18
secured area 3-27
status registers 3-18—3-21
writing to 3-17

S

SCSI controller 1-5
SCSI controller, enable 2-13
SCSI ID selection 2-13
SCSI-device connector 3-9
selectable boot sequence 3-29
selected feedback return 1-8
sequencing, output voltage 1-14
serial controller port 1-5
serial port 1-5
serial port address 2-12
serial port, enable 2-12
set configuration 3-29
setup
bus contention 2-3
POS procedures 2-4
system board 2-6
shutdown status byte 3-22
signal
address 20 3-27
arbitrate/-grant 3-4
audio sum node 1-4
-card selected feedback 2-6
-card setup 2-15
channel reset 2-15
-ECC memory 2-9, 3-8
NMI 3-4
output 3-26
-preempt 3-4
presence detect 0—3 2-9, 3-8, 3-12
selected feedback return 1-8
setup 2-4
size, system unit 1-11
speaker data enable 3-26
specifications
performance 1-9, 1-10
physical 1-11
speed, clock 1-3
square-wave frequency 3-20
startup sequence 3-29
status registers
(RT/CMOS) 3-18—3-21
streaming data 1-8
submodel byte 1-3
synchronous channel checks 1-8
system
clock speed 1-3
configuration utility programs 2-3
control ports 3-26—3-27
description 1-3
functions, miscellaneous 3-25
performance 1-9, 1-10
reset 3-25
specifications 1-11
timers 1-4
system board
address map 1-6
enable/setup register 2-7
group 1 POS register 2 2-8
group 1 POS register 4 2-11
group 1 POS register 5 2-11
group 2 POS register 2 2-12
group 2 POS register 3 2-12
group 3 POS register 2 2-13
group 3 POS register 3 2-13
memory connectors 3-8
POS I/O address map 2-5
SCSI controller, enable 2-13
SCSI ID selection 2-13
SCSI-device connector 3-9
serial port address 2-12
serial port, enable 2-12
setup 2-4, 2-6

T

temperature 1-11
time status indicator 3-22
time-and-date updates 3-20
time-base frequency 3-19
time-update cycle 3-19
timers, system 1-4

U

update-ended interrupt 3-19, 3-20
usable-memory bytes 3-24

V

video subsystem 1-5
voltage, input 1-11
voltage, output 1-13

W

warning
  central arbiter 3-5
  NMI 3-25
  POS 2-3
  reserved areas ix
  RT/CMOS 3-16
  RT/CMOS RAM I/O
    operations 3-17
watchdog-timer status 3-27
weight, system unit 1-11
width, system unit 1-11

X

XGA-2 video 1-5

Personal System/2
Model 80
Technical Reference

Third Edition (October 1990)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer of express or implied warranties in certain transactions, therefore, this statement may not apply to you.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Requests for technical information about IBM products should be made to your IBM Authorized Dealer or your IBM Marketing Representative.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

© Copyright International Business Machines Corporation 1989, 1990. All rights reserved.

Note to U.S. Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Special Notices

References in this publication to IBM products, programs, or services do not imply that IBM intends to make these available in all countries in which IBM operates. Any reference to an IBM product, program or service is not intended to state or imply that only IBM's product, program, or service may be used. Any functionally equivalent product, program, or service that does not infringe any of IBM's intellectual property rights or other legally protectible rights may be used instead of the IBM product, program, or service. Evaluation and verification of operation in conjunction with other products, programs, or services, except those expressly designated by IBM, are the user's responsibility.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

The following terms, denoted by an asterisk (*) in this publication, are trademarks of the IBM Corporation in the United States and/or other countries:

IBM
Micro Channel
Personal Computer AT
Personal System/2
PS/2

The following terms, denoted by a double asterisk (**) in this publication, are trademarks of other companies as follows:

Intel	Intel Corporation
Motorola	Motorola, Incorporated

Preface

This technical reference contains hardware and software interface information specific to the IBM Personal System/2 Model 80 computer. It is intended for those who develop hardware and software products for these systems. Users should understand computer architecture and programming concepts.

This publication consists of the following sections:

- Section 1, "System Overview," describes the system, features and specifications.
- Section 2, "Programmable Option Select," describes registers used for configuration.
- Section 3, "System Board," describes the system specific hardware implementations.

This technical reference should be used with the following publications:

- *IBM Personal System/2 Hardware Interface Technical Reference — Architectures*
- *IBM Personal System/2 Hardware Interface Technical Reference — Common Interfaces*
- *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*

Warning: The term "Reserved" describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

© Copyright IBM Corp. 1989, 1990

Notes:

Contents

Section 1. System Overview 1-1
Description 1-3
System Board Features 1-3
System Board I/O Address Map 1-6
Specifications 1-7
Power Supply 1-12
Outputs 1-12
Output Protection 1-13
Voltage Sequencing 1-13
Power Supply Connectors 1-14

Section 2. Programmable Option Select 2-1
Description 2-3
POS Address Map 2-5
Card Selected Feedback 2-5
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-6
System Board POS Register 2 (Hex 0102) 2-7
System Board POS Register 3 (Hex 0103) – Type 1 2-8
System Board POS Register 3 (Hex 0103) – Type 2 2-10
System Board POS Register 3 (Hex 0103) – Type 3 2-11
System Board POS Register 4 (Hex 0104) – Type 3 2-13
Adapter Enable/Setup Register (Hex 0096) 2-13

Section 3. System Board 3-1
Description 3-3
80387 Math Coprocessor 3-3
Micro Channel Implementation 3-3
Exception Reporting 3-3
Matched Memory 3-3
Central Arbiter 3-9
Memory 3-12
Read-Only Memory Subsystem – Type 1 3-12
Read-Only Memory Subsystem – Type 2 and Type 3 3-12
Random Access Memory Subsystem 3-12
System and Nonsystem Memory 3-13
Memory Caching 3-13
Error Recovery 3-15
Memory Subsystem Control 3-16
Memory Registers – Type 1 3-16
Memory Registers – Type 2 3-20
Memory Registers – Type 3 3-23

© Copyright IBM Corp. 1989, 1990

System Memory Maps 3-26
System Board Memory Connectors 3-33
Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM 3-36
Miscellaneous System Functions 3-47
Nonmaskable Interrupt 3-47
System Control Port B (Hex 0061) 3-47
System Control Port A (Hex 0092) 3-49
Power-On Password 3-51
Hardware Compatibility 3-51
Error Codes 3-52

Index X-1

Figures

1-1. Model and Submodel Bytes 1-3
1-2. System Board Devices and Features—Type 1 and Type 2 1-4
1-3. System Board Devices and Features—Type 3 1-5
1-4. System Board I/O Address Map 1-6
1-5. Performance Specifications—Type 1 1-7
1-6. Performance Specifications—Type 2 1-8
1-7. Performance Specifications—Type 3 1-9
1-8. Physical Specifications 1-10
1-9. Acoustical Readings 1-11
1-10. Component Maximum Current 1-12
1-11. Channel Load Current 1-12
1-12. Voltage Assignments for the Internal Drive Power-Supply Connectors 1-14
2-1. POS I/O Address Map 2-5
2-2. Card Selected Feedback Register (Hex 0091) 2-5
2-3. System Board Enable/Setup Register (Hex 0094) 2-6
2-4. System Board POS Register 2 (Hex 0102) 2-7
2-5. Parallel Port Select Bits 2-8
2-6. System Board POS Register 3 (Hex 0103)—Type 1 2-9
2-7. POS Register 3 (Bits 3, 2)—Type 1 2-9
2-8. POS Register 3 (Bits 1, 0)—Type 1 2-9
2-9. POS Register 3 (Hex 0103)—Type 2 2-10
2-10. POS Register 3 (Bits 3, 2)—Type 2 2-10
2-11. R1 and T1 Bit Values—Type 2 2-11
2-12. System Board POS Register 3 (Hex 0103)—Type 3 . . . 2-11
2-13. POS Register 3 (Bits 6, 3)—Type 3 2-12
2-14. POS Register 3 (Bits 6, 3)—Type 3 2-12
2-15. System Board POS Register 4 (Hex 0104)—Type 3 . . . 2-13
2-16. Adapter Enable/Setup Register (Hex 0096) 2-13
3-1. Matched-Memory Extension Voltage and Signal Assignments 3-4
3-2. Matched Memory Cycle (No Waits) 3-8
3-3. Arbitration Bus Priority Assignments 3-9
3-4. Arbitration Register, Write to Hex 0090 3-10
3-5. Arbitration Register, Read Hex 0090 3-10
3-6. Mapping of the First 32MB Segment 3-14
3-7. Memory Error Address Reassignment 3-15
3-8. Memory Enable Bits (Connector 2) 3-17
3-9. Memory Enable Bits (Connector 1) 3-17
3-10. Memory Encoding Register (Bits 5 and 4)—Type 1 . . . 3-17
3-11. Memory Encoding—Type 1 3-19

© Copyright IBM Corp. 1989, 1990

3-12. Split Address Register 3-19
3-13. Memory Encoding Register 1—Type 2 3-20
3-14. Memory Enable Bits—Type 2 3-20
3-15. Memory Encoding Register 1 (Bits 3 and 1) 3-21
3-16. Memory Encoding Register 2—Type 2 3-22
3-17. Memory Encoding Register 2 (Bits 5 and 4)—Type 2 . 3-22
3-18. Memory Encoding Register 1 (Hex 00E1) 3-23
3-19. Memory Encoding Register 2 (Hex 00E0) 3-25
3-20. Memory Encoding Register 3 (Hex 00E2 3-25
3-21. System Memory Map 1—Type 1, Type 2, and Type 3 . 3-27
3-22. System Memory Map 2—Type 1, Type 2, and Type 3 . 3-27
3-23. System Memory Map 3—Type 1 3-28
3-24. System Memory Map 3—Type 2 and Type 3 3-28
3-25. System Memory Map 4—Type 1 3-29
3-26. System Memory Map 4—Type 2 and Type 3 3-29
3-27. System Memory Map 5—Type 1 3-30
3-28. System Memory Map 5—Type 2 and Type 3 3-30
3-29. System Memory Map 6—Type 1 3-31
3-30. System Memory Map 6—Type 2 and Type 3 3-31
3-31. System Memory Map 7—Type 2 and Type 3 3-32
3-32. System Memory Map 8—Type 2 and Type 3 3-32
3-33. System Board Memory Connector Pin Locations 3-33
3-34. System Board Memory Connector 3-35
3-35. RT/CMOS RAM Address Map 3-36
3-36. RT/CMOS Address Register and NMI Mask (Hex 0070) 3-37
3-37. RT/CMOS Data Register (Hex 0071) 3-37
3-38. Real-Time Clock Bytes 3-39
3-39. Status Register A 3-39
3-40. Status Register B 3-40
3-41. Status Register C 3-41
3-42. Status Register D 3-41
3-43. Diagnostic Status Byte 3-42
3-44. Diskette Drive Type Byte 3-43
3-45. Diskette Drive Type Byte (Bits 7 - 4) 3-43
3-46. Diskette Drive Type Byte (Bits 3 - 0) 3-44
3-47. Equipment Byte 3-45
3-48. Equipment Byte (Bits 7, 6) 3-45
3-49. Equipment Byte (Bits 5, 4) 3-45
3-50. System Control Port B (Write) 3-48
3-51. System Control Port B (Read) 3-48
3-52. System Control Port A 3-49
3-53. Error Codes 3-52

Section 1. System Overview

Description 1-3
System Board Features 1-3
System Board I/O Address Map 1-6
Specifications 1-7
| Power Supply 1-12
| Outputs 1-12
| Output Protection 1-13
| Voltage Sequencing 1-13
| Power Supply Connectors 1-14

© Copyright IBM Corp. 1989, 1990

Notes:

Description

The IBM* Personal System/2* Model 80 is a self-contained, floor-standing computer that features the Micro Channel* architecture. It comes with a keyboard, and can support two internal diskette drives, two internal fixed disk drives, and a tape drive, or CD-ROM.

A system can have either a Type 1, Type 2, or Type 3 system board. The major differences among the three system boards are system clock speed, component layout, and memory. In addition, the Type 3 system board:

- Uses a two-way, set-associative, store-through, 64KB (KB = 1024 bytes) cache for instructions and data
- Has two connectors for system board memory.

Programs identify the type of system board by reading the model and submodel bytes. Interrupt hex 15, function code (AH) = hex C0, returns the model and submodel bytes. The following table shows these bytes, system board types, and system clock speeds.

Model Byte	Submodel Byte	System Board	System Clock
F8	00	Type 1	16 MHz
F8	01	Type 2	20 MHz
F8	80	Type 3	25 MHz

Figure 1-1. Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems, and check the supplements section for updates to that listing.

System Board Features

The following tables list the system board devices and features. The Hardware Interface Technical Reference manuals describes devices common to PS/2* products by type number.

* IBM, Personal System/2, PS/2, and Micro Channel are trademarks of the International Business Machines Corporation.

Device	Type	Features
Microprocessor	—	80386 32-bit address and 32-bit data interface
System Timers	1	Channel 0 — System timer Channel 2 — Tone generation for speaker Channel 3 — Watchdog timer
ROM Subsystem	—	128KB (KB = 1024 bytes)
RAM Subsystem	—	Type 1 system board, 1 or 2MB (MB = 1,048,576 bytes) Type 2 system board, 2 or 4MB Expandable on the channel
CMOS RAM Subsystem	—	64-byte CMOS RAM with real-time clock/calendar 2KB CMOS RAM extension Battery backup
Video Subsystem	1	Auxiliary connector on the channel Analog output 256KB video memory
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal.
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	1	Supports: - 720KB formatted diskette density - 1.44MB formatted diskette density.
Serial Controller	1, 2	RS-232C interface Programmable as serial port 1 or 2 FIFO mode[1] and character mode
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output
Micro Channel	—	Eight channel connectors for Type 3 adapters: - Three 32-bit connectors with a matched-memory extension - Five 16-bit connectors: - One with a video extension - One occupied by the fixed disk drive adapter
Math Coprocessor Socket	—	Supports 80387 math coprocessor Same clock speed as the system microprocessor

[1] The FIFO mode is supported only by the Type 2 serial controller

Figure 1-2. System Board Devices and Features — Type 1 and Type 2

Device	Type	Features
Microprocessor	—	80386 32-bit address and 32-bit data interface
Cache Controller	—	82385 64KB of static-RAM cache
System Timers	1	Channel 0 — System timer Channel 2 — Tone generation for speaker Channel 3 — Watchdog timer
ROM Subsystem	—	128KB
RAM Subsystem	—	4 or 8MB Expandable on the channel
CMOS RAM Subsystem	—	64-byte CMOS RAM with real-time clock/calendar 2KB CMOS RAM extension Battery backup
Video Subsystem	1	Auxiliary connector on the channel Analog output 256KB video memory
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal.
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	1	Supports: - 720KB formatted diskette density - 1.44MB formatted diskette density.
Serial Controller	2	RS-232C interface Programmable as serial port 1 or 2 FIFO mode and character mode
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output Supports DMA operations
Micro Channel	—	Eight channel connectors for Type 3 adapters: - Four 32-bit connectors with matched-memory extension. - Four 16-bit connectors: - Two with video extension - One occupied by fixed disk adapter.
Math Coprocessor Socket	—	Supports 80387 math coprocessor Same clock speed as the system microprocessor

Figure 1-3. System Board Devices and Features — Type 3

System Board I/O Address Map

Hex Addresses	Device
0000 - 001F	DMA Controller (0–3)
0020, 0021	Interrupt Controller (Master)
0040, 0042 - 0044, 0047	System Timers
0060	Keyboard, Auxiliary Device
0061	System Control Port B
0064	Keyboard, Auxiliary Device
0070, 0071	RT/CMOS and NMI Mask
0081 - 0083, 0087	DMA Page Registers (0–3)
0089 - 008B, 008F	DMA Page Registers (4–7)
0090	Central Arbitration Control Point
0091	Card Selected Feedback Register
0092	System Control Port A
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
00A0 - 00A1	Interrupt Controller (Slave)
00C0 - 00DF	DMA Controller (4–7)
00E0 - 00E2	Memory Encoding Registers
00F0 - 00FF	Math Coprocessor
0100 - 0107	Programmable Option Select
01F0 - 01F8	Fixed Disk Drive Controller
0278 - 027B	Parallel Port 3
02F8 - 02FF	Serial Port 2 (RS-232C)
0378 - 037B	Parallel Port 2
03B4, 03B5, 03BA	Video Subsystem
03BC - 03BF	Parallel Port 1
03C0 - 03C5	Video Subsystem
03C6 - 03C9	Video DAC
03CA, 03CC, 03CE, 03CF	Video Subsystem
03D4, 03D5, 03DA	Video Subsystem
03F0 - 03F7	Diskette Drive Controller
03F8 - 03FF	Serial Port 1 (RS-232C)

Figure 1-4. System Board I/O Address Map

Specifications

Device	Number of Waits	Cycle Time (ns)
Microprocessor (16 MHz – 62.5 ns Clock):		
Access to System Board RAM	1	187.5
Access to System Board ROM	1	187.5
Access to Channel:		
Default Transfer Cycle	2	250
Synchronous Extended Transfer Cycle	4	375
Refresh Rate (Typically performed every 15.1 μs)		625 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (8 MHz – 125 ns Clock):		
Single Transfer: 375 + I/O Access + Memory Access		
Burst Transfers: 375 + (I/O Access + Memory Access)N *		
System Board Memory Access		375
Default Transfer Cycle		250
Synchronous Extended Transfer Cycle		375

* N is the number of transfers in the burst.

Figure 1-5. Performance Specifications – Type 1

Device	Number of Waits	Cycle Time (ns)
Microprocessor (20 MHz – 50 ns Clock):		
Access to System Board RAM: *		
Memory Read (Page Hit)	0	100
Memory Read (Page Miss)	2	200
Memory Write (Page Hit)	1	150
Memory Write (Page Miss)	2	200
Access to Channel:		
Default Transfer Cycle	2	200
Synchronous Extended Transfer Cycle	4	300
Refresh Rate (Typically performed every 15.1 μs)		500 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer: 300 + I/O Access + Memory Access		
Burst Transfers: 300 + (I/O Access + Memory Access)N **		
System Board Memory Access		300
Default Transfer Cycle		200
Synchronous Extended Transfer Cycle		300

* Adapters installed in the channel should not rely on monitoring system board memory accesses because channel memory control signals may not be present during these accesses.

** N is the number of transfers in the burst.

Figure 1-6. Performance Specifications – Type 2

Device	Number of Waits	Cycle Time (ns)
Microprocessor (25 MHz – 40 ns Clock):		
Access to System Board RAM: *		
Memory Read (Cache Hit)	0	80
Memory Write (Cache Hit)	0	80**
Memory Read (Cache Miss, Page Hit)	0 - 2	80 - 160
Memory Write (Cache Miss, Page Hit)	0	80**
Memory Read (Cache Miss, Page Miss)	3 - 5	200 - 280
Memory Write (Cache Miss, Page Miss)	0	80**
Access to Channel:		
Default Transfer Cycle	4	240
Synchronous Extended Transfer Cycle	7	360
Refresh Rate (Typically performed every 15.1 μs)		600 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer: 300 + I/O Access + Memory Access		
Burst Transfers: 300 + (I/O Access + Memory Access)N ***		
System Board Memory Access		300
Default Transfer Cycle		200
Synchronous Extended Transfer Cycle		300

* Adapters installed in the channel should not rely on monitoring system board memory accesses because channel memory control signals may not be present during these accesses.

** The Write operation is buffered outside the microprocessor. Additional time is required if a Cache Read Miss or another Write operation occurs before the Write operation is completed.

*** N is the number of transfers in the burst.

Figure 1-7. Performance Specifications – Type 3

Size:	
Width	165 mm (6.5 in)
Width (feet extended)	318 mm (12.5 in)
Depth	483 mm (19.0 in)
Height	597 mm (23.5 in)
Weight (with one fixed disk drive)	20.6 kg (45.3 lb)
Cables:	
Power Cable	1.8 m (6 ft)
Keyboard Cable	3.05 m (10 ft)
Air Temperature:	
System On	15.6 to 32.2°C (60 to 90°F)
System Off	10.0 to 43.0°C (50 to 110°F)
Humidity:	
System On	8% to 80%
System Off	8% to 80%
Maximum Altitude	2133.6 m (7000 ft)
Heat Output:	
225 Watt	350 Watts/hour (1200 BTUs/hour)
242 Watt	375 Watts/hour (1280 BTUs/hour)
250 Watt	390 Watts/hour (1330 BTUs/hour)
Acoustical Readings	(See Figure 1-9 on page 1-11)
Electrical Input:	
Input Voltage (Range is automatically selected; sinewave input is required):	
Low Range	90 (min) – 137 (max) Vac
High Range	180 (min) – 265 (max)Vac
Frequency:	
Low Range	47 (min) – 53 (max) Hz
High Range	57 (min) – 63 (max) Hz
Input in Kilovolt-Ampere (kVA):	
Minimum configuration (as shipped by IBM)	0.18 kVA
Maximum configuration:	
225 Watt Power Supply	0.58 kVA
242 Watt Power Supply	0.62
250 Watt Power Supply	0.65 kVA
Electromagnetic Compatibility	
FCC Class B	

Figure 1-8. Physical Specifications

Description	L_{WAd} in bels Operation	Idle	L_{pAm} in dB Operation	Idle	$<L_{pA}>_m$ in dB Operation	Idle
Model 80	5.3	5.3	43	43	40	40

Notes

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

All measurements made in accordance with ANSI S12.10, and reported in conformance with ISO DIS 9296.

The measurements are preliminary data and subject to change.

Figure 1-9. Acoustical Readings

Power Supply

The power supply requires a sinewave input and converts the ac input voltage to three dc output voltages. The power supply provides power for the following:

- System board
- Channel adapters
- Internal diskette drives
- Internal fixed disk drives
- Auxiliary device
- Keyboard.

The power switch and one light-emitting diode (LED) is on the front of the system unit. The power supply is operating when the LED is lit.

Outputs

The power supply provides separate voltage sources for the system board and the drives. The system-board voltages are +5 Vdc, +12 Vdc, and −12 Vdc. The drive voltages are +5 Vdc and +12 Vdc. The following is a list of the approximate power provided for system components.

System Component	Maximum Current	
	+12 Vdc	+5 Vdc
Internal Fixed Disk Drives (per power supply connector)	2.5 A	1.5 A
Auxiliary Device	None	300 mA
Keyboard	None	275 mA

Figure 1-10. Component Maximum Current

The following are the load currents allowed for each channel connector.

Supply Voltage	16-Bit Connector Maximum Current	32-Bit Connector Maximum Current
+ 5.0 Vdc	1.6 A	2.0 A
+12.0 Vdc	0.175 A	0.175 A
−12.0 Vdc	0.040 A	0.040 A

Figure 1-11. Channel Load Current

The formulas used to determine the power requirements and the voltage regulation tolerances are in the Micro Channel adapter

| design information in the *Hardware Interface Technical Reference - Architectures* manual.

Output Protection

A short circuit placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state with no damage to the power supply.

If an overvoltage fault occurs (internal to the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of its nominal value.

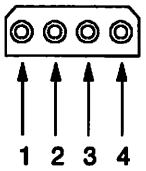
If either of these shutdown states is actuated, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least ten seconds.

Voltage Sequencing

At power-on time, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Power Supply Connectors

The power supply provides two 4-pin connectors for internal fixed disk drives. This connector can be extended to provide power to more than one internal drive as long as the total power does not exceed the connector specifications shown in Figure 1-10 on page 1-12.



Pin	Signal
1	+12 Vdc
2	DC Return
3	DC Return
4	+5 Vdc

Figure 1-12. Voltage Assignments for the Internal Drive Power-Supply Connectors

Section 2. Programmable Option Select

Description 2-3
POS Address Map 2-5
Card Selected Feedback 2-5
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-6
System Board POS Register 2 (Hex 0102) 2-7
System Board POS Register 3 (Hex 0103) – Type 1 2-8
System Board POS Register 3 (Hex 0103) – Type 2 2-10
System Board POS Register 3 (Hex 0103) – Type 3 2-11
System Board POS Register 4 (Hex 0104) – Type 3 2-13
Adapter Enable/Setup Register (Hex 0096) 2-13

© Copyright IBM Corp. 1989, 1990

Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used on the Model 80 system boards.

Warning:

- IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignment of the same system resource, improper operation of the feature, loss of data, or possible damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention will occur, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- Bit 7 (channel reset) in the Adapter Enable/Setup register must be set to 0 to program the adapters.
- Only 8-bit instructions are supported for setup operations. Using 32- or 16-bit I/O instructions on 8-bit POS registers will cause erroneous data to be written or read.

Setup functions respond to I/O addresses, hex 0100 through 0107, only when their unique setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

System Board Video Subsystem Setup:

- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 0 to place the system board video into the setup mode.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 7 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system board functions.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register must be set to 1 to allow adapter setup.
- Bit 5 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the Video Subsystem.
- Bit 7 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to a system board function.

Other System Board Setup:

- Bit 7 in the System Board Enable/Setup register must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 5 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the Video Subsystem.

POS Address Map

The following table shows the organization of the I/O address space used by POS. Bit 0 of POS Register 2 and bits 6 and 7 of POS Register 5 are fixed. All other bits in POS Registers 2 through 5 are free-form.

Address (Hex)	Function
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
0100	POS Register 0—Adapter Identification Byte (Low Byte)
0101	POS Register 1—Adapter Identification Byte (High Byte)
0102	POS Register 2—Option Select Data Byte 1 Bit 0 is Card Enable.
0103	POS Register 3—Option Select Data Byte 2
0104	POS Register 4—Option Select Data Byte 3
0105	POS Register 5—Option Select Data Byte 4 Bit 7 is the channel check active indicator Bit 6 is the channel check status-available indicator
0106	POS Register 6—Reserved
0107	POS Register 7—Reserved

Figure 2-1. POS I/O Address Map

Card Selected Feedback

When an adapter is addressed, it responds by setting the '-card selected feedback' signal (-CD SFDBK) to active. -CD SFDBK is derived from the address decode and driven by a totem pole driver. It is latched by the system board and can be read through the Card Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and thereby determine if the video subsystem, system board I/O, or an adapter is addressed and functioning.

Bit	Function
7 - 1	Reserved
0	-Card Selected Feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7 - 1 These bits are reserved.

Bit 0 This bit is set to 1 whenever -CD SFDBK was active on a previous cycle, or whenever the system board I/O functions (diskette drive, serial, or parallel interfaces) are accessed by an I/O cycle. Reading this register resets the bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information during setup. The diskette drive controller, serial port, and parallel port are treated as a single device. The video subsystem is also an integrated part of the system board; however, POS treats it as a separate device. The System Board Enable/Setup register is used to place the system board or the video subsystem into the setup mode.

System Board Enable/Setup Register (Hex 0094)

This is a read/write register; all bits in this register default to 1 (enabled).

Bit	Function
7	Enable/-Setup System Board Functions
6	Reserved
5	Enable/-Setup Video Subsystem
4 - 0	Reserved

Figure 2-3. System Board Enable/Setup Register (Hex 0094)

Bit 7 When this bit is set to 0, various system board I/O functions are placed in the setup mode. The diskette drive controller, serial port, and parallel port are controlled through System Board POS Register 2 (hex 0102).

When this bit is set to 1, the system board function is enabled.

Bit 6 This bit is reserved.

Bit 5 When this bit is set to 0, the video subsystem is placed in the setup mode and controlled through POS Register 2 (hex 0102). When set to 1, and bit 0 in hex 0102 is set to 1, video is enabled.

Bit 0 of POS Register 2 is the video enable bit. When this bit is set to 0, the video subsystem does not respond to commands, addresses, or data. If video is being generated when the video enable bit is set to 0, the output is still generated. For information on BIOS calls to enable or disable the video, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Note: When video is disabled, access to the video DAC registers is disabled.

Bits 4 - 0 These bits are reserved.

System Board POS Register 2 (Hex 0102)

When the system board is in the setup mode, the diskette drive controller, serial port, and parallel port are controlled by this read/write register. Reading this register returns the current state of these system board functions.

Bit	Function
7	Disable Parallel Port Extended Mode
6, 5	Parallel Port Select
4	Enable Parallel Port
3	Serial Port Select
2	Enable Serial Port
1	Enable Diskette Drive Interface
0	Enable System Board

Figure 2-4. System Board POS Register 2 (Hex 0102)

Bit 7 When set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional interface. When set to 1, this bit disables the bidirectional mode. This bit is set to 0 at power on. The Type 1 and Type 2 system-boards POST sets it to 1, and the Type 3 system-board POST sets it to 0.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Hex Address	Interrupt Level
0 0	Parallel 1	03BC - 03BF	7
0 1	Parallel 2	0378 - 037B	7
1 0	Parallel 3	0278 - 027B	7
1 1	Reserved	----------	-

Figure 2-5. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bit 3 When set to 1, this bit sets the system board serial port as Serial 1 (addresses hex 03F8 through 03FF), which uses interrupt level 4. When set to 0, this bit sets the serial port as Serial 2 (addresses hex 02F8 through 02FF), which uses interrupt level 3.

Bit 2 When this bit and bit 0 are set to 1, the system board serial port is enabled.

Bit 1 When this bit and bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When set to 1, this bit allows bits 4, 2, and 1 to enable and disable their respective devices. When set to 0, this bit disables the diskette drive interface, system board serial port, and system board parallel port, regardless of the state of bits 4, 2, and 1.

System Board POS Register 3 (Hex 0103) – Type 1

This read-only register is accessed while the system board is in the setup mode. It contains information about the presence and type of memory card installed in each system board connector. Connector 1 is closest to the power supply; connector 2 is furthest from the power supply.

Note: The Type 1 system board supports one or two 1MB memory cards.[1]

Bit	Function
7 - 4	Reserved
3	-1MB Memory Card in Connector 2
2	-Memory Card Present in Connector 2
1	-1MB Memory Card in Connector 1
0	-Memory Card Present in Connector 1

Figure 2-6. System Board POS Register 3 (Hex 0103) — Type 1

Bits 7 - 4 Reserved.

Bits 3, 2 These bits indicate if memory is installed in memory connector 2 as shown in the following table.

Bits 3 2	Available RAM
0 0	1MB Memory Card in Connector 2
0 1	Reserved
1 0	Reserved
1 1	No Memory Card in Connector 2

Figure 2-7. POS Register 3 (Bits 3, 2) — Type 1

Bits 1, 0 These bits indicate if memory is installed in memory connector 1 as shown in the following table.

Bits 1 0	Available RAM
0 0	1MB Memory Card in Connector 1
0 1	Reserved
1 0	Reserved
1 1	No Memory Card in Connector 1

Figure 2-8. POS Register 3 (Bits 1, 0) — Type 1

Additional registers at address hex 00E0 and 00E1 are used during setup to define how memory is used. See "Random Access Memory Subsystem" on page 3-12 for more information.

1 80386 System Board Memory Expansion Kit.

System Board POS Register 3 (Hex 0103) – Type 2

This read-only register is accessed while the system board is in the setup mode. It contains information about the presence and type of memory card installed in each system board connector. Connector 1 is closest to the power supply; connector 2 is furthest from the power supply.

Note: The Type 2 system board supports one or two 2MB memory cards.[2]

Bit	Function
7 - 4	Reserved
3	2MB Memory Card, Connector 2 (T Signal)
2	-Memory Card Present, Connector 2 (R Signal)
1	2MB Memory Card, Connector 1 (T Signal)
0	-Memory Card Present, Connector 1 (R Signal)

Figure 2-9. POS Register 3 (Hex 0103) – Type 2

Bits 7, 4 These bits are reserved.

Bits 3, 2 These bits indicate if memory is installed in memory connector 2 as shown in the following table.

Bits 3 2	Available RAM
0 0	Reserved
0 1	Reserved
1 0	2MB Memory Card in Connector 2
1 1	No Memory Card in Connector 2

Figure 2-10. POS Register 3 (Bits 3, 2) – Type 2

Bits 1, 0 These bits indicate if memory is installed in memory connector 1 as shown in the following table.

[2] 80386 System Board 2MB Memory Expansion Kit

Bits 1 0	Available RAM
0 0	Reserved
0 1	Reserved
1 0	2MB Memory Card in Connector 1
1 1	Invalid (At Least 1MB Must Be Available in Connector 1)

Figure 2-11. R1 and T1 Bit Values — Type 2

Additional registers at address hex 00E0 and 00E1 are used during setup to define how memory is used. See "Random Access Memory Subsystem" on page 3-12 for more information.

System Board POS Register 3 (Hex 0103) — Type 3

On the Type 3 system board, two read-only registers, POS Register 3 and 4, contain information about the type of memory on the Type 3 system board. The Type 3 system board only supports 80 nanosecond memory cards. The memory connectors are numbered from left to right as viewed from the front of the system. (See Figure 3-34 on page 3-35 for information on the signals.)

Bit	Function
7	Reserved
6	Memory Connector 2 (T2 signal)
5	Memory Connector 1 (T2 signal)
4	Security Override
3	Memory Connector 2 (T1 signal)
2	Memory Card Presence Control (R signal)
1	Memory Connector 1 (T1 signal)
0	Memory Card Presence Control (R signal)

Figure 2-12. System Board POS Register 3 (Hex 0103) — Type 3

Bit 7 This bit is reserved.

Bits 6, 3 These bits indicate the type of memory installed in connector 2 as shown in the following table.

Bits 6 3	Available RAM
0 0	Reserved
0 1	4MB Memory Card in Connector 2
1 0	Reserved
1 1	Reserved

Figure 2-13. POS Register 3 (Bits 6, 3) – Type 3

Bits 5, 1 These bits indicate the type of memory installed in connector 1 as shown in the following table.

Bits 5 1	Available RAM
0 0	Reserved
0 1	4MB Memory Card in Connector 1
1 0	Reserved
1 1	Reserved

Figure 2-14. POS Register 3 (Bits 6, 3) – Type 3

Bit 4, This bit is 0 when the service pin on the speaker/battery connector is connected to ground. This function is used by service and manufacturing personnel.

Bit 2 This is the presence-detect bit for connector 1. This bit is 0 if the proper memory card is installed.

Bit 0 This is the presence-detect bit for connector 2. This bit is 0 if the proper memory card is installed.

System Board POS Register 4 (Hex 0104) – Type 3

On the Type 3 system board, this read-only register and POS Register 3 contain information about the type of memory on the Type 3 system board.

Bit	Function
7	Reserved
6	Reserved
5	- RAM2HS
4	- RAM1HS
3	+ CIDI
2	+ CIDI
1	Reserved
0	+ Disables ROM/RAM 4KB

Figure 2-15. System Board POS Register 4 (Hex 0104) – Type 3

Bits 7, 6, 1 These bits are reserved.

Bit 5 This bit defines the type card installed in connector 2. This bit is 0 if a high-speed (80 nanosecond) memory card is installed.

Bit 4 This bit defines the type card installed in connector 1. This bit is 0 if a high-speed (80 nanosecond) memory card is installed.

Bits 3, 2 These bits are prepared for the memory card of the cache memory controller.

Bit 0 This bit disables the 4KB RAM area starting at E0000 for the display adapter card.

Adapter Enable/Setup Register (Hex 0096)

The Adapter Enable/Setup register selects the connector to be set up.

Bit	Symbol
7	Channel Reset
6 - 4	Reserved
3	Card Setup Enable
2 - 0	Channel Select 2 - 0

Figure 2-16. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6 - 4 These bits are reserved.

Bit 3 When set to 1, this bit enables the '-card setup' signal selected by bits 2 through 0.

Bits 2 - 0 These bits are the address bits for the '-card setup' signal. Connectors 1 through 8 are addressed as 0 through 7, respectively. When bit 3 is set to 1, these bits select the connector that is put into setup mode.

Each channel connector has a unique '-card setup' signal (-CD SETUP) associated with it. This signal is used to put the adapters in the setup mode, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Notes:

1. The signal, -CD SETUP, goes active only when an operation is performed in the I/O address range hex 0100 through 0107.
2. The status of port hex 0096 can be read by software. However, when the port is read, bits 6, 5, and 4 are set to 1.

Section 3. System Board

Description 3-3
80387 Math Coprocessor 3-3
Micro Channel Implementation 3-3
| Exception Reporting 3-3
Matched Memory 3-3
Matched-Memory Extension 3-4
Signal Descriptions 3-5
Matched-Memory Cycle 3-6
Matched-Memory Cycle Timing (No Waits) 3-7
Central Arbiter 3-9
Arbitration Bus Priority Assignments 3-9
Central Arbiter Programming 3-10
Memory 3-12
Read-Only Memory Subsystem—Type 1 3-12
Read-Only Memory Subsystem—Type 2 and Type 3 3-12
Random Access Memory Subsystem 3-12
| System and Nonsystem Memory 3-13
Memory Caching 3-13
Error Recovery 3-15
Memory Subsystem Control 3-16
Memory Registers—Type 1 3-16
Memory Encoding Register (Hex 00E1) 3-17
Split Address Register (Hex 00E0)—Type 1 3-19
Memory Registers—Type 2 3-20
Memory Encoding Register 1 (Hex 00E1)—Type 2 3-20
Memory Encoding Register 2 (Hex 00E0)—Type 2 3-22
Memory Registers—Type 3 3-23
Memory Encoding Register 1 (HEX 00E1) 3-23
Memory Encoding Register 2 (Hex 00E0) 3-25
Memory Encoding Register 3 (Hex 00E2) 3-25
System Memory Maps 3-26
System Board Memory Connectors 3-33
Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM 3-36
RT/CMOS Address Register and NMI Mask (Hex 0070) . . 3-37
RT/CMOS Data Register (Hex 0071) 3-37
RT/CMOS RAM I/O Operations 3-38
Real-Time Clock Bytes (Hex 000-00D) 3-39
CMOS RAM Configuration 3-42
Miscellaneous System Functions 3-47
Nonmaskable Interrupt 3-47
System Control Port B (Hex 0061) 3-47

© Copyright IBM Corp. 1989, 1990

System Control Port A (Hex 0092) 3-49
Power-On Password 3-51
Hardware Compatibility 3-51
Error Codes 3-52

Description

This section describes the Model 80 implementation of the 80387 Math Coprocessor, Micro Channel architecture, memory subsystem, and miscellaneous system ports. Additional information on these topics can be found in the *Hardware Interface Technical Reference* listed in the preface of this manual.

80387 Math Coprocessor

The 80387 Math Coprocessors are matched to the speed of the system microprocessor and operate in the synchronous mode. The 16 MHz, 20 MHz, and 25 MHz math coprocessors are not interchangeable; their logical operation is the same.

Micro Channel Implementation

This section describes the implementation of the Micro Channel architecture on Model 80 system boards. Refer to the Micro Channel architecture information in the *Hardware Interface Technical Reference — Architectures* manual for more information.

Exception Reporting

Exceptions should be reported using the asynchronous channel check procedure. The synchronous channel check procedure is not supported.

Matched Memory

The 32-bit channel connector with matched-memory extension is a dual 93-pin, 50-mil card-edge design. The matched-memory extension provides three signal lines, two ground lines, and three reserved lines.

Note: Although a memory adapter can respond to -MMC active by driving the '-matched memory cycle request' signal (-MMCR) active, a Type 2 or Type 3 system board ignores -MMCR and performs a default cycle if the 'channel ready' signal (CD CHRDY) is active, or a synchronous-extended cycle if CD CHRDY is inactive. A Type 2 or Type 3 system board will also

drive the '-matched memory cycle command' signal (-MMC CMD) active at the same time as the '-command' signal (-CMD).

Matched-Memory Extension

This extension to the 32-bit Micro Channel connector provides the signals necessary to accommodate matched-memory cycles.

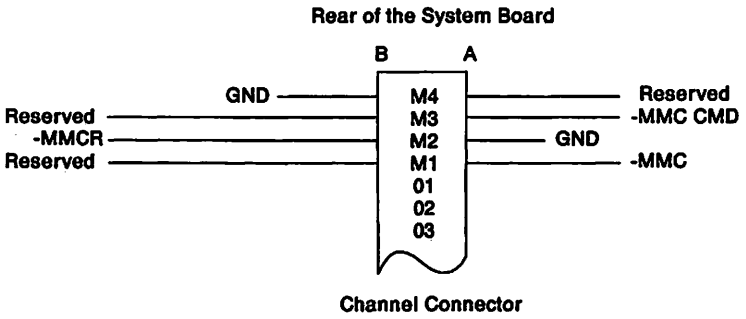


Figure 3-1. Matched-Memory Extension Voltage and Signal Assignments

Signal Descriptions

The following are descriptions of the matched-memory signals.

-MMC: -Matched Memory Cycle: This signal is driven by the system board logic to indicate to the channel slaves that the system microprocessor is the controlling master and is able to run a matched-memory cycle. -MMC is driven by a tri-state driver that can sink 24 milliamps.

-MMCR: -Matched Memory Cycle Request: This is a bus cycle control input signal. A 16- or 32-bit channel slave drives -MMCR to request a matched-memory cycle available on the system bus. This signal is driven active from an address decode and MEMORY/-IO signal.

If -MMCR is driven active by an 8-bit channel slave, or if it is driven active by a 16- or 32-bit channel slave during a cycle other than a microprocessor bus cycle, a default transfer cycle is run and -MMCR is not honored. CD CHRDY is used to extend the matched-memory cycle, as needed. The 'address latch' signal (-ADL) and -CMD remain inactive for the entire matched-memory cycle.

Only the system microprocessor can drive matched-memory cycles. This signal is wired separately to each of the 32-bit channel connectors on the system board and ORed by the system logic. This signal is driven by a totem-pole driver that can sink 6 milliamps.

-MMC CMD: -Matched Memory Cycle Command: This output signal to the bus is generated for system microprocessor bus cycles only. It is used during a matched-memory cycle to define when the data on the bus is valid. The trailing edge of this signal indicates the end of the matched-memory cycle. As with -CMD, this signal indicates the time that the data is valid on the bus, and indicates when to latch the data from the bus or stop driving the data onto the bus. -MMC CMD is driven by a tri-state driver that can sink 24 milliamps.

Matched-Memory Cycle

This section describes the Type 1 matched-memory bus operation supported by the Micro Channel. The Type 1 implementation is such that a channel slave can be either a memory or I/O slave with a data bus width of 16 or 32 bits. No 8-bit devices are allowed to run matched-memory cycles.

In addition to the three basic types of cycles defined by the Micro Channel (default, synchronous extended, and asynchronous extended), the Type 1 system board also supports the matched-memory cycle. The matched-memory cycle is a system-unique function supported by the Micro Channel, and is provided for memory subsystem expansion. This function allows the most efficient data transfer capability between the 16-MHz 80386 system microprocessor and channel memory. The system board ROM and RAM (held on the local bus) and the IBM 80386 Memory Expansion Adapter (held on the channel) adhere to the matched-memory cycle protocol described in this section.

Matched-memory cycles are a minimum of three 16-MHz clocks or a cycle time of 187.5 nanoseconds. (Default transfer cycles are a minimum of four clocks or a cycle time of 250 nanoseconds.) The target channel slave must request the matched-memory cycle on a cycle-by-cycle basis through -MMCR, or it will get the default transfer cycle.

A system microprocessor bus cycle begins by the 'address,' 'byte enables,' and 'bus definition' signals becoming valid in the first clock cycle of the bus cycle. Either of the status bits driven active signals the start of the channel bus cycle. The status state (Ts) is the first clock cycle. After Ts, the command state (Tc) is entered. Channel slaves respond to the bus operation during Tc, either transferring read data to or accepting write data from the system bus. Tc states can be repeated as often as necessary to assure sufficient time for the channel slave to respond. The signal, CD CHRDY, is used to determine whether Tc is repeated. A repeated Tc state is called a 62.5-nanosecond wait state.

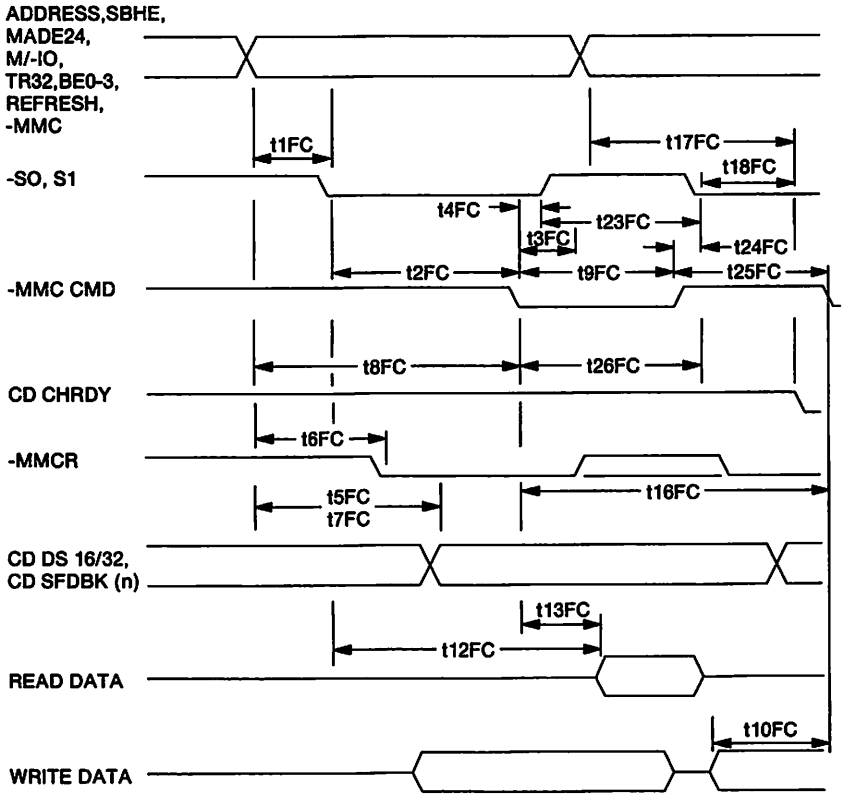
If -MMCR is driven active by the channel slave, then -MMC CMD is driven by the system microprocessor.

If -MMCR is not returned from the channel slave, a default cycle is run. Default transfer and matched-memory bus cycles can be mixed in any manner, because the mechanism is completely dynamic on a

bus cycle basis. Bus cycles can be extended until CD CHRDY is sampled as active.

CD CHRDY is driven inactive by a slave to allow additional time to complete a default or matched-memory cycle when the normal cycle length is not sufficient to service that device. The timings for the matched-memory cycles are shown on the following pages.

Matched-Memory Cycle Timing (No Waits)



Symbol	Description	Min/Max
t3 FC	ADDR hold from -MMC CMD active	20 / - ns
t4 FC	Status hold from -MMC CMD active	25 / - ns
t9 FC	-MMC CMD pulse width	85 / - ns
t9 FCE	-MMC CMD pulse width (Extended Cycle)	145 / - ns
t10 FC	Write data valid to -MMC CMD active	0 / - ns
t11 FC	Write data hold from -MMC CMD inactive	30 / - ns
t13 FC	Read data valid from -MMC CMD active	- / 60 ns
t14 FC	Read data hold from -MMC CMD inactive	0 / - ns
t15 FC	Read data off delay from -MMC CMD inactive	- / 40 ns
t16 FC	-MMC CMD active to next -MMC CMD active	240 / - ns
t17 FC	CD CHRDY valid from ADDR valid	- / 70 ns
t18 FC	CD CHRDY valid from Status active	- / 30 ns
t19 FC	CD CHRDY active from Status inactive	- / 9 ns
t20 FC	Read data valid from -MMC CMD active	- / 125 ns
t21 FC	Read data valid from CD CHRDY active	- / 45 ns
t22 FC	-MMC CMD inactive from CD CHRDY active	65 / - ns
t23 FC	Status inactive pulse width	30 / - ns
t24 FC	Next Status active to -MMC CMD inactive	- / 5 ns
t25 FC	-MMC CMD inactive pulse width	85 / - ns

Figure 3-2. Matched Memory Cycle (No Waits)

Matched-memory cycles are supported for 32-bit and 16-bit channel devices only. Eight-bit channel devices cannot run matched-memory cycles.

Note: Adapters using this protocol can be installed only in the three 32-bit channel connectors and therefore sacrifice some *portability*. These adapters may not fit or operate in some other systems.

When -MMC is active, 32-bit and 16-bit devices should not use -MADE 24, A0, A1, or -SBHE in logic that generates -MMCR, -CD DS 16/32, -CD SFDBK, and CD CHRDY.

Central Arbiter

The central arbitration control point gives intelligent subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. This arbiter supports up to 16 arbitrating devices.

Arbitration Bus Priority Assignments

The following table shows the assignment of arbitration levels. The functions with the lowest arbitration level have the highest priority.

ARB Level	Primary Assignment
-2	Memory Refresh
-1	NMI
0	DMA Channel 0 (Programmable to any arbitration level)
1	DMA Channel 1
2	DMA Channel 2
3	DMA Channel 3
4	DMA Channel 4 (Programmable to any arbitration level)
5	DMA Channel 5
6	DMA Channel 6
7	DMA Channel 7
8 - E	Available
F	System Microprocessor

Figure 3-3. Arbitration Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation, and by the previous controlling master. To prevent overrun, the diskette drive controller must not be held inactive for more than 12 micro-sections.

NMI service is executed at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal is in the arbitrate state.

When the central arbitration control point receives a level -1 request (NMI, a system-board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level -1 request, and

holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following tables.

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Mask
5	Enable Extended Arbitration
4 - 0	Reserved

Figure 3-4. Arbitration Register, Write to Hex 0090

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Masked by NMI
5	Bus Time-Out
4	Reserved
3 - 0	Value of Arbitration Bus During Previous Grant State

Figure 3-5. Arbitration Register, Read Hex 0090

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit must be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 enables extended arbitration. The minimum arbitration cycle is 300 nanoseconds; this bit extends that minimum cycle to 600 nanoseconds. This bit is set to 0 during a system reset.

Reading this bit as a 1 indicates that a bus time-out has occurred, and resets bit 6 in this register to 0.

Bit 4 This bit is reserved and must be 0.

Bits 3 - 0 These bits are undefined for a write operation and must be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Memory

The Model 80 systems use the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- Real-time clock and CMOS RAM.

Read-Only Memory Subsystem – Type 1

The ROM subsystem on the Type 1 system board consists of four 32KB by 8-bit modules in a 32KB by 32-bit arrangement (KB equals 1024 bits). ROM is assigned at the top of the first and last 1MB address space (000E0000 and FFFE0000). ROM is not parity-checked. It operates with one 62.5-nanosecond wait state.

Read-Only Memory Subsystem – Type 2 and Type 3

The ROM subsystem on the Type 2 and Type 3 system boards consist of two 64KB by 8-bit modules in a 64KB by 16-bit arrangement. ROM is active at power-on at the top of the first and last 1MB of address space (000E0000 and FFFE0000). After POST ensures the proper operation of system memory, the ROM code is copied to RAM at the same address space, and the ROM is disabled.

Random Access Memory Subsystem

The RAM subsystem on the system board consists of memory modules mounted on a printed-circuit board, which attaches to the system board through a 3- by 32-pin connector. Two connectors are provided on the system board. The Type 1 system board supports the 1MB memory cards; the Type 2 system board supports the 2MB memory cards. Type 2 system board POST routines require a minimum of 1MB of functional memory installed in connector 1. The Type 1 system board requires a minimum of 1MB of functional memory and the Type 3 requires a minimum of 1MB to 4MB; however it can be installed in either connectors 1 or connectors 2. The RAM subsystem is 36 bits wide: 32 data bits and 4 parity bits. One parity bit is generated for each byte of data written. During a read operation, one parity bit is checked for each byte of data read by the device controlling the bus.

Notes:

1. Additional memory can be added in any of the 32-bit Micro Channel connectors. The total amount of memory installed must not exceed the 16MB addressing limit of the DMA controller.
2. For the Type 3 system board, system memory must be 32-bit wide (nonsystem memory can be any width).

System and Nonsystem Memory

Two basic types of memory can be assigned addresses within the memory address space: system memory and nonsystem memory.

System memory is memory that is managed and allocated by the primary operating system. It remains assigned to and fixed in the 4GB (GB = 1,073,741,824 bytes) physical address space, and its contents can be accessed or modified only by an independent master (bus master, system microprocessor, or DMA controller).

Nonsystem memory is memory that is not managed or allocated by the primary operating system. It is made up of memory-mapped I/O devices, memory on an adapter that can be directly modified by the adapter, or memory that can be relocated within the address space, such as bank switched and EMS (expanded memory specifications). Nonsystem memory should not be mapped into microprocessor's cacheable address space.

Memory Caching

The following figure is the memory map for the first 32MB of address space on Type 3 system boards and shows which addresses can be used with the cache. On the Type 3 system board, the address space from 32MB to the end of the second GB (GB = 1,073,741,842 bytes) is not usable. The third and fourth GB are not mapped into the cache, but can be used, especially for nonsystem memory.

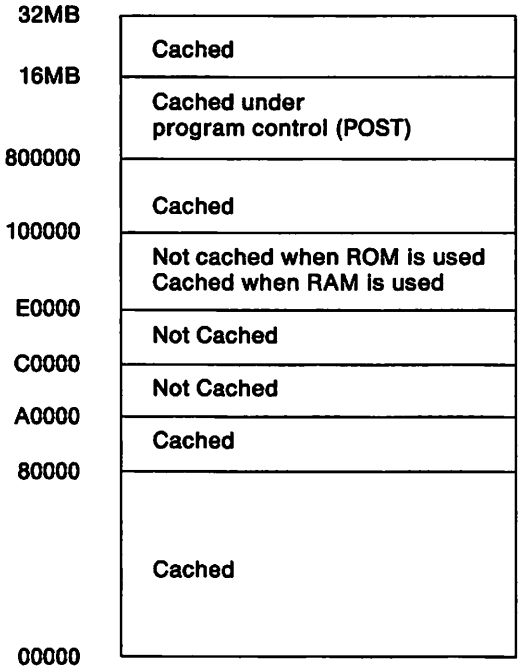


Figure 3-6. Mapping of the First 32MB Segment

Within the first 16MB of address space, all system memory above 1MB must be one contiguous sum starting at the 1MB boundary. If nonsystem memory is present, it should be assigned addresses starting at 16MB and counting down. Do not assign addresses below 8MB to nonsystem memory.

If nonsystem memory exists between 8MB and 16MB, caching for that 8MB block must be disabled even if system memory also is located there. Setup routines must be aware of the existence and location of nonsystem memory so that POST can properly control the caching of the second 8MB.

In the 16MB to 4GB address space, system memory can be contiguously placed from 16MB up to 32MB and can be cached. If nonsystem memory is within the 16MB to 4GB address space, it should be assigned addresses starting at 4GB and counting down, allowing space for system ROM.

Error Recovery

If POST detects a memory error in the first 512KB of memory, the first physical 1MB block of memory is deactivated. The addresses assigned to the deactivated block are reassigned to the second physical block of system board memory, if installed. If an error also is detected in the first 512KB of the second 1MB block of system board memory, the system cannot recover. The first 512KB of memory address space cannot be assigned to reside on an adapter installed in the channel.

POST does not deactivate a memory block if an error is detected in the second 512KB of that block. If an error is detected in that area of memory, the 1MB block containing the error can be deactivated. Have its addresses reassigned by running the memory diagnostics program on the Reference Diskette supplied with the system. Once a block of memory is deactivated, it is ignored by POST.

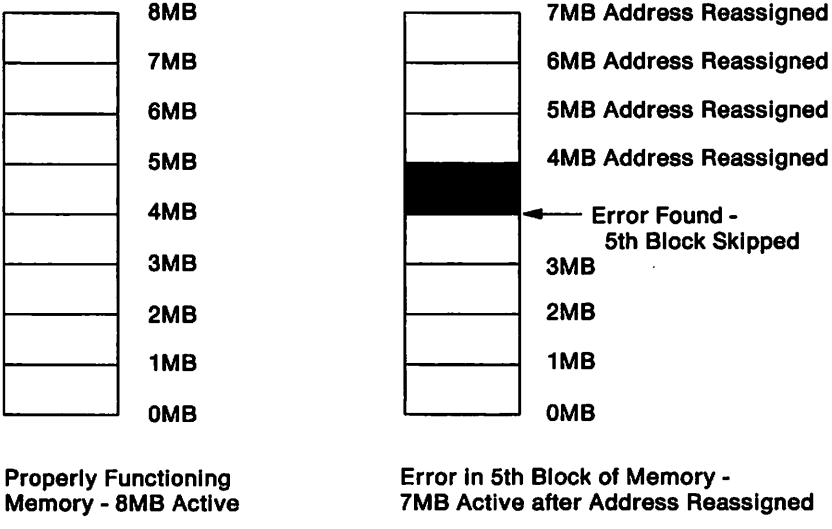


Figure 3-7. Memory Error Address Reassignment

Memory Subsystem Control

The Type 1, Type 2, and Type 3 system boards enable memory in 1MB blocks. Each block must start on a 1MB boundary. Because 128KB of system board ROM, 128KB of I/O ROM, and 128KB of video RAM are mapped within the first 1MB address space, the first physical 1MB of memory cannot be mapped to contiguous addresses and is therefore split at either the 512KB or 640KB boundary. The first 512KB or 640KB is addressed beginning at hex 00000000; the remaining unmapped memory, called the *split-memory block*, can be mapped in several ways:

- Type 1 system board – The entire split-memory block is mapped to the first available address following the last full 1MB block of activated memory. Alternatively, the split-memory block can be handled in either of the following ways:
  - It can be totally disabled.
  - 128KB of the split-memory block can be mapped to the system board ROM address space, replacing the system board ROM. The remainder of the split-memory block is disabled.
- Type 2 system board – In addition to mapping the first 512KB or 640KB of physical RAM, the Type 2 system board automatically maps 128KB of the first 1MB of RAM to the system board ROM address space. The ROM code is then copied into RAM at this location. The remaining unmapped memory, the *split-memory block*, can be either disabled or mapped to the first available address following the last full 1MB block of activated memory .

The size of the split-memory block, memory mapping, and disabling of memory blocks are controlled by registers residing at addresses hex 00E0 and 00E1. The Type 1, Type 2, and Type 3 system boards define these registers differently.

Memory Registers – Type 1

Three registers define how the system board memory is addressed and used:

- Memory Encoding register (hex 00E1)
- Memory Encoding register (hex 00E0)
- Memory Encoding register (hex 00E2).

Memory Encoding Register (Hex 00E1)

This read/write register determines the amount of enabled system board memory and how it is used.

Bit	Function
7	EN4
6	EN3
5	EN2
4	EN1
3	-ENSPLIT
2	-640
1	ROMEN
0	-ENPLRPCH

Figure 3-8. Memory Enable Bits (Connector 2)

Bits 7, 6 These bits define the amount of enabled memory in system board memory connector 2.

Bits 7 6	Amount of RAM	Function
0 0	Reserved	
0 1	Reserved	
1 0	1MB	1MB Memory Card enabled in Connector 2
1 1	0MB	Memory Card Disabled or No Memory Card Present in Connector 2

Figure 3-9. Memory Enable Bits (Connector 1)

Bits 5, 4 These bits define the amount of enabled memory in system board memory connector 1.

Bits 5 4	Amount of RAM	Function
0 0	Reserved	
0 1	Reserved	
1 0	1MB	1MB Memory Card enabled in Connector 1
1 1	0MB	Memory Card Disabled or No Memory Card Present in Connector 1

Figure 3-10. Memory Encoding Register (Bits 5 and 4) — Type 1

Bit 3 This bit determines whether the split-memory block is assigned addresses or disabled.

When this bit is set to 0, the split-memory block is enabled. The split-memory block size is 384KB or 512KB, depending on the -640 bit, and its address is determined in the Split Address register. When this bit is set to 1, the split-memory block is disabled; however, 128KB of the split-memory block can be used in the ROM address space by setting bit 1 (ROMEN) to 0.

Bit 2 This bit determines where the first active 1MB block of RAM is split.

When this bit is set to 0, 640KB of the first 1MB of memory is mapped into the first 640KB of address space (hex 00000000 to 0009FFFF). When set to 1, 512KB of the first 1MB of memory is mapped into the first 512KB of address space (hex 00000000 to 0007FFFF) and addresses 00080000 through 0009FFFF are unused.

Bit 1 This bit can deactivate the system board ROM and use its address space for system board RAM.

When set to 0, this bit places the ROM address space (hex 000E0000 to 000FFFFF) into RAM. The split-memory block must be disabled. Either 256KB or 384KB of memory is unused (depending on the -640 bit) and the ROM modules are deactivated. When this bit is set to 1, the ROM modules are left active.

The following table shows how bits 3, 2, and 1 are used together to define the various configurations.

Bits 3 2 1	Function
0 0 0	Invalid
0 0 1	ROM Enabled, Split at 640KB, High 384KB at Split Address
0 1 0	Invalid
0 1 1	ROM Enabled, Split at 512KB, High 512KB at Split Address
1 0 0	ROM Disabled, Split at 640KB, 128KB of High 384KB at ROM Address
1 0 1	ROM Enabled, Split at 640KB, High 384KB Not Used
1 1 0	ROM Disabled, Split at 512KB, 128KB of High 512KB at ROM Address
1 1 1	ROM Enabled, Split at 512KB, High 512KB Not Used

Figure 3-11. Memory Encoding—Type 1

Bit 0 When set to 0, this bit enables parity checking of system board memory. To clear a parity error, this bit must be set to 1 and then to 0.

Split Address Register (Hex 00E0)—Type 1

This read/write register defines the starting address of the split-memory block.

Bit	Function
7 - 4	Reserved
3	SPA23
2	SPA22
1	SPA21
0	SPA20

Figure 3-12. Split Address Register

Bits 7 - 4 These bits are reserved and must be set to 0.

Bits 3 - 0 These bits define the starting address of the split-memory block.

These bits must not be set to a value of 0 unless -ENSPLIT is set to 1. When -ENSPLIT is set to 0, these bits determine the starting address of the split-memory block. The starting address can be at any 1MB boundary from 1MB to 15MB.

Note: If the total system memory is equal to or greater than 16MB, the split-memory block cannot be used.

Memory Registers – Type 2

Two registers define how the system board memory is addressed and used:

- Memory Encoding Register 1
- Memory Encoding Register 2 (hex 00E0).

Memory Encoding Register 1 (Hex 00E1) – Type 2

This read/write register determines the amount of enabled system board memory in connector 1 and how it is used.

Bit	Function
7, 6	Reserved
5	-Card 1 EN2
4	-Card 1 EN1
3	-ENSPLIT
2	-640
1	ROMEN
0	-ENPLRPCH

Figure 3-13. Memory Encoding Register 1 – Type 2

Bits 7, 6 These bits are reserved and must be set to 1.

Bits 5 - 4 These bits define the amount of enabled memory in system board memory connector 1.

Bits 5 4	Amount of RAM	Function
0 0	2MB	2MB Card Enabled in Connector 1
0 1	1MB	First 1MB Disabled on 2MB Card in Connector 1
1 0	1MB	Second 1MB Disabled on 2MB Card in Connector 1
1 1	0MB	Invalid (1MB Minimum Must Be Present)

Figure 3-14. Memory Enable Bits – Type 2

Bit 3 This bit determines whether the split-memory block is assigned addresses or is disabled. The top 128KB of the first 1MB is always mapped into the ROM address space, and the ROM code is copied into this space.

When this bit is set to 0, the split-memory block is enabled. The split-memory block size is dependent on the value of the- 640 bit. Its address is determined in Memory Encoding Register 2. When this bit is set to 1, the split-memory block is disabled.

Note: If the total system memory is equal to or greater than 16MB, the split-memory block cannot be used.

Bit 2 This bit determines where the first active 1MB of memory is split.

When this bit is set to 0, the system maps 640KB of the first 1MB to address hex 00000000 to 0009FFFF. The split-memory block, 256KB, is mapped to the address specified in Memory Encoding register 2.

When this bit is set to 1, the system maps 512KB of the first 1MB to address hex 00000000 to 0007FFFF. The split-memory block, 384KB, is mapped to the address specified in Memory Encoding register 2. The addresses, hex 00080000 to 0009FFFF, are unassigned.

Bit 1 This bit determines how addresses, hex 000E0000 to 000FFFFF, are assigned.

When this bit is set to 1, ROM is enabled and the read-access addresses are assigned to ROM; the write-access addresses are assigned to RAM. When this bit is set to 0, ROM is disabled and read addresses are assigned to RAM; the write addresses are disabled while ROM is disabled.

Note: When this bit is set to 1, system performance will be substantially slower because of 16-bit accesses to ROM and a longer cycle.

The following figure shows how bits 3, 2, and 1 are used together to define the various configurations.

Bits 3 2 1	Function
0 0 0	ROM Disabled, Split at 640KB, 256KB at Split Address
0 0 1	ROM Enabled (ROM Mapped to RAM Disabled), Split at 640KB, 256KB at Split Address
0 1 0	ROM Disabled, Split at 512KB, 384KB at Split Address
0 1 1	ROM Enabled (ROM Mapped to RAM Disabled), Split at 512KB, 384KB at Split Address
1 0 0	ROM Disabled, Split at 640KB, 256KB at Split Address Disabled
1 0 1	ROM Enabled (ROM Mapped to RAM Disabled), Split at 640KB, 256KB at Split Address Disabled
1 1 0	ROM Disabled, Split at 512KB, 384KB at Split Address Disabled
1 1 1	ROM Enabled (ROM Mapped to RAM Disabled), Split at 512KB, 384KB at Split Address Disabled

Figure 3-15. Memory Encoding Register 1 (Bits 3 and 1)

Bit 0 When set to 0, this bit enables parity checking of system board memory. To clear a parity error, this bit must be set to 1 and then to 0.

Memory Encoding Register 2 (Hex 00E0) – Type 2

This read/write register determines the amount of enabled system board memory in connector 2 and the starting address of the split-memory block.

Bit	Function
7, 6	Reserved
5	-Card 2 EN2
4	-Card 2 EN1
3	SPA23
2	SPA22
1	SPA21
0	SPA20

Figure 3-16. Memory Encoding Register 2 – Type 2

Bits 7, 6 These bits are reserved and must be set to 1.

Bits 5 - 4 These bits define the amount of enabled memory in system board memory connector 2.

Bits 5 4	Amount	Function of RAM
0 0	2MB	2MB Card Enabled in Connector 2
0 1	1MB	First 1MB Disabled on 2MB Card in Connector 2
1 0	1MB	Second 1MB Disabled on 2MB Card in Connector 2
1 1	0MB	All Disabled Or No Card Present.

Figure 3-17. Memory Encoding Register 2 (Bits 5 and 4) – Type 2

Bits 3 - 0 This register defines the starting address of the split-memory block.

These bits must not be set to a value of 0 unless split memory is disabled. When split memory is enabled, these bits determine its starting address. The starting address can be at any 1MB boundary from 1MB to 15MB.

Note: If the total system memory is equal to or greater than 16MB, the split-memory block cannot be used.

Memory Registers – Type 3

Memory Encoding registers 1, 2, and 3 define how the system board memory is addressed and used.

Memory Encoding Register 1 (HEX 00E1)

This register determines how the first 1MB of memory is addressed and is used with Memory Encoding Register 2 to determine the amount of system board memory enabled.

Bit	Function
7	-Card 2 EN4
6	-Card EN1
5	-Card EN2
4	-Card EN1
3	-ENSPLIT
2	-640
1	ROMEN
0	-ENPLRPCH

Figure 3-18. Memory Encoding Register 1 (Hex 00E1)

Bits 7, 6 These bits define system board memory in connector 2. When they are set to 0, bit 6 enables the first 1MB block and bit 7 enables the second 1MB block.

Bits 5, 4 Theses bits define system board memory in connector 1. When they are set to 0, bit 4 enables the first 1MB block and bit 5 enables the second 1MB block.

BIT 3 This bit determines whether the split-memory block is assigned addresses or is disabled. The top 128KB of the first 1MB is always mapped into the ROM address space and the ROM code is copied into this space.

When this bit is set to 0, the split-memory block is enabled. The split-memory block size is dependent on the value of the -640 bit. Its address is determined in Memory Encoding Register 2. When this bit is set to 1, the split-memory block is disabled.

Note: If the total system memory is equal to or greater than 16MB, the split-memory block cannot be used.

BIT 2 This bit determines where the first active 1MB of memory is split.

When the first bit is set to 0, the system maps 640KB of the first 1MB to address hex 00000000 to 0007FFFF. The split-memory block, 256KB, is mapped to the address specified in Memory Encoding register 2.

When this bit is set to 1, the system maps 512 of the first 1MB to address hex 00000000 to 0007FFFF. The split-memory block, 384KB, is mapped to the address specified in the Memory Encoding register 2. The address hex 00080000 to 0009FFFF are unassigned.

BIT 1 This bit determines how addresses hex 000E0000 to 000FFFFF are assigned.

When this bit is set to 1, ROM is enabled and the read-access addresses is assigned to ROM; the write-access addresses are assigned to RAM. When this bit is set to 0, ROM is disabled and read addresses are assigned to RAM; the write address are disabled while ROM is disabled.

Note: When this bit is set to 1, system performance will be substantially slower because of 16 bit accesses to ROM and a longer cycle.

BIT 0 When set to 0, this bit enables parity checking of system board memory. For compatibility with other systems, enabling and disabling of parity checking should be done through the System Control Port B at address hex 0061.

Memory Encoding Register 2 (Hex 00E0)

This register is used with Memory Encoding Register 1 to determine the amount of system board memory that is enabled. It also contains the address for the split-memory block.

Bit	Function
7	-Card 4 EN2
6	-Card 4 EN1
5	-Card 4 EN2
4	-Card 3 EN1
3	SPA23
2	SPA22
1	SPA21
0	SPA20

Figure 3-19. Memory Encoding Register 2 (Hex 00E0)

Bits 7, 6 These bits define the system board memory in connector 4. When set to 0, bit 6 enables the first 1MB block and bit 7 enables the second 1MB block.

Bits 5, 4 These bits define the system board memory in connector 3. When they are set to 0, bit 4 enables the first 1MB block and bit 5 enables the second 1MB block.

Bits 3 - 0 These bits define the starting address of the split-memory block. When split memory is enabled, these bits determine its starting address. The starting address can be at any boundary from 1MB to 15MB.

Memory Encoding Register 3 (Hex 00E2)

This read/write register is used by the Type 3 system board and provides control of the cache memory.

Bit	Function
7	Reserved
6	-Preempt Enable
5	-Cache Flush
4	Lock
3	Reserved
2	-Cache 2nd 8MB
1	Reserved
0	-Enable Cache

Figure 3-20. Memory Encoding Register 3 (Hex 00E2

Bits 7 This bit is reserved.

Bit 6 This bit controls the preempt support for the system microprocessor on the Type 3 system board. When this bit is set to 1, preempt is disabled. When this bit is set to 0, system logic activates the '-preempt' signal when the system microprocessor accesses a memory location not satisfied in the cache (cache miss).

Bit 5 See the description of bit 0.

Bit 4 This bit controls whether locked-access operations from the system microprocessor can or cannot be cache hits. If this bit is set to 0, all locked-access operations are treated as cache misses. If this bit is set to 1, locked access operations can be cache hits.

Bit 3 This bit is reserved.

Bit 2 This bit determines whether the second 8MB of memory is cache are not. When the bit is set to 0, the second 8MB is cache.

Bit 1 This bit is reserved.

Bit 0 This bit and bit 5 work together to control the state of the cache: either disabled and clear, or enabled. These bits must always be opposite polarities, and they must be modified in the same I/O instruction. When bit 5 is set to 0 and bit 0 is set to 1, the cache is disabled and flushed of data; when bit 5 is set to 1 and bit 0 is set to 1, the cache is enabled.

Note: The cache must be disabled and flushed before enabling ROM or disabling the cache of the second 8MB.

System Memory Maps

Memory is mapped by registers at hex 00E0 and 00E1. The mapping results in either 512KB or 640KB of system board RAM starting at address hex 00000000. A 256-byte portion and a 1KB portion of this RAM are reserved as BIOS data areas. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for details.

In the following tables, the variable *X* represents the number of 1MB blocks of system board memory starting at or above the hex 00100000 boundary. The variable *Y* represents the number of 1MB blocks of memory installed in the channel starting at or above the hex 00100000 boundary (*Y* = 0 to 15).

The following table shows the memory mapping when:

Enable Split bit = 1
640 bit = 1
ROM enable bit = 1.

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-21. System Memory Map 1—Type 1, Type 2, and Type 3

The following table shows the memory mapping when:

Enable Split bit = 1
640 bit = 0
ROM enable bit = 1.

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-22. System Memory Map 2—Type 1, Type 2, and Type 3

The following tables show the memory mapping when:

Enable Split bit = 0
640 bit = 1
ROM enable bit = 1
Split address byte = 1 + *X* + *Y* (Total Range = 1 to 15).

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to (00100000 + *X*MB + *Y*MB + 512KB - 1)	512KB System Board RAM
(00100000 + *X*MB + *Y*MB + 512KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-23. System Memory Map 3 – Type 1

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to (00100000 + *X*MB + *Y*MB +384KB – 1)	384KB System Board RAM
(00100000 + *X*MB + *Y*MB + 384KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-24. System Memory Map 3 – Type 2 and Type 3

The following tables show the memory mapping when:

Enable Split bit = 0
640 bit = 0
ROM enable bit = 1
Split address byte = 1 + *X* + *Y* (Total Range = 1 to 15).

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to (00100000 + XMB + YMB + 384KB - 1)	384KB System Board RAM
(00100000 + XMB + YMB + 384KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-25. System Memory Map 4 – Type 1

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to (00100000 + XMB + YMB + 256KB – 1)	256KB System Board RAM
(00100000 + XMB + YMB + 256KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-26. System Memory Map 4 – Type 2 and Type 3

The following tables show the memory mapping when:

Enable Split bit = 1
640 bit = 1
ROM enable bit = 0

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00008000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-27. System Memory Map 5 — Type 1

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00008000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-28. System Memory Map 5 — Type 2 and Type 3

The following tables show the memory mapping when:

Enable Split bit = 1
640 bit = 0
ROM enable bit = 0

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-29. System Memory Map 6 – Type 1

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-30. System Memory Map 6 – Type 2 and Type 3

The following table shows the memory mapping when:

Enable Split bit = 0
640 bit = 1
ROM enable bit = 0
Split address bits = 1 + *X* + *Y* (Total Range = 1 to 15).

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to (00100000 + XMB + YMB + 384KB − 1)	384KB of First 1MB at Split Address
(00100000 + XMB + YMB + 384KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-31. System Memory Map 7 — Type 2 and Type 3

The following table shows the memory mapping when:

Enable Split bit = 0
640 bit = 0
ROM enable bit = 0
Split address bits = 1 + *X* + *Y* (Total Range = 1 to 15).

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to (00100000 + XMB + YMB + 256KB-1)	256KB of First 1MB at Split Address
(00100000 + XMB + YMB + 256KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-32. System Memory Map 8 — Type 2 and Type 3

System Board Memory Connectors

The Type 1, 2, and 3 system boards are equipped with two 3- by 32-pin system board memory connectors. A memory card must be installed in connector 1 before additional memory can be used in the channel.

The following figure shows the pin locations of the 3- by 32-pin system board memory connectors. The pin locations are the same for connectors 1 and 2. Connector 1 is closest to the power supply. Pin 32 is closest to the rear of the system board.

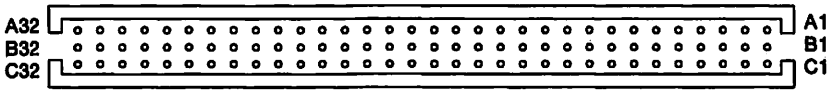


Figure 3-33. System Board Memory Connector Pin Locations

The following is a list of signals used by the system board memory connectors.

-MW -Memory Write

-MA(0-8) -Memory Address (0 through 8)

-RAS(0-3) -Row Address Strobe (0 through 3)

-CAS(0-3) -Column Address Strobe (0 through 3)

-CASP -Column Address Strobe Parity

MDP(0-3) Memory Data Parity (0 through 3)

MD(0-31) Memory Data (0 through 31)

-BE(0-3) -Byte Enable (0 through 3)

R This signal is used by POS Register 3 during system board setup to determine the presence of a memory card in each of the two system board memory connectors.

Note: Type 2 system board POST routines require a minimum of 1MB of functional memory installed in connector 1. The Type 1 system board also requires a minimum of 1MB of functional memory; however, it may be installed in either connector. The Type 3 system board POST routines require 4MB of functional memory installed in connector 1.

-RAMHS This signal is used by POS Register 4 to detect the memory speed.

T1, T2 These signals are used by POS Register 3 during system board setup to determine the type of memory card installed in each of the two Type 3 system board memory connectors. See Section 2, "Programmable Option Select," for additional information.

The following figure shows the pin assignments for the Type 3 system board memory connector. Inputs (I) to and Outputs (O) from the system board also are shown.

Row A			Row B			Row C		
Pin	I/O	Signal	Pin	I/O	Signal	Pin	I/O	Signal
A1	N/A	Reserved	B1	N/A	Ground	C1	I/O	MD0
A2	O	-MW	B2	O	+5 Vdc	C2	I/O	MD1
A3	O	MA0	B3	N/A	Ground	C3	I/O	MD2
A4	O	MA1	B4	O	+5 Vdc	C4	I/O	MD3
A5	O	MA2	B5	N/A	Ground	C5	I/O	MD4
A6	O	MA3	B6	O	+5 Vdc	C6	I/O	MD5
A7	O	MA4	B7	N/A	Ground	C7	I/O	MD6
A8	O	MA5	B8	O	+5 Vdc	C8	I/O	MD7
A9	O	MA6	B9	N/A	Ground	C9	I/O	MD8
A10	O	MA7	B10	O	+5 Vdc	C10	I/O	MD9
A11	O	MA8	B11	N/A	Ground	C11	I/O	MD10
A12	O	-RAS0	B12	O	+5 Vdc	C12	I/O	MD11
A13	O	-RAS1	B13	N/A	Ground	C13	I/O	MD12
A14	O	-RAS2	B14	O	+5 Vdc	C14	I/O	MD13
A15	O	-RAS3	B15	N/A	Ground	C15	I/O	MD14
A16	I	-RAMHS*	B16	O	+5 Vdc	C16	I/O	MD15
A17	I	-R	B17	N/A	Ground	C17	I/O	MD16
A18	I	T2*	B18	O	+5 Vdc	C18	I/O	MD17
A19	O	-CAS0	B19	N/A	Ground	C19	I/O	MD18
A20	O	-CAS1	B20	O	+5 Vdc	C20	I/O	MD19
A21	O	-CAS2	B21	N/A	Ground	C21	I/O	MD20
A22	O	-CAS3	B22	O	+5 Vdc	C22	I/O	MD21
A23	I/O	MDP0	B23	N/A	Ground	C23	I/O	MD22
A24	I/O	MDP1	B24	O	+5 Vdc	C24	I/O	MD23
A25	I/O	MDP2	B25	N/A	Ground	C25	I/O	MD24
A26	I/O	MDP3	B26	O	+5 Vdc	C26	I/O	MD25
A27	I	-BE0	B27	N/A	Ground	C27	I/O	MD26
A28	I	-BE1	B28	O	+5 Vdc	C28	I/O	MD27
A29	I	-BE2	B29	N/A	Ground	C29	I/O	MD28
A30	I	-BE3	B30	O	+5 Vdc	C30	I/O	MD29
A31	I	-CASP	B31	N/A	Ground	C31	I/O	MD30
A32	I	T1	B32	O	+5 Vdc	C32	I/O	MD31

Note: * Type 3 only

Figure 3-34. System Board Memory Connector

Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM

The real-time clock/complementary metal-oxide semiconductor RAM (RT/CMOS) chip contains the real-time clock and 64 bytes of CMOS RAM. The internal clock circuitry uses 14 bytes of this memory, and the rest is allocated to configuration and system status information.

In addition to the 64 bytes of CMOS RAM, a 2KB CMOS RAM extension is provided for configuration and other system information.

A 6-Vdc lithium battery maintains voltage to the RT/CMOS RAM and 2KB CMOS RAM extension when the power supply is not in operation.

The system cover can be locked to prevent battery removal and loss of password and configuration information.

The following table shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM
000 - 00D	Real-Time Clock
00E	Diagnostic Status
00F	Shutdown Status
010	Diskette Drive Type
011	First Fixed Disk Drive Type
012	Second Fixed Disk Drive Type
013	Reserved
014	Equipment
015 - 016	Low and High Base Memory
017 - 018	Low and High Expansion Memory
019 - 031	Reserved
032 - 033	Configuration CRC
034	Reserved
035 - 036	Low and High Useable Memory
037	Date Century
038 - 03F	Reserved

Figure 3-35. RT/CMOS RAM Address Map

RT/CMOS Address Register and NMI Mask (Hex 0070)

This register is used in conjunction with the port at hex 0071 to read and write the RT/CMOS RAM bytes.

Bit	Function
7	NMI Mask
6	Reserved
5 - 0	RT/CMOS RAM Address

Figure 3-36. RT/CMOS Address Register and NMI Mask (Hex 0070)

Warning: The operation following a write to hex 0070 must access port hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM might occur.

Bit 7 When this bit is set to 1, the NMI is masked off (the NMI is disabled). This bit is set to 1 by a power-on reset. This is a write-only bit.

Bit 6 Reserved.

Bits 5 - 0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This port is used in conjunction with the address register at hex 0070 to read and write the RT/CMOS RAM bytes.

Bit	Function
7 - 0	RT/CMOS Data

Figure 3-37. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts must be masked to prevent other interrupt routines from changing the CMOS Address register before data is read or written. After I/O operations, the RT/CMOS and NMI Mask register (hex 0070) must be left pointing to Status Register D (hex 00D).

Warning: The operation following a write to hex 0070 must access hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM might occur.

The following steps are required to perform I/O operations to the RT/CMOS RAM addresses:

1. Write the RT/CMOS RAM address to the RT/CMOS Address register (hex 0070).
2. Write the data to address hex 0071.

Reading RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS Address register (hex 0070).
2. Read the data from address hex 0071.

Real-Time Clock Bytes (Hex 000-00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following table.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second Alarm	1
002	Minutes	2
003	Minute Alarm	3
004	Hours	4
005	Hour Alarm	5
006	Day of Week	6
007	Date of Month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-38. Real-Time Clock Bytes

Status Register A (Hex 00A)

Bit	Function
7	Update in Progress
6 - 4	22-Stage Divider
3 - 0	Rate Selection Bits

Figure 3-39. Status Register A

Bit 7 When set to 1, this bit indicates the time-update cycle is in progress. When set to 0, it indicates the current date and time can be read.

Bits 6 - 4 These three divider-selection bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768 kHz time base. This is the only value supported by the system for proper timekeeping.

Bits 3 - 0 These bits allow the selection of a divider output frequency. The system initializes the rate selection bits to a binary 0110, which selects a 1.024 kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Periodic Interrupt Enable
5	Alarm Interrupt Enable
4	Update-Ended Interrupt Enabled
3	Square Wave Enabled
2	Date Mode
1	24-Hour Mode
0	Daylight Savings Enabled

Figure 3-40. Status Register B

Bit 7 When set to 0, this bit updates the cycle, normally by advancing the counts at a rate of one per second. When set to 1, this bit immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This bit is a read and write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

Bit 5 When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit indicates if the time-and-date calendar updates use binary or binary-coded-decimal (BCD) formats. When set to 1, this bit indicates a binary format. The system initializes this bit to 0.

Bit 1 This bit establishes if the hours byte is in the 24-hour or 12-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When set to 1, this bit enables the daylight savings time mode. When set to 0, it disables the mode, and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt Request Flag
6	Periodic Interrupt Flag
5	Alarm Interrupt Flag
4	Update-Ended Interrupt Flag
3 - 0	Reserved

Figure 3-41. Status Register C

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 This bit is used in conjunction with bits 6, 5, and 4. When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When set to 1, this bit indicates that a periodic interrupt occurred.

Bit 5 When set to 1, this bit indicates that an alarm interrupt occurred.

Bit 4 When set to 1, this bit indicates that an update-ended interrupt occurred.

Bits 3 - 0 Reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6 - 0	Reserved

Figure 3-42. Status Register D

Bit 7 This read-only bit monitors the power-sense pin. A low state of this pin indicates a loss of power to the real-time clock (dead battery). When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power.

Bits 6 - 0 Reserved.

Note: The Setup program initializes status registers A, B, C, and D when the time, and date are set. Interrupt hex 1A is the BIOS interface to read and set the time and date, and it initializes the registers the same way as the Setup program.

CMOS RAM Configuration

The following shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-Time Clock Chip Power
6	Configuration Record and Checksum Status
5	Incorrect Configuration
4	Memory Size Miscompare
3	Fixed Disk Controller/Drive C Initialization Status
2	Time Status Indicator
1	Adapter Configuration Miscompare
0	Adapter ID Time-Out

Figure 3-43. Diagnostic Status Byte

Bit 7 When set to 1, this bit indicates the real-time clock chip lost power.

Bit 6 When this bit is set to 1, the checksum is incorrect.

Bit 5 This is a check, at power-on time, of the Equipment byte. When set to 1, the configuration information is incorrect. Power-on checks require that at least one diskette drive be installed (bit 0 of the Equipment byte, hex 014, is set to 1).

Bit 4 When set to 1, this bit indicates the power-on check determined that the memory size is not the same as in the configuration record.

Bit 3 When set to 1, this bit indicates that the controller or drive C failed initialization, which prevents the system from attempting a power-on reset.

Bit 2 When set to 0, this bit indicates the time is valid. When set to 1, this bit indicates the time is invalid.

Bit 1 This bit indicates if the installed adapters match the configuration information. When this bit is set to 1, the adapters do not match the configuration information.

Bit 0 When set to 1, this bit indicates a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7 - 4	First Diskette Drive Type
3 - 0	Second Diskette Drive Type

Figure 3-44. Diskette Drive Type Byte

Bits 7 - 4 These bits indicate the first diskette drive type, as shown in the following table.

Bits 7 6 5 4	Function
0 0 0 0	No Drive Present
0 0 0 1	Double-Sided Diskette Drive (48 Tracks Per Inch, 360KB)
0 0 1 1	High-Capacity Diskette Drive (720KB)
0 1 0 0	High-Density Diskette Drive (1.44MB)

Note: All combinations that are not shown are reserved.

Figure 3-45. Diskette Drive Type Byte (Bits 7 - 4)

Bits 3 - 0 These bits indicate the second diskette drive type, as shown in the following table.

Bits 3 2 1 0	Function
0 0 0 0	No Drive Present
0 0 0 1	Double-Sided Diskette Drive (48 Tracks Per Inch, 360KB)
0 0 1 1	High-Capacity Diskette Drive (720KB)
0 1 0 0	High-Density Diskette Drive (1.44MB)

Note: All combinations that are not shown are reserved.

Figure 3-46. Diskette Drive Type Byte (Bits 3 - 0)

First Fixed Disk Drive Type Byte (Hex 011): This byte defines the type of the first fixed disk drive (drive C). Hex 00 indicates that a fixed disk drive is *not* installed.

Second Fixed Disk Drive Type Byte (Hex 012): This byte defines the type of the second fixed disk drive (drive D). Hex 00 indicates that a fixed disk drive is *not* installed.

Note: For more information about fixed disk drive types, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Reserved Byte (Hex 013): This byte is reserved.

Equipment Byte (Hex 014): The equipment byte defines (for the power-on diagnostic tests) the basic equipment in the system.

Bit	Function
7, 6	Number of Diskette Drives
5, 4	Display Operating Mode
3, 2	Reserved
1	Math Coprocessor Presence
0	Diskette Drive Presence

Figure 3-47. Equipment Byte

Bits 7, 6 These bits indicate the number of diskette drives installed.

Bits 7 6	Number of Diskette Drives
0 0	One Drive
0 1	Two Drives
1 0	Reserved
1 1	Reserved

Figure 3-48. Equipment Byte (Bits 7, 6)

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-Column Mode
1 0	80-Column Mode
1 1	Monochrome Mode

Figure 3-49. Equipment Byte (Bits 5, 4)

Bits 3, 2 Reserved.

Bit 1 When set to 1, this bit indicates that a math coprocessor is installed.

Bit 0 When set to 1, this bit indicates that a diskette drive is installed.

Low and High Base Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 is equal to 640KB. The low byte is hex 15; the high byte is hex 16.

Low and High Expansion Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The hexadecimal values in these bytes represent the number of 1KB blocks of expansion memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 17; the high byte is hex 18.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 33; the high byte is hex 32.

Reserved Byte (Hex 034): This byte is reserved.

Low and High Useable Memory Bytes (Hex 035 and 036): These bytes define the total amount of useable memory above the 1MB address space.

The hexadecimal values in these bytes represent the number of 1KB blocks of useable memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 35; the high byte is hex 36.

Date Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 through 03F): These bytes are reserved.

Miscellaneous System Functions

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system Watchdog time-out has occurred. The NMI stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts, and the IRET instruction restores the interrupt flag to the state it was in prior to the interrupt. A system reset causes a reset of the NMI.

Nonmaskable interrupt requests from system board parity and channel check are subject to mask control with the NMI mask bit in the RT/CMOS Address register. The Watchdog Timer and system channel time-out are not masked by this bit. (See "RT/CMOS Address Register and NMI Mask (Hex 0070)" on page 3-37). The power-on default of the NMI mask is 1 (NMI disabled). Prior to enabling the NMI after a power-on reset, the parity check and channel check state are initialized by the POST.

Warning: The operation following a write to hex 0070 must access port hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM might occur.

System Control Port B (Hex 0061)

Bit definitions for the read and write functions of this port are shown in the following tables.

Bit	Function
7	Reset Timer 0 Output Latch (IRQ0)
6 - 4	Reserved
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-50. System Control Port B (Write)

Bit	Function
7	Parity Check
6	Channel Check
5	Timer 2 Output
4	Toggles with Each Refresh Request
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-51. System Control Port B (Read)

Bit 7 Setting this bit to 1 resets IRQ0. Reading this bit as a 1 indicates a parity check has occurred.

Bit 6 Reading this bit as a 1 indicates a channel check has occurred.

Bit 5 This bit indicates the condition of the timer 2 'output' signal.

Bit 4 This bit toggles with each refresh request.

Bit 3 Setting this bit to 0 enables channel check. This bit is set to 1 during a power-on reset.

Bit 2 Setting this bit to 0 enables parity check. This bit is set to 1 during a power-on reset.

Bit 1 Setting this bit to 1 enables speaker data.

Bit 0 Setting this bit to 1 enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7, 6	Fixed-Disk Activity Light
5	Reserved
4	Watchdog Timer Status
3	Security Lock Latch
2	Reserved = 0
1	Alternate Gate A20
0	Alternate Hot Reset

Figure 3-52. System Control Port A

Bits 7, 6 These bits control the fixed-disk activity light. Setting either bit to 1 turns the fixed-disk activity light on. Setting both bits to 0 turns the light off. The power-on reset condition of each bit is 0.

Bit 5 Reserved.

Bit 4 This read-only bit indicates the Watchdog Timer status. When this bit is set to 1, a Watchdog time-out has occurred. For more information about the Watchdog Timer, refer to the *Hardware Interface Technical Reference*.

Bit 3 This bit provides the security lock for the secured area of RT/CMOS. Setting this bit to 1 electrically locks the 8-byte, power-on password. Once this bit is set by POST, it can only be cleared by turning the system off.

Bit 2 Reserved.

Bit 1 This bit is used to enable the 'address 20' signal (A20) when the microprocessor is in the real address mode. When this bit is set to 0, A20 cannot be used in real mode addressing. This bit is set to 0 during a system reset.

Bit 0 This bit provides an alternative method of resetting the system microprocessor. This alternative method supports operating systems requiring faster operation than was provided on the IBM Personal Computer AT* Resetting the system microprocessor is used to switch the microprocessor from the protected mode to the real address mode. The alternate reset takes 13.4 microseconds.

This bit is set to 0 either by a system reset or a write operation. When a write operation changes this bit from 0 to 1, the alternate reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is 0, POST assumes the system was just powered on. If the bit is 1, POST assumes a switch from the protected mode to the real mode has taken place.

* Personal Computer AT is a trademark of the International Business Machines Corporation.

Power-On Password

RT/CMOS RAM has eight bytes reserved for the power-on password and its check character. The eight bytes are initialized to hex 00. The microprocessor can access these bytes only during power-on self-test (POST). After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by a program. A power-on password can be from one to seven characters.

During power-on password installation, the password (1 to 7 keyboard scan codes), is stored in the security space.

Power-on password installation is a function of a program on the Reference Diskette. Once the power-on password utility has been installed, the password can be changed only during the POST. When a power-on password is installed, changed, or removed, the password is not visible on the display.

The system unit cover can be physically locked to prevent unauthorized access to the battery. This helps prevent unauthorized battery removal and loss of power-on password and configuration information.

For information about the keyboard password, see the "Keyboard and Auxiliary Device Controller" section in the *Hardware Interface Technical Reference*.

Hardware Compatibility

The Model 80 maintains many of the interfaces used by the IBM Personal Computer AT. In most cases, command and status organization of these interfaces is maintained.

The functional interfaces for the Model 80 are compatible with the following interfaces:

- The Intel** 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).

** Intel is a trademark of the Intel Corporation.

- The Intel 8237 DMA controller-address and transfer counters, page registers, and status fields only. The Command and Request registers are not supported. The rotate and mask functions are not supported. The Mode register is partially supported.
- The NS16450 serial port.
- The Intel 8088, 8086, and 80286 microprocessors.
- The Intel 8272 diskette drive controller.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The Intel 8042 keyboard port at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.
- The Intel 80287 and 8087 math coprocessors.

Error Codes

POST returns a message in the form of a number to indicate the type of test that failed. The following table gives the failure indicated with the associated error code. For information on unlisted error codes, contact Developer Assistance at 1-800-IBM-7763 (this number is for developers who are registered with IBM).

** Motorola is a trademark of Motorola, Incorporated.

Error Number	Error Indication
101	Interrupt failure
102	Timer failure
103	Timer interrupt failure
104	Protected mode failure
105	Keyboard controller command failure
107	Hot MNI test
108	Timer bus test
109	Memory select
110	System board parity
111	I/O parity
112	Watchdog timeout
113	DMA arbitration timeout
114	External ROM checksum
160	System board ID not recognized
161	Bad battery or configuration
162	CMOS checksum or adapter ID mismatch
163	Date and time not set
164	Memory size mismatch
165	Adapter ID mismatch
166	Card busy
167	System clock not updating
201	Memory miscompare or parity
202	Memory address line error (address line 00 - 15)
203	Memory address line error (address line 16 - 31)
211	Memory Base 64K on system board failed
214	Memory Base 64K on daughter/SIP 2 failed
214	Memory Base 64K on daughter/SIP 1 failed
221	ROM to RAM copy
225	Wrong speed memory on system board
301	Keyboard interface
303	Keyboard or system board
304	Keyboard clock failure
305	Keyboard +5V error
601	Diskette Drive or Controller
602	Diskette boot record
1101	Async error
2401	System board video
8601	Mouse timeout
8602	Mouse interface
8603	Mouse interrupt
10480	Drive C seek failure
10481	Drive D seek failure
10482	Drive failed controller test
10483	Driver controller failed to reset
10490	Drive C read failure
10491	Drive D read failure
12901	Failed processor portion of processor board test (Type 3)
12902	Failed cache portion of processor board test (Type 3)

Figure 3-53. Error Codes

Notes:

Index

A

acoustic readings 1-11
activity light 3-49
adapter setup register 2-13
address maps
  memory 3-26
  POS 2-5
  system 1-6
address 20 gate 3-49
alternate reset 3-50
arbiter programming 3-10
arbitration control point 3-9
arbitration level 3-9
arbitration register 3-10
arbitration, central control point 3-10

B

base memory bytes 3-46
battery 3-36
bit values 2-10
bus contention 2-3
bus priority assignments 3-9

C

cached memory 3-13
cache, memory 3-13
card selected feedback 2-5
-CD SFDBK 2-5
central arbitration control point 3-9
channel 1-4, 3-3
channel check enable 3-48
channel check latch 3-48
channel connectors 3-4
CMOS RAM 3-36
configuration CRC bytes 3-46
configuration, RT/CMOS 3-42
connectors, memory 3-33
connector, matched memory 3-4
coprocessor, math 3-3
cycles
  matched memory 3-6
  synchronous extended 3-6

D

date century byte 3-46
default 3-6
description
  memory 3-12
  NMI 3-47
  password 3-51
  programmable option select 2-3
  real-time clock 3-36
  system 1-3
  system board 1-3
description, power supply 1-12
diagnostic status byte (RT/CMOS) 3-42
diskette drive type byte 3-43
diskette overruns 3-9

E

enable error checking 3-22
enable NMI 3-37
encoding registers, type 2 3-20
encoding register, type 1 3-17
equipment byte 3-45
error recovery 3-15
extended arbitration 3-11
extension, matched memory 3-4

F

fault, overvoltage 1-13
feedback, card selected 2-5
fixed disk activity light 3-49
fixed disk drive activity light 1-12
fixed disk drive initialization 3-42
fixed disk type byte 3-44

© Copyright IBM Corp. 1989, 1990

G

gate A20 3-49

I

identifier, model 1-3
interrupts
  IRQ0 reset 3-48
  NMI reset 3-47
I/O address map 1-6

L

light, fixed disk drive activity 1-12
light, power 1-12
list of features 1-4

M

matched memory 3-3, 3-4
matched memory cycle 3-6
matched memory extension 3-4
math coprocessor 3-3
maximum current 1-10
measurements 1-10
memory
  addressing 3-16
  available memory 2-8
  cached 3-13
  channel RAM 3-27
  channel ROM 3-27
  connectors 3-33
  description 3-12
  encoding registers, Type 1 3-16
  encoding registers, Type 3 3-23
  encoding register, type 2 3-20
  error recovery 3-15
  maps 3-26, 3-27
  matched memory cycle 3-6
  matched memory timing (no waits) 3-7
  nonsystem 3-13
  performance 1-7
  POS register 3, type 2 2-10
  POST routines 3-12, 3-34
  random access memory subsystem 3-12
memory *(continued)*
  read-only Type 1 3-12
  reassigning 3-15
  refresh 3-9
  registers, Type 2 3-20
  ROM enable 3-18
  signals 3-33, 3-35
  split 3-16, 3-18
  split address, Type 1 3-19
  split block 3-21
  split-memory block 3-16
  support 3-12
  system board 3-27
  system memory maps 3-26
  video 3-27
memory caching 3-13
memory connector location 2-8, 2-10
memory size miscompare 3-42
micro channel 1-4, 3-3
microprocessor
  alternate reset 3-50
  mode switch compatibility 3-50
  performance 1-7
  real address mode 3-49
microprocessor cache 3-13
-MMC 3-5
-MMC CMD 3-5
-MMCR 3-5
mode switching 3-50
model/submodel bytes 1-3

N

NMI mask 3-37
NMI service 3-9
NMI signal 3-9
noise readings 1-11
nonmaskable interrupt (NMI) 3-47
nonsystem memory 3-13

O

output voltage sequencing 1-13
outputs, power supply 1-12
overvoltage fault 1-13

P

parallel port select 2-7
parity check 3-22
parity check enable 3-48
password, power-on 3-51
performance 1-7, 3-3
ports, system control 3-47
POS register 2 2-7
POS register 3, type 1 2-8
POS register 3, type 2 2-10
power specifications 1-10
power supply 1-4
power supply description 1-12
power supply LED 1-12
power supply output protection 1-13
power supply outputs 1-12
programmable option select (POS) 2-3
  address decode 2-5
  address map 2-5
  registers 2-5
  setup procedures 2-3
  setup register 2-6
  system board 2-6
  system board I/O 2-7
  system configuration utilities 2-3
  system memory maps 3-26
  video 2-6
  warning 2-3
programming, arbiter 3-10
protected mode switch 3-50
protection, power supply 1-13

R

RAM 3-12
random access memory 3-12
read-only memory, Type 1 3-12
read-only memory, Type 2 3-12
read-only memory, Type 3 3-12
real mode switch 3-50
real-time clock bytes 3-39
refresh 3-9
refresh request 3-48
registers
  adapter setup 2-13
  card feedback 2-5
  memory encoding, type 1 3-17
  memory encoding, type 2 3-20
  miscellaneous system 3-47
  RT/CMOS and NMI mask 3-37
  RT/CMOS status registers 3-39
  split address—Type 1 3-19
  system board POS 2-6
  system control 3-47
ROM enable 3-21
ROM Type 2 3-12
ROM Type 3 3-12
RT/CMOS address register 3-37
RT/CMOS RAM 3-36
  password 3-51
  secured area 3-49
R1,R2 bit values 2-10

S

second fixed disk type byte 3-44
sequencing, output voltage 1-13
setup
  bus contention 2-3
  memory encoding register—type 2 3-20
  memory split 3-18
  POS register 3, type 1 2-8
  POS register 3, type 2 2-10
  registers 2-6
  ROM enable 3-18
  split memory address, Type 1 3-19
  system board 2-6
  system board I/O 2-7
  system memory maps 3-26
  video 2-6
shutdown status byte 3-43
signals
  -MMC 3-5
  -MMC CMD 3-5
  -MMCR 3-5
  matched memory 3-4, 3-5
  memory 3-33, 3-35

size 1-10
sound specifications 1-11
speaker data enable 3-48
specifications, system unit 1-10
split address register—Type 1 3-19
split memory block 3-16, 3-21
status registers (RT/CMOS) 3-39
subsystems, memory 3-12
switch to real 3-50
system address map 1-6
system board 1-3
  features 1-3
  I/O register 2-7
  memory connectors 3-33
  memory map 3-27
  model identifier 1-3
  POS registers 2-6
  setup 2-6
system configuration utilities 2-3
system control port A 3-49
system control ports 3-47
system description 1-3
system memory 3-13
system performance 1-7
system ports, miscellaneous 3-47
system reset 3-47
system unit specifications 1-10

T

time status indicator 3-42
timing
  matched memory (no waits) 3-7
type identifier 1-3
T1,T2 bit values 2-10

V

valid RAM bit 3-41
video setup 2-6

W

warnings
  arbitration 3-9
  central arbiter 3-11
  NMI mask 3-47
warnings *(continued)*
  POS 2-3
  real-time clock 3-37
  reserved areas v
watchdog status 3-49

Numerics

80386 performance 1-7
80387 math coprocessor 3-3

Personal System/2
Model 90 XP 486
Technical Reference

Note

Before using this information and the product it supports, be sure to read the general information under "Notices" on page xi.

Fourth Edition (June 1992)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer of express or implied warranties in certain transactions, therefore, this statement may not apply to you.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Requests for technical information about IBM products should be made to your IBM Authorized Dealer or your IBM Marketing Representative.

© Copyright International Business Machines Corporation 1990, 1992. All rights reserved.
Note to U.S. Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Contents

Figures vii

Notices xi
Trademarks and Service Marks xi

Preface xiii

Section 1. System Overview 1-1
| Description 1-3
| System Board Devices and Features 1-3
| Processor Complex 1-5
System Board I/O Address Map 1-6
| Micro Channel Compatibility 1-7
Specifications 1-9
Power Supply 1-10
Outputs 1-11
Output Protection 1-12
Voltage Sequencing 1-12
Power Supply Connectors 1-12

Section 2. Programmable Option Select 2-1
Description 2-3
POS Address Map 2-5
Card Selected Feedback Register (Hex 0091) 2-6
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-6
System Board POS Register 2 (Hex 0102) 2-7
| System Board POS Register 3 (Hex 0103) 2-9
System Board POS Registers 4 (Hex 0104) 2-10
System Board POS Register 5 (Hex 0105) 2-11
Diskette Drive POS Register 4 (Hex 0104) 2-12
Adapter Enable/Setup Register (Hex 0096) 2-13
Second Serial Port POS Register 2 (Hex 0102) 2-14
Second Serial Port POS Register 4 (Hex 0104) 2-14
Second Serial Port POS Register 5 (Hex 0105) 2-15

Section 3. System Board 3-1
| Description 3-3
Micro Channel Implementation 3-3
| Central Arbiter 3-3
Diskette Drive Connector 3-7
| System Board Memory Connectors 3-8

© Copyright IBM Corp. 1990, 1992

| Real-Time Clock/Complementary Metal-Oxide Semiconductor
| (RT/CMOS) RAM 3-10
RT/CMOS Address Register and NMI Mask (Hex 0070) 3-11
RT/CMOS Data Register (Hex 0071) 3-11
RT/CMOS RAM I/O Operations 3-12
Real-Time Clock Bytes (Hex 000–00D) 3-13
| CMOS RAM Configuration 3-17
Miscellaneous System Functions and Ports 3-21
Nonmaskable Interrupt 3-21
| System Control Port B (Hex 0061) 3-22
System Control Port A (Hex 0092) 3-23
Power-On Password 3-25
Selectable Boot Sequence 3-26
Hardware Compatibility 3-27
| Error Codes 3-28

Section 4. Type 1 Processor Complexes 4-1
| Description 4-3
| Type 1A 4-4
| Type 1B 4-7
| Type 1C 4-10
| Type 1D 4-13
Type 1 Processor Complexes—I/O Address Map 4-15
| Type 1 Processor Complexes—Level 2 Cache 4-15
Type 1 Processor Complexes—Memory Subsystem 4-15
| Type 1 Processor Complexes—Memory Presence Detect . . . 4-16
| Type 1 Processor Complexes—Cache Address Map 4-17
Type 1 Processor Complexes—Read-Only Memory Subsystem 4-19

Section 5. Type 2 Processor Complexes 5-1
| Description 5-3
| Type 2A 5-4
| Type 2B 5-7
Type 2 Processor Complexes—I/O Address Map 5-10
| Type 2 Processor Complexes—Level 2 Cache 5-10
| Type 2 Processor Complexes—Memory Subsystem 5-10
| Type 2 Processor Complexes—Memory Presence Detect . . . 5-11
| Type 2 Processor Complexes—Cache Address Map 5-12
Type 2 Processor Complexes—Read-Only Memory Subsystem 5-14

| **Section 6. Type 3 Processor Complexes** 6-1
| Description 6-3
| Type 3A 6-4
| Type 3 Processor Complexes—I/O Address Map 6-7
| Type 3 Processor Complexes—Level 2 Cache 6-7
| Type 3 Processor Complexes—Memory Subsystem 6-8

| Type 3 Processor Complexes—Memory Presence Detect 6-9
| Type 3 Processor Complexes—Cache Address Map 6-10
| Type 3 Processor Complexes—Read-Only Memory Subsystem 6-12

Index X-1

Notes:

Figures

1-1. System Board Devices and Features 1-3
1-2. Processor Complexes 1-5
1-3. System Board I/O Address Map 1-6
1-4. Physical Specifications 1-9
1-5. Acoustical Readings 1-10
1-6. Power Provided for Internal Devices 1-11
1-7. Load Current for the Micro Channel Connectors 1-11
1-8. Voltage Assignments for the Internal Power-Supply Connectors 1-12
2-1. POS I/O Address Map 2-5
2-2. Card Selected Feedback Register (Hex 0091) 2-6
2-3. System Board Enable/Setup Register (Hex 0094) 2-7
2-4. System Board POS Register 2 (Hex 0102) 2-8
2-5. Parallel Port Select Bits 2-8
2-6. System Board POS Register 3 (Hex 0103)—Write 2-9
2-7. System Board POS Register 3 (Hex 0103)—Read 2-9
2-8. Error-Checking Information 2-10
2-9. System Board POS Register 4 (Hex 0104) 2-10
2-10. System Board POS Register 5 (Hex 0105) 2-11
2-11. Primary Serial Port Address Select Bits 2-11
2-12. Diskette Drive POS Register 4 (Hex 0104) 2-12
2-13. Adapter Enable/Setup Register (Hex 0096) 2-13
2-14. Second Serial Port POS Register 2 (Hex 0102) 2-14
2-15. Second Serial Port POS Register 4 (Hex 0104) 2-14
2-16. Second Serial Port POS Register 5 (Hex 0105) 2-15
2-17. Second Serial Port Address Select Bits 2-15
3-1. Arbitration Bus Priority Assignments 3-4
3-2. Arbitration Register (Hex 0090)—Write 3-5
3-3. Arbitration Register (Hex 0090)—Read 3-5
3-4. Diskette Drive Connector 3-7
3-5. Memory Connector Numbering 3-8
3-6. System Board Memory Connector 3-9
3-7. RT/CMOS RAM Address Map 3-10
3-8. RT/CMOS Address Register and NMI Mask (Hex 0070) 3-11
3-9. RT/CMOS Data Register (Hex 0071) 3-11
3-10. Real-Time Clock Bytes (Hex 000−00D) 3-13
3-11. Status Register A (Hex 00A) 3-14
3-12. Status Register B (Hex 00B) 3-14
3-13. Status Register C (Hex 00C) 3-16
3-14. Status Register D (Hex 00D) 3-16
3-15. Diagnostic Status Byte (Hex 00E) 3-17
3-16. Diskette Drive Type Byte (Hex 010) 3-18

© Copyright IBM Corp. 1990, 1992

3-17. First Diskette Drive Type Byte (Bits 7–4) 3-18
3-18. Second Diskette Drive Type Byte (Bits 3–0) 3-18
3-19. Equipment Byte (Hex 014) 3-19
3-20. Equipment Byte (Bits 7, 6) 3-19
3-21. Equipment Byte (Bits 5, 4) 3-19
3-22. System Control Port B (Hex 0061)—Write 3-22
3-23. System Control Port B (Hex 0061)—Read 3-22
3-24. System Control Port A (Hex 0092) 3-23
3-25. POST Error Messages 3-29
4-1. Type 1 Processor Complexes—Model and Submodel Bytes 4-3
4-2. Type 1A Processor Complex—Features and Devices . . 4-4
4-3. Type 1A Processor Complex—System Performance Specifications 4-5
4-4. Type 1A Processor Complex—Memory Performance Specifications, ... 4-6
4-5. Type 1B Processor Complex—Features and Devices . . 4-7
4-6. Type 1B Processor Complex—System Performance Specifications 4-8
4-7. Type 1B Processor Complex—Memory Performance Specifications 4-9
4-8. Type 1C Processor Complex—Features and Devices . 4-10
4-9. Type 1C Processor Complex—System Performance Specifications 4-11
4-10. Type 1C Processor Complex—Memory Performance Specifications 4-12
4-11. Type 1D Processor Complex—Features and Devices . 4-13
4-12. Type 1D Processor Complex—System Performance Specifications 4-14
4-13. Type 1D Processor Complex—Memory Performance Specifications 4-14
4-14. Type 1 Processor Complexes—I/O Address Map 4-15
4-15. Type 1 Processor Complexes—Presence-Detect Bits . 4-16
4-16. Type 1 Processor Complexes—Cache Address Map Summary 4-18
5-1. Type 2 Processor Complexes—Model and Submodel Bytes 5-3
5-2. Type 2A Processor Complex—Features and Devices . . 5-4
5-3. Type 2A Processor Complex—System Performance Specifications 5-5
5-4. Type 2A Processor Complex—Memory Performance Specifications 5-6
5-5. Type 2B Processor Complex—Features and Devices . . 5-7
5-6. Type 2B Processor Complex—System Performance Specifications 5-8

5-7. Type 2B Processor Complex—Memory Performance Specifications 5-9
5-8. Type 2 Processor Complexes—I/O Address Map 5-10
5-9. Type 2 Processor Complexes—Presence-Detect Bits . 5-11
5-10. Type 2 Processor Complexes—Cache Address Map Summary 5-13
6-1. Type 3 Processor Complexes—Model and Submodel Bytes 6-3
6-2. Type 3A Processor Complex—Features and Devices . . 6-4
6-3. Type 3A Processor Complex—System Performance Specifications 6-5
6-4. Type 3A Processor Complex—Memory Performance Specifications 6-6
6-5. Type 3A Processor Complex—Channel Bus Master Performance Specifications 6-7
6-6. Type 3 Processor Complexes—I/O Address Map 6-7
6-7. Type 3 Processor Complexes—Presence-Detect Bits . . 6-9
6-8. Type 3 Processor Complexes—Cache Address Map Summary 6-11

Notes:

Notices

References in this publication to IBM products, programs, or services do not imply that IBM intends to make these available in all countries in which IBM operates. Any reference to an IBM product, program or service is not intended to state or imply that only IBM's product, program, or service may be used. Any functionally equivalent product, program, or service that does not infringe any of IBM's intellectual property rights or other legally protectible rights may be used instead of the IBM product, program, or service. Evaluation and verification of operation in conjunction with other products, programs, or services, except those expressly designated by IBM, are the user's responsibility.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

Trademarks and Service Marks

The following terms, denoted by an asterisk (*) used in this publication, are trademarks of the IBM Corporation in the United States or other countries:

IBM
Micro Channel
Personal Computer AT
Personal System/2
PS/2
XGA

The following terms, denoted by a double asterisk (**) used in this publication, are trademarks of other companies as follows:

Intel	Intel Corporation
Intel486	Intel Corporation
Intel487	Intel Corporation
Motorola	Motorola, Incorporated
National Semiconductor	National Semiconductor Corporation

© Copyright IBM Corp. 1990, 1992

Notes:

Preface

The Technical Reference library is intended for those who develop hardware and software products for IBM Personal Computers and IBM Personal System/2 products. Users should understand computer architecture and programming concepts.

| Additions and changes have been made since the third edition of this
| manual. New or changed information is marked in the text with the
| same mark that is in the margin of this text.

This manual consists of the following sections:

Section 1, "System Overview," describes the system, features, and specifications.

Section 2, "Programmable Option Select," describes the registers used for configuration.

Section 3, "System Board," describes the system-specific hardware implementations of the Micro Channel architecture.

| Section 4, "Type 1 Processor Complexes," describes the
| components and features of the type 1 processor complexes.

| Section 5, "Type 2 Processor Complexes," describes the
| components and features of the type 2 processor complexes.

| Section 6, "Type 3 Processor Complexes," describes the
| components and features of the type 3 processor complexes.

Warning: The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

© Copyright IBM Corp. 1990, 1992

This technical reference should be used with the following publications. These publications contain additional information on many of the subjects discussed in this technical reference.

IBM Personal System/2 Hardware Interface Technical Reference—Architectures

IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference

Information about diskette drives, fixed disk drives, adapters, and external options are in separate option technical references.

Section 1. System Overview

| Description 1-3
| System Board Devices and Features 1-3
| Processor Complex 1-5
System Board I/O Address Map 1-6
| Micro Channel Compatibility 1-7
Specifications 1-9
Power Supply 1-10
  Outputs 1-11
  Output Protection 1-12
  Voltage Sequencing 1-12
  Power Supply Connectors 1-12

© Copyright IBM Corp. 1990, 1992

Notes:

Description

The IBM* Personal System/2* (PS/2*) Model 90 XP 486 is a self-contained, desktop computer system with a keyboard. The system can support a maximum of four internal drives. Three of these drives can be removable-media direct access storage devices (DASD) (diskette, tape, or optical) or three can be nonremovable-media DASD devices.

All Model 90 XP 486 systems use the same system board. The system board has:

- Four Micro Channel* connectors
- Extended Graphics Array (XGA*) Video Subsystem
- Diskette drive, parallel port, and two serial port controllers
- Keyboard connector
- Pointing-device connector
- Eight memory connectors on two riser cards
- Processor complex connector
- 64-byte complementary metal-oxide semiconductor (CMOS) random access memory (RAM)
- Real-time clock.

System Board Devices and Features

The following figure lists the system board devices and features. The *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* describes devices common to PS/2 products by type number.

Device	Type	Features
Microprocessor	---	Connector for processor complex (see Figure 1-2 on page 1-5)
System Timers	1	Channel 0—System timer Channel 2—Tone generation for speaker Channel 3—Watchdog timer
RAM Subsystem	---	Two riser cards provide eight connectors Refer to the processor complex for more information

Figure 1-1 (Part 1 of 2). System Board Devices and Features

* Trademark of the IBM Corporation.

Device	Type	Features
CMOS RAM Subsystem	—	64-byte CMOS RAM with real-time clock/calendar 8KB CMOS RAM extension (KB equals 1024 bytes) Battery backup
Audio Subsystem	1	Driven by —System-timer channel 2 —The 'audio sum node' signal
Video Subsystem	2	XGA video functions —VGA mode —132 column mode —Extended graphics mode 512KB or 1MB of video memory
Interrupt Controller	1	16 levels of system interrupts Interrupts are level sensitive
Keyboard/Auxiliary Device Controller	2	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	2	Supports —3.5-in. diskette drive (1.44MB) —5.25-in. diskette drive (360KB and 1.2MB) —3.5-in. diskette drive (2.88MB)†
Serial Port Controller	3	Two RS-232C interfaces —One 25-pin connector (primary serial) —One 9-pin connector (second serial) Programmable as serial ports 1–8 DMA, FIFO, and character modes
Parallel Port Controller	3	Programmable as parallel ports 1–4 Supports bidirectional input and output Supports DMA operation
Micro Channel	—	Four connectors for Type 3 adapters —One 32-bit connector with an auxiliary video extension —Three 32-bit connectors with matched memory extension One connector contains a fixed-disk adapter

† Not supported in all Model 90 XP 486 systems.

Figure 1-1 (Part 2 of 2). System Board Devices and Features

Processor Complex

The functions of the system can be changed depending on which processor complex is installed. The processor complex determines the model/submodel byte information. The major components on the processor complex are:

- System microprocessor
- System clock
- Direct memory access (DMA) controller
- Memory controller.

The processor complexes fall into one of three types (type 1, 2, or 3) depending on the following:

- Type of DMA controller installed (16- or 32-bit)
- Type of memory error detection supported (parity or ECC)
- Type of memory configuration supported (interleaved or noninterleaved).

The following figure lists the different processor complexes.

Processor Complex	Processor—Speed	Memory (Interleaved, Noninterleaved, or Both)	Error Detection (Parity, ECC, or Both)	Page
Type 1A	80486DX—25 MHz	Interleaved	Parity	4-4
Type 1B	80486DX—33 MHz	Interleaved	Parity	4-7
Type 1C	80486SX—20 MHz	Interleaved	Parity	4-10
Type 1D	80486DX—50 MHz	Interleaved	Parity	4-13
Type 2A	80486SX—25 MHz	Both	Parity	5-4
Type 2B	80486DX2—50 MHz	Both	Parity	5-7
Type 3A	80486DX—50 MHz	Interleaved	Both†	6-4

† The systems use *either* parity or ECC to detect memory errors *(but not a combination of both)*.

Figure 1-2. Processor Complexes

System Board I/O Address Map

Address (Hex)	Device
0020, 0021	Interrupt controller
0040, 0042–0044, 0047	System timers
0060	Keyboard, auxiliary device
0061	System Control Port B
0064	Keyboard, auxiliary device
0070, 0071	RT/CMOS and NMI mask
0091	Card Selected Feedback register
0092	System Control Port A
0094	System Board Enable/Setup register
0096	Adapter Enable/Setup register
00A0–00A1	Interrupt controller
0100–0107	Programmable option select
0108–010F	Information panel
0278–027D	Parallel port 3
02F8–02FF	Serial port 2
0378–037D	Parallel port 2
03B4–03BB	Video subsystem
03BC–03BF	Parallel port 1
03C0–03CF	Video subsystem
03D4–03DB	Video subsystem
03F0–03F7	Diskette drive controller
03F8–03FF	Serial port 1
1278–127D	Parallel port 1 (DMA mode)
1378–137D	Parallel port 4
2100–217F	Video subsystem
3220–3227	Serial port 3
3228–322F	Serial port 4
4220–4227	Serial port 5
4228–422F	Serial port 6
5220–5227	Serial port 7
5228–522F	Serial port 8
83F8–83FF	Serial port 1 (DMA mode)
82F8–82FF	Serial port 2 (DMA mode)
B220–B227	Serial port 3 (DMA mode)
B228–B22F	Serial port 4 (DMA mode)
C220–C227	Serial port 5 (DMA mode)
C228–C22F	Serial port 6 (DMA mode)
D220–D227	Serial port 7 (DMA mode)
D228–D22F	Serial port 8 (DMA mode)

Figure 1-3. System Board I/O Address Map

Micro Channel Compatibility

The following describes the system limitations in the support of Micro Channel procedures.

Streaming Data

The system board supports 10-MHz streaming-data procedures involving transfers between adapters.

Devices on the system board and the processor complex work with streaming-data adapters; however, they do not use the streaming-data procedure. Transfers default to the basic transfer procedure.

The exception is systems with the type 3A processor complex, which support the 16- and 32-bit, 100 nanoseconds streaming-data procedure. Masters accessing system board memory will receive a request to use the streaming-data procedure.

Data Parity

The system board supports data-parity procedures involving transfers between adapters.

Devices on the system board and the processor complex work with adapters that support data parity; however, they do not use the data-parity option. Transfers default to the basic transfer procedure.

The exception is systems with the type 3A processor complex, which support the data-parity option. Masters accessing system board memory, and slaves being addressed by the system master, will exchange data with parity included only if the given adapter supports the data-parity procedure.

Address Parity

The system board supports address-parity procedures involving transfers between adapters.

Devices on the system board and the processor complex work with adapters that support address parity; however, they do not use the address-parity option. Transfers default to the basic transfer procedure.

Selected Feedback Return Signal

Most system boards and processor complexes support the 'selected feedback return' signal, except for I/O devices at addresses below hex 0110. These devices are controlled

by the system master only and should not be accessed by bus masters.

The exception is systems with type 2 processor complexes, which do not support the 'selected feedback return' signal.

Synchronous Channel Check

Synchronous channel checks for exceptions other than Micro Channel data-parity exceptions, Micro Channel address-parity exceptions, and slave dependent exceptions generally are not supported in this system. The channel check exception reporting field in adapter POS will be set to disable synchronous channel checks and enable asynchronous channel checks.

The exception is systems with the type 3A processor complex. In these systems, all synchronous channel checks can be enabled.

Synchronous channel checks for slave dependent exceptions, Micro Channel data-parity exceptions, or Micro Channel address-parity exceptions, typically issued by slaves, are the responsibility of the master that owned the channel and issued the access to the slave. However, in this system, these channel checks can also be detected by logic on the system board, resulting in a nonmaskable interrupt (NMI).

DMA

In most systems, the DMA controller supports DMA slaves with 8-bit or 16-bit data widths. Transfers are limited to the memory address space below 16MB.

The exception is systems with the type 3A processor complex. In these systems, the DMA controller supports 8-bit, 16-bit, and 32-bit data widths. It can address memory space above 16MB. See the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* for more information.

Specifications

Size	
Width	440 mm (17.3 in.)
Depth	430 mm (16.9 in.)
Height	140 mm (5.5 in.)
Weight	12 kg (26 lb)
Cables	
Power cable	1.8 m (6 ft)
Keyboard cable	1.8 m (6 ft)
Air Temperature	
System on	
0 – 3000 ft	10.0 to 35.0°C (50 to 95°F)
3000 – 7000 ft	10.0 to 32.2°C (50 to 90°F)
System off	10.0 to 43.0°C (50 to 110°F)
Humidity	8% to 80%
Maximum Altitude	2134 m (7000 ft)
Heat Output	329 W (1125 BTU per hour)
Acoustical Readings	See Figure 1-5 on page 1-10
Electrical	
Input voltage	Range is automatically selected Sinewave input required
Low range	90 (min) to 137 (max) V ac
High range	180 (min) to 265 (max) V ac
Input frequency	50 Hz ± 3 Hz or 60 Hz ± 3 Hz
Maximum current draw	
Low range	4.8 A
High range	2.4 A
Input in kilovolt-ampere (kVA)	
Minimum configuration (as shipped)	0.15 kVa
Maximum configuration	0.48 kVa
Electromagnetic Compatibility	FCC Class B

Figure 1-4. Physical Specifications

Description	L_{WAd} in bels		L_{pAm} in dB		$<L_{pA}>_m$ in dB	
	Operate	Idle	Operate	Idle	Operate	Idle
Model 90 XP 486	5.1	5.1	43	43	37	37

Notes:

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

All measurements are made in accordance with ANSI standard 12.10 and are reported in conformance with ISO DIS 9296.

The measurements are preliminary data and are subject to change.

Figure 1-5. Acoustical Readings

Power Supply

The power supply requires a sinewave input and converts the ac input voltage to three dc output voltages. The power supply automatically adjusts to match the input voltage range. The power supply provides power for the following:

- System board
- Processor complex
- Micro Channel adapters
- Internal diskette drives
- Internal fixed disk drives
- Auxiliary device
- Keyboard.

The power switch and two light-emitting diodes (LED) are on the front of the system unit. The power supply is operating properly when the green LED is lit. The amber LED is the fixed-disk-activity indicator.

Outputs

The power supply provides separate voltage sources for the system board and the drives. The system board voltages are +5 V dc, +12 V dc, and −12 V dc. The voltages for the internal drives are +5 V dc and +12 V dc. The following is the approximate power provided for system components.

System Component	Maximum Current	
	+12 V dc	+5 V dc
Internal fixed disk drives†	3.2 A	2.3 A
Auxiliary device		300 mA
Keyboard		275 mA
† Total for both power supply connectors		

Figure 1-6. Power Provided for Internal Devices

The following are the load currents allowed for the connectors for the Type 3 Micro Channel adapters. The formulas used to determine the power requirements and the definition of adapter types can be found in the section of the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures* that describes the Micro Channel architecture.

Supply Voltage	Maximum Current
+ 5.0 V dc	2.0 A
+12.0 V dc	0.175 A
−12.0 V dc	0.040 A

Figure 1-7. Load Current for the Micro Channel Connectors

Output Protection

A short circuit placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state with no damage to the power supply.

If an overvoltage fault occurs (internal to the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of the nominal value of the power supply.

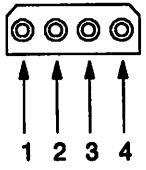
If either of these shutdown states occurs, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least one second.

Voltage Sequencing

At power-on, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Power Supply Connectors

The power supply provides two 4-pin connectors for internal devices. The total power used by both connectors must not exceed the amount shown in Figure 1-6 on page 1-11.



Pin	Signal	Pin	Signal
1	+12 V dc	3	dc return
2	dc return	4	+5 V dc

Figure 1-8. Voltage Assignments for the Internal Power-Supply Connectors

Section 2. Programmable Option Select

Description 2-3
POS Address Map 2-5
Card Selected Feedback Register (Hex 0091) 2-6
System Board Setup 2-6
System Board Enable/Setup Register (Hex 0094) 2-6
System Board POS Register 2 (Hex 0102) 2-7
System Board POS Register 3 (Hex 0103) 2-9
System Board POS Registers 4 (Hex 0104) 2-10
System Board POS Register 5 (Hex 0105) 2-11
Diskette Drive POS Register 4 (Hex 0104) 2-12
Adapter Enable/Setup Register (Hex 0096) 2-13
Second Serial Port POS Register 2 (Hex 0102) 2-14
Second Serial Port POS Register 4 (Hex 0104) 2-14
Second Serial Port POS Register 5 (Hex 0105) 2-15

© Copyright IBM Corp. 1990, 1992

Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used on the Model 90 XP 486 system board. For additional POS information, refer to the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures.*

Warning:

- IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignment of the same system resource, improper operation of the feature, loss of data, or possible damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention will occur, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- Bit 7 (channel reset) in the Adapter Enable/Setup register must be set to 0 to program the adapters.
- Only 8-bit instructions are supported for setup operations. Using 32- or 16-bit I/O instructions on 8-bit POS registers will cause erroneous data to be written or read.

Setup functions respond to I/O addresses hex 0100 through 0107 only when their unique setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

Primary System Board Setup:

- Bit 7 must be set to 0 while other bits in the System Board Enable/Setup register (hex 0094) are set to 1 to set up the primary system board functions.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.

System Board Video Subsystem Setup:

- Bit 5 in the System Board Enable/Setup register must be set to 0 to place the system board video into the setup mode.
- Bits 7 and 6 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.

Diskette Drive Setup:

- Bit 6 must be set to 0 while other bits in the System Board Enable/Setup register are set to 1 to set up the diskette drive functions on the system board.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.

Second Serial Port Setup:

- Only bits 3, 2, and 0 in the Adapter Enable/Setup register are set to 1 to set up the second serial port on the system board (9-pin connector).
- Bits 7–0 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system board functions.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register must be set to 1 to allow adapter setup.
- Bits 7–0 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to system board functions.

POS Address Map

The following figure shows the organization of the I/O address space used by POS. Bit 0 of POS Register 2 and bits 6 and 7 of POS Register 5 are fixed. All other bits in POS Registers 2 through 5 are free form.

Address (Hex)	Function
0094	System Board Enable/Setup register
0096	Adapter Enable/Setup register
0100	POS Register 0—Adapter Identification byte (low byte)
0101	POS Register 1—Adapter Identification byte (high byte)
0102	POS Register 2—Option Select Data byte 1 Bit 0 is card enable.
0103	POS Register 3—Option Select Data byte 2
0104	POS Register 4—Option Select Data byte 3
0105	POS Register 5—Option Select Data byte 4
0106	Reserved
0107	Reserved

Figure 2-1. POS I/O Address Map

Card Selected Feedback Register (Hex 0091)

When an adapter is addressed, it responds by setting the '-card selected feedback' signal (-CD SFDBK) to active. -CD SFDBK is derived from the address decode and driven by a totem pole driver. It is latched by the system board and can be read through the Card Selected Feedback register at address hex 0091.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and thereby determine if the system board I/O or an adapter is addressed and functioning.

Bit	Function
7–1	Reserved
0	-Card selected feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7–1 These bits are reserved.

Bit 0 This bit is set to 1 when -CD SFDBK was active on a previous cycle or when the system board I/O functions (diskette drive, primary serial, or parallel interfaces) are accessed by an I/O or DMA cycle. Reading this register resets this bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information during setup. The diskette drive controller, primary serial port, and parallel port are treated as a single device. The video subsystem is treated as a second, separate device on the system board. The System Board Enable/Setup register is used to place the system board into the setup mode.

System Board Enable/Setup Register (Hex 0094)

This is a read/write register; all bits in this register default to 1 (enabled). Setup functions should be accessed only one at a time.

Bit	Function
7	Enable/setup system board functions
6	Enable/setup diskette drive functions
5	Enable/setup video subsystem
4–0	Reserved

Figure 2-3. System Board Enable/Setup Register (Hex 0094)

Bit 7 When this bit is set to 0, various system board I/O functions are placed in the setup mode. The diskette drive controller, primary serial port, and parallel port are controlled through System Board POS Register 2 (hex 0102).

When this bit is set to 1, the system board function is enabled.

Bit 6 Additional setup for diskette drive. When this bit is set to 0, these setup functions are available through the Diskette Drive POS Register 4.

Bit 5 When this bit is set to 0, the video subsystem is placed in setup mode. While in setup mode, the video subsystem is controlled through the video subsystem POS registers. When bit 5 is set to 1, the video subsystem is enabled. (See the Video Subsystem section of the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* for operation of the POS registers).

Bits 4–0 These bits are reserved.

System Board POS Register 2 (Hex 0102)

When the system board is in the setup mode, the diskette drive controller, primary serial port, and parallel port are controlled by this read/write register. Reading this register returns the current state of these system board functions.

Bit	Function
7	Disable parallel port extended mode
6, 5	Select parallel port
4	Enable parallel port
3	Select primary serial IRQ
2	Enable primary serial port
1	Enable diskette drive interface
0	Enable system board

Figure 2-4. System Board POS Register 2 (Hex 0102)

Bit 7 When set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional (extended mode) interface. When set to 1, this bit disables the bidirectional mode. This bit is set to 0 after power-on.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Address (Hex)	Interrupt Level
0 0	Parallel 1	03BC–03BF†	7
0 1	Parallel 2	0378–037D	7
1 0	Parallel 3	0278–027D	7
1 1	Parallel 4	1378–137D	7

† The addresses are hex 1278–127D for the DMA operations.

Figure 2-5. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bit 3 When this bit is set to 1, the primary serial port (25-pin connector) uses interrupt request level 4. When this bit is set to 0, the primary serial port uses interrupt request level 3.

Bit 2 When this bit and bit 0 are set to 1, the primary serial port is enabled.

Bit 1 When this bit and bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When set to 1, this bit allows bits 4, 2, and 1 to enable and disable their respective devices. When set to 0, this bit disables the diskette drive interface, primary system board serial port, and system board parallel port, regardless of the state of bits 4, 2, and 1.

System Board POS Register 3 (Hex 0103)

The system board has connectors that provide for installation of eight single inline memory modules (also called *memory modules*) (for more information about these memory connectors, see "System Board Memory Connectors" on page 3-8). Information about each memory module is contained in four read-only data registers; each data register is selected by writing its index to the write-only index register.

POS Register 3 provides access to the read-only data registers and a write-only index register. To determine the memory information for a particular connector, write the appropriate index to POS Register 3, then read POS Register 3. The following figure shows the relationship of the index value, the memory connector, and the available data register information.

Index Value (Hex)	Description
01	Presence detect information for A1 and B1
05	Presence detect information for A2 and B2
09	Presence detect information for A3 and B3
0D	Presence detect information for A4 and B4
10	Error-checking information for all connectors
Note: Values that are not shown are reserved.	

Figure 2-6. System Board POS Register 3 (Hex 0103)—Write

The following information is returned by reading POS Register 3 when the appropriate index value is written to POS Register 3. For coding of the presence detect signals, see Figure 4-15 on page 4-16, Figure 5-9 on page 5-11, and Figure 6-7 on page 6-9.

Bit	Description
7	Presence detect 3, connector B
6	Presence detect 2, connector B
5	Presence detect 1, connector B
4	Presence detect 0, connector B
3	Presence detect 3, connector A
2	Presence detect 2, connector A
1	Presence detect 1, connector A
0	Presence detect 0, connector A

Figure 2-7. System Board POS Register 3 (Hex 0103)—Read

The following information is returned when index value hex 10 is selected.

Bit	Description
7	Parity/-ECC, connector B4
6	Parity/-ECC, connector B3
5	Parity/-ECC, connector B2
4	Parity/-ECC, connector B1
3	Parity/-ECC, connector A4
2	Parity/-ECC, connector A3
1	Parity/-ECC, connector A2
0	Parity/-ECC, connector A1

Figure 2-8. Error-Checking Information

Each bit indicates the type of error-checking method used by that memory module— data-parity or error-checking and correction (ECC). When the bit is set to 1, the module in the specified connector uses the data-parity method to check for errors. When the bit is set to 0, the module uses the ECC method.

System Board POS Registers 4 (Hex 0104)

This register is accessed when bit 7 of the System Board Enable/Setup register is set to 0. The register is used to specify the arbitration levels used by the primary serial port during transmit and receive operations in the DMA mode.

Bit	Description
7–4	Receive arbitration level
3–0	Transmit arbitration level

Figure 2-9. System Board POS Register 4 (Hex 0104)

Bits 7–4 These bits select the arbitration level used for the transfer of data that is being received through the primary serial port.

Bits 3–0 These bits select the arbitration level used for the transfer of data that is being transmitted through the primary serial port.

System Board POS Register 5 (Hex 0105)

This register is used to specify the arbitration level used by the parallel port and the I/O addresses used by the primary serial port.

Bit	Description
7	Reserved
6–4	Select primary serial address
3–0	Parallel port arbitration level

Figure 2-10. System Board POS Register 5 (Hex 0105)

Bit 7 This bit is reserved.

Note: This bit might be read as 0 but does not indicate any occurrence of channel check.

Bits 6–4 These bits are used to select the I/O addresses that are used by the primary serial port on the system board. The I/O addresses can be the compatible addresses or the extended address (see Serial Port Controller in the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* for more information on addressing).

Bits 6 5 4	Assignment	Address (Hex)	
		Compatible	Extended
0 0 0	Serial 1	03F8–03FF	83F8–83FF
0 0 1	Serial 2	02F8–02FF	82F8–82FF
0 1 0	Serial 3	3220–3227	B220–B227
0 1 1	Serial 4	3228–322F	B228–B22F
1 0 0	Serial 5	4220–4227	C220–C227
1 0 1	Serial 6	4228–422F	C228–C22F
1 1 0	Serial 7	5220–5227	D220–D227
1 1 1	Serial 8	5228–522F	D228–D22F

Figure 2-11. Primary Serial Port Address Select Bits

Bits 3–0 These bits select the arbitration level used by the parallel port controller.

Diskette Drive POS Register 4 (Hex 0104)

This register is accessed when bit 6 of the System Board Enable/Setup register is set to 0. The register is used to specify the arbitration level used by the diskette drive controller.

Bit	Description
7–4	Reserved
3–0	Diskette drive arbitration level

Figure 2-12. Diskette Drive POS Register 4 (Hex 0104)

Bits 7–4 These bits are reserved.

Bits 3–0 These bits select the arbitration level used by the diskette drive controller.

Adapter Enable/Setup Register (Hex 0096)

This read/write register selects the connector to be configured.

Bit	Description
7	Channel reset
6–4	Reserved (set to 0)
3	Enable card setup
2–0	Channel select 2–0

Figure 2-13. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6–4 These bits are reserved and must be set to 0.

Bit 3 When set to 1, this bit enables the '-card setup' signal selected by bits 2 through 0.

Bits 2–0 These bits are the address bits for the '-card setup' signal to the connectors and the second serial port. Connectors 1 through 4 are addressed as 0 through 3; the second serial port is addressed as 5. When bit 3 is set to 1, these bits select the connector or function for setup cycles.

Each channel connector has a unique '-card setup' signal (-CD SETUP) associated with it. This signal is used to select the adapters for setup cycles, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Note: -CD SETUP goes active only when an operation is performed in the I/O address range hex 0100 through 0107.

Second Serial Port POS Register 2 (Hex 0102)

While the second serial port is selected for setup cycles, this read/write register is used to control the second serial port interface.

Bit	Description
7–4	Reserved
3	Select second serial IRQ
2	Enable second serial
1	Reserved
0	Enable second serial

Figure 2-14. Second Serial Port POS Register 2 (Hex 0102)

Bits 7–4 These bits are reserved.

Bit 3 When this bit is set to 1, the second serial port uses IRQ4; when it is set to 0, the second serial port uses IRQ3.

Bit 2 When this bit and bit 0 are set to 1, the second serial port is enabled. When either bit is set to 0, the port is disabled.

Bit 1 This bit is reserved.

Bit 0 When this bit and bit 2 are set to 1, the second serial port is enabled. When either bit is set to 0, the port is disabled.

Second Serial Port POS Register 4 (Hex 0104)

While the second serial port is selected for setup cycles, this read/write register selects the arbitration level used.

Bit	Description
7–4	Receive arbitration level
3–0	Transmit arbitration level

Figure 2-15. Second Serial Port POS Register 4 (Hex 0104)

Bits 7–4 These bits select the arbitration level used in the transfer of data being received by the second serial port.

Bits 3–0 These bits select the arbitration level used in the transfer of data being transmitted by the second serial port.

Second Serial Port POS Register 5 (Hex 0105)

While the second serial port is selected for setup cycles, this read/write register selects the I/O address of the second serial port.

Bit	Description
7	Reserved
6-4	Select I/O address
3-0	Reserved

Figure 2-16. Second Serial Port POS Register 5 (Hex 0105)

Bit 7 This bit is reserved.

Note: This bit might be read as 0 but does not indicate any occurrence of channel check.

Bits 6–4 These bits are used to select the I/O addresses that are used by the second serial port on the system board. The I/O addresses can be the compatible addresses or the extended address.

Bits 6 5 4	Assignment	Address (Hex)	
		Compatible	Extended
0 0 0	Serial 1	03F8–03FF	83F8–83FF
0 0 1	Serial 2	02F8–02FF	82F8–82FF
0 1 0	Serial 3	3220–3227	B220–B227
0 1 1	Serial 4	3228–322F	B228–B22F
1 0 0	Serial 5	4220–4227	C220–C227
1 0 1	Serial 6	4228–422F	C228–C22F
1 1 0	Serial 7	5220–5227	D220–D227
1 1 1	Serial 8	5228–522F	D228–D22F

Figure 2-17. Second Serial Port Address Select Bits

Bits 3–0 These bits are reserved.

Notes:

Section 3. System Board

| Description 3-3
Micro Channel Implementation 3-3
| Central Arbiter 3-3
Arbitration Bus Priority Assignments 3-3
Central Arbiter Programming 3-4
Diskette Drive Connector 3-7
| System Board Memory Connectors 3-8
| Real-Time Clock/Complementary Metal-Oxide Semiconductor
| (RT/CMOS) RAM 3-10
RT/CMOS Address Register and NMI Mask (Hex 0070) 3-11
RT/CMOS Data Register (Hex 0071) 3-11
RT/CMOS RAM I/O Operations 3-12
Real-Time Clock Bytes (Hex 000–00D) 3-13
| CMOS RAM Configuration 3-17
Miscellaneous System Functions and Ports 3-21
Nonmaskable Interrupt 3-21
| System Control Port B (Hex 0061) 3-22
System Control Port A (Hex 0092) 3-23
Power-On Password 3-25
Selectable Boot Sequence 3-26
Hardware Compatibility 3-27
| Error Codes 3-28

© Copyright IBM Corp. 1990, 1992

Notes:

Description

This section describes channel differences and various system ports and connectors for the Model 90 XP 486. For additional information about these and other topics, refer to the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces.*

Micro Channel Implementation

This section describes the implementation of the Micro Channel architecture on Model 90 XP 486 systems. For general Micro Channel information, refer to *IBM Personal System/2 Hardware Interface Technical Reference—Architectures.*

Note: The system does not support adapters that use the matched memory extension.

Central Arbiter

The central arbitration control point gives intelligent subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. This arbiter supports up to 16 arbitrating devices.

Arbitration Bus Priority Assignments

The following figure shows the assignment of arbitration levels. The functions with the lowest arbitration level have the highest priority.

ARB Level	Primary Assignment
-2	Memory refresh
-1	NMI
0	DMA channel 0 (programmable to any arbitration level)
1	DMA channel 1
2	DMA channel 2
3	DMA channel 3
4	DMA channel 4 (programmable to any arbitration level)
5	DMA channel 5
6	DMA channel 6
7	DMA channel 7
8–B	Available
C	SCSI adapter
D, E	Available
F	System microprocessor

Figure 3-1. Arbitration Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation, and by the previous controlling master. To prevent overrun, the diskette drive controller should not be held inactive for more than 12 microseconds.

Nonmaskable interrupt (NMI) service is executed at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal is in the arbitrate state.

When the central arbitration control point receives a level -1 request (NMI, a system board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level -1 request, and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following figures.

Bit	Definition
7	Enable system microprocessor cycle
6	Arbitration mask
5	Enable extended arbitration
4–0	Reserved

Figure 3-2. Arbitration Register (Hex 0090)—Write

Bit	Definition
7	Enable system microprocessor cycle
6	Arbitration masked by NMI
5	Bus time-out
4	Reserved
3–0	Value of arbitration bus during previous grant state

Figure 3-3. Arbitration Register (Hex 0090)—Read

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 1 by POST.

Reading this bit as a 1 indicates system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 enables extended arbitration. The minimum arbitration cycle is 300 nanoseconds; this bit extends that minimum cycle to 600 nanoseconds. This bit is set to 0 by POST.

Reading this bit as a 1 indicates that a bus time-out has occurred and resets bit 6 in this register to 0.

Bit 4 This bit is reserved and must be 0.

Bits 3–0 These bits are undefined for a write operation and should be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Diskette Drive Connector

The system provides three 2-by-17-pin connectors for attaching internal diskette drives. Each connector passes control and data signals between the diskette drive controller on the system board and the drives, and provides the power to each drive.

The following figure shows the signal assignments and pin numbers for the diskette drive connectors.

Pin	Signal	Pin	Signal
1	Ground	2	Data rate select 1
3	+5 V dc	4	Drive type ID 1
5	Ground	6	+12 V dc
7	Ground	8	-Index
9	Drive type ID 0	10	Reserved
11	Ground	12	-Drive select
13	Ground	14	Reserved
15	Ground	16	-Motor enable
17	Media type ID 1	18	-Direction in
19	Ground	20	-Step
21	Ground	22	-Write data
23	Ground	24	-Write enable
25	Ground	26	-Track 0
27	Media type ID 0	28	-Write protect
29	Ground	30	-Read data
31	Ground	32	-Head 1 select
33	Data rate select 0	34	-Diskette change

Figure 3-4. Diskette Drive Connector

System Board Memory Connectors

The Model 90 XP 486 system board has two connectors for riser cards. Each riser card provides four 72-pin memory connectors that support a variety of single inline memory modules (also called *memory modules*).

The following figure shows the location of the riser cards and memory connectors as viewed from the front of the system. The individual connectors are logically identified as A1 through A4 and B1 through B4; on both riser cards, these connectors are physically identified as J1 through J4, as shown in parentheses.

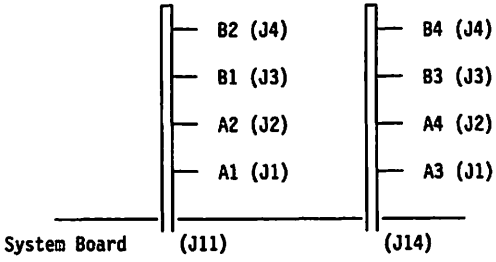


Figure 3-5. Memory Connector Numbering

Note: Riser 1 should be fully populated before putting memory in riser 2.

The following figure shows the pin assignments for the 1- by 72-pin memory connectors. Refer to "Type 1 Processor Complexes—Memory Presence Detect" on page 4-16, "Type 2 Processor Complexes—Memory Presence Detect" on page 5-11, and "Type 3 Processor Complexes—Memory Presence Detect" on page 6-9 for decoding of the presence-detect signals.

Pin	Signal	Pin	Signal
1	Ground	37	Parity data 1/ECC check bit 1
2	Data 0	38	Parity data 3/ECC check bit 3
3	Data 16	39	Ground
4	Data 1	40	Column address strobe 0
5	Data 17	41	Column address strobe 2
6	Data 2	42	Column address strobe 3
7	Data 18	43	Column address strobe 1
8	Data 3	44	Row address strobe 0
9	Data 19	45	Row address strobe 1
10	+5 V dc	46	Block select 1/ECC check bit 5
11	-Column address strobe P	47	Write enable
12	Address 0	48	+Parity/-ECC
13	Address 1	49	Data 8
14	Address 2	50	Data 24
15	Address 3	51	Data 9
16	Address 4	52	Data 25
17	Address 5	53	Data 10
18	Address 6	54	Data 26
19	Reserved	55	Data 11
20	Data 4	56	Data 27
21	Data 20	57	Data 12
22	Data 5	58	Data 28
23	Data 21	59	+5 V dc
24	Data 6	60	Data 29
25	Data 22	61	Data 13
26	Data 7	62	Data 30
27	Data 23	63	Data 14
28	Address 7	64	Data 31
29	Block select 0/ECC check bit 4	65	Data 15
30	+5 V dc	66	Block select 2/ECC check bit 6
31	Address 8	67	Presence detect 0
32	Address 9	68	Presence detect 1
33	Row address strobe 3	69	Presence detect 2
34	Row address strobe 2	70	Presence detect 3
35	Parity data 2/ECC check bit 2	71	Block select 3
36	Parity data 0/ECC check bit 0	72	Ground

Figure 3-6. System Board Memory Connector

Real-Time Clock/Complementary Metal-Oxide Semiconductor (RT/CMOS) RAM

The real-time clock/complementary metal-oxide semiconductor (RT/CMOS) RAM module contains the real-time clock and 64 bytes of CMOS RAM. The internal clock circuitry uses 14 bytes of this memory, and the rest is allocated for configuration and system-status information.

In addition to the 64 bytes of CMOS RAM, an 8KB CMOS RAM extension is provided for configuration and other system information.

A battery maintains voltage to the RT/CMOS RAM and 8KB CMOS RAM extension when the power supply is not in operation.

The system cover can be locked to prevent battery removal and, consequently, prevents the loss of password and configuration information.

The following figure shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000–00D	Real-time clock bytes
00E	Diagnostic Status byte
00F	Shutdown Status byte
010	Diskette Drive Type byte
011	Reserved
012	Reserved
013	Reserved
014	Equipment byte
015, 016	Low and High Base-Memory bytes
017, 018	Low and High Expansion-Memory bytes
019–031	Reserved
032, 033	Configuration CRC bytes
034	Reserved
035, 036	Low and high usable memory above 1MB to 16MB
037	Date-Century byte
038–3F	Reserved

Figure 3-7. RT/CMOS RAM Address Map

RT/CMOS Address Register and NMI Mask (Hex 0070)

This read/write register is used in conjunction with the RT/CMOS Data register (hex 0071) to read and write the RT/CMOS RAM bytes.

Bit	Function
7	NMI mask
6	Reserved
5–0	RT/CMOS RAM address

Figure 3-8. RT/CMOS Address Register and NMI Mask (Hex 0070)

Warning: The operation following a write operation to hex 0070 must access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Bit 7 When this bit is set to 1, the NMI is masked (the NMI is disabled). This bit is set to 1 by a power-on reset. This is a write-only bit.

Bit 6 This bit is reserved.

Bits 5–0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This port is used in conjunction with the RT/CMOS Address and NMI Mask register (hex 0070) to read and write the RT/CMOS RAM bytes.

Bit	Function
7–0	RT/CMOS data

Figure 3-9. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts must be masked to prevent other interrupt routines from changing the CMOS Address register before data is read from or written to.

Warning: The operation following a write operation to hex 0070 must access hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Writing to RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Write the data to address hex 0071.
3. Write the address hex 0F to the RT/CMOS and NMI Mask register; this leaves address hex 0070 pointing to the Shutdown Status byte (hex 0F).
4. Read from address hex 0071 to restore the RT/CMOS (see the warning above).

Reading from RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Read the data from address hex 0071.
3. Write the address hex 0F to the RT/CMOS and NMI Mask register; this leaves address hex 0070 pointing to the Shutdown Status byte (hex 0F).
4. Read from address hex 0071 to restore the RT/CMOS.

Real-Time Clock Bytes (Hex 000 – 00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following figure.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second alarm	1
002	Minutes	2
003	Minute alarm	3
004	Hours	4
005	Hour alarm	5
006	Day of week	6
007	Date of month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-10. Real-Time Clock Bytes (Hex 000 – 00D)

Note: The Setup program initializes Status Registers A and B when the time and date are set. Interrupt 1AH is the BIOS interface to read and set the time and date. It initializes the register in the same way that the Setup program does.

Status Register A (Hex 00A)

Bit	Function
7	Update in progress
6–4	22-stage divider
3–0	Rate-selection bits

Figure 3-11. Status Register A (Hex 00A)

Bit 7 When set to 1, this bit indicates the time-update cycle is in progress. When set to 0, it indicates the current date and time can be read.

Bits 6–4 These 3 divider-selection bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768-kHz time base. This is the only value supported by the system for proper timekeeping.

Bits 3–0 These bits allow the selection of a divider output frequency. The system initializes the rate-selection bits to a binary 0110, which selects a 1.024-kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Enable periodic interrupt
5	Enable alarm interrupt
4	Enable update-ended interrupt
3	Enable square wave
2	Date mode
1	24-hour mode
0	Enable daylight savings

Figure 3-12. Status Register B (Hex 00B)

Bit 7 When set to 0, this bit updates the cycle, normally by advancing the counts at a rate of one per second. When set to 1, this bit immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This bit is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

Bit 5 When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit indicates if the time-and-date calendar updates use binary or binary-coded-decimal (BCD) formats. When set to 1, this bit indicates a binary format. The system initializes this bit to 0.

Bit 1 This bit establishes if the hours byte is in the 24-hour or 12-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When set to 1, this bit enables the daylight savings time mode. When set to 0, it disables the mode, and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt-request flag
6	Periodic-interrupt flag
5	Alarm-interrupt flag
4	Update-ended interrupt flag
3–0	Reserved

Figure 3-13. Status Register C (Hex 00C)

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 This bit is used in conjunction with bits 6, 5, and 4. When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When set to 1, this bit indicates that a periodic interrupt occurred.

Bit 5 When set to 1, this bit indicates that an alarm interrupt occurred.

Bit 4 When set to 1, this bit indicates that an update-ended interrupt occurred.

Bits 3–0 These bits are reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6–0	Reserved

Figure 3-14. Status Register D (Hex 00D)

Bit 7 This read-only bit monitors the power-sense pin. A low state of this pin indicates a loss of power to the real-time clock (dead battery). When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power.

Bits 6–0 These bits are reserved.

CMOS RAM Configuration

The following figure shows the bit definitions for the CMOS RAM Configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-time clock module power
6	Configuration record and checksum status
5	Incorrect configuration
4	Memory size miscompare
3	Fixed disk controller/drive C initialization status
2	Time-status indicator
1	Adapter-configuration miscompare
0	Adapter-ID time-out

Figure 3-15. Diagnostic Status Byte (Hex 00E)

Bit 7 When set to 1, this bit indicates the real-time clock lost power.

Bit 6 When this bit is set to 1, the checksum is incorrect.

Bit 5 This is a check, at power-on, of the Equipment byte. When set to 1, the configuration information is incorrect. Power-on checks require that at least one diskette drive be installed (bit 0 of the Equipment byte, hex 014, is set to 1).

Bit 4 When set to 1, this bit indicates the power-on check determined that the memory size is not the same as in the configuration record.

Bit 3 When set to 1, this bit indicates that the controller or drive C failed initialization, which prevents the system from attempting a power-on reset.

Bit 2 When set to 0, this bit indicates the time is valid. When set to 1, this bit indicates the time is invalid.

Bit 1 This bit indicates if the installed adapters match the configuration information. When this bit is set to 1, the adapters do not match the configuration information.

Bit 0 When set to 1, this bit indicates a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette installed.

Bit	Function
7–4	First diskette drive type
3–0	Second diskette drive type

Figure 3-16. Diskette Drive Type Byte (Hex 010)

Bits 7–4 These bits indicate the first diskette drive type, as shown in the following figure.

Bits 7 6 5 4	Function
0 0 0 0	No drive present
0 0 0 1	5.25-inch, 360KB diskette drive
0 0 1 0	5.25-inch, 1.2MB diskette drive
0 0 1 1	3.5-inch, 720KB diskette drive
0 1 0 0	3.5-inch, 1.44MB diskette drive
0 1 1 0	3.5-inch, 2.88MB diskette drive

Note: Combinations that are not shown are reserved.

Figure 3-17. First Diskette Drive Type Byte (Bits 7–4)

Bits 3–0 These bits indicate the second diskette drive type, as shown in the following figure.

Bits 3 2 1 0	Function
0 0 0 0	No drive present
0 0 0 1	5.25-inch, 360KB diskette drive
0 0 1 0	5.25-inch, 1.2MB diskette drive
0 0 1 1	3.5-inch, 720KB diskette drive
0 1 0 0	3.5-inch, 1.44MB diskette drive
0 1 1 0	3.5-inch, 2.88MB diskette drive

Note: Combinations that are not shown are reserved.

Figure 3-18. Second Diskette Drive Type Byte (Bits 3–0)

Reserved Byte (Hex 011): This byte is reserved.

Reserved Byte (Hex 012): This byte is reserved.

Reserved Byte (Hex 013): This byte is reserved.

Equipment Byte (Hex 014): The Equipment byte, for the power-on diagnostic tests, defines the basic equipment in the system.

Bit	Function
7, 6	Number of diskette drives
5, 4	Display operating mode
3, 2	Reserved
1	Math coprocessor presence
0	Diskette drive presence

Figure 3-19. Equipment Byte (Hex 014)

Bits 7, 6 These bits indicate the number of diskette drives installed, as shown in the following figure.

Bits 7 6	Number of Diskette Drives
0 0	One drive
0 1	Two drives
1 0	Three drives
1 1	Reserved

Figure 3-20. Equipment Byte (Bits 7, 6)

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port, as shown in the following figure.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-column mode
1 0	80-column mode
1 1	Monochrome mode

Figure 3-21. Equipment Byte (Bits 5, 4)

Bits 3, 2 These bits are reserved.

Bit 1 When set to 1, this bit indicates that a math coprocessor is installed.

Bit 0 When set to 1, this bit indicates that a diskette drive is installed.

Low and High Base-Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 indicates 640KB. The low byte is hex 015; the high byte is hex 016.

Low and High Expansion-Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The value from these bytes represents the number of 1KB blocks of expansion memory. For example, hex 0800 indicates 2048KB. The low byte is hex 017; the high byte is hex 018.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check (CRC) data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 033; the high byte is hex 032.

Reserved Byte (Hex 034): This byte is reserved.

Low and High Usable Memory Bytes (Hex 035 and 036): These bytes define the total amount of contiguous usable memory from 1MB to 16MB.

The hexadecimal values in these bytes represent the number of 1KB blocks of usable memory. For example, hex 0800 indicates 2048KB. The low byte is hex 035; the high byte is hex 036.

Date-Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 through 03F): These bytes are reserved.

Miscellaneous System Functions and Ports

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system watchdog time-out has occurred. The NMI stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts and the IRET instruction restores the interrupt flag to the state it was in before the interrupt. A system reset causes a reset of the NMI.

The NMI requests that are caused by channel checks and system board memory-parity errors are subject to mask control with the NMI mask bit in the RT/CMOS Address register. The Watchdog Timer and system channel time-out are not masked by this bit. (See "RT/CMOS Address Register and NMI Mask (Hex 0070)" on page 3-11). The power-on default of the NMI mask is 1 (NMI disabled). Prior to enabling the NMI after a power-on reset, the parity-check and channel-check state are initialized by the POST.

Warning: The operation following a write operation to hex 0070 must access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the read and write functions of this port are shown in the following figures.

Bit	Function
7	Reset timer 0 output latch (IRQ0)
6–4	Reserved
3	Enable channel check
2	Enable parity check
1	Enable speaker data
0	Timer 2 gate to speaker

Figure 3-22. System Control Port B (Hex 0061)—Write

Bit	Function
7	Memory parity check
6	Channel check
5	Timer 2 output
4	Toggles with each refresh request
3	Enable channel check
2	Enable parity check
1	Enable speaker data
0	Timer 2 gate to speaker

Figure 3-23. System Control Port B (Hex 0061)—Read

Bit 7 Setting this bit to 1 resets IRQ0. Reading this bit as a 1 indicates a memory parity check has occurred.

Bit 6 Reading this bit as a 1 indicates a channel check has occurred.

Bit 5 This bit indicates the condition of the timer/counter 2 'output' signal.

Bit 4 This bit toggles for each refresh request.

Bit 3 Setting this bit to 0 enables channel check. Setting this bit to 1 disables channel check and clears the channel-check latch.

Bit 2 Setting this bit to 0 enables system board memory parity check. This bit is set to 1 during a power-on reset. To clear the indication of a parity error, set this bit to 1 and then to 0.

Note: This does not clear the source of a parity error.

Bit 1 Setting this bit to 1 enables speaker data.

Bit 0 Setting this bit to 1 enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7, 6	Fixed disk activity light
5	Reserved
4	Watchdog timer status
3	Security lock latch
2	Reserved (set to 0)
1	Alternate gate A20
0	Alternate hot reset

Figure 3-24. System Control Port A (Hex 0092)

Bits 7, 6 These bits control the fixed disk activity light. Setting either bit to 1 turns the fixed disk activity light on. Setting both bits to 0 turns the light off. The power-on reset condition of each bit is 0.

Bit 5 This bit is reserved.

Bit 4 This read-only bit indicates the watchdog-timer status. When this bit is set to 1, a watchdog time-out has occurred. For more information about the watchdog timer, refer to System Timers in *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces*.

Bit 3 This bit provides the security lock for the secured area of RT/CMOS. Setting this bit to 1 electronically locks the 8-byte, power-on password. Once this bit is set by POST, it can only be cleared by turning the system off.

Bit 2 This bit is reserved.

Bit 1 This bit is ORed with bit 1 in the Keyboard Output port to enable the 'address 20' signal (A20). When both bits are set to 0, A20 is disabled and set to 0. This bit is set to 0 during POST. (See the Keyboard and Auxiliary Device Controller section in the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces*.)

Bit 0 This bit provides an alternate method of resetting the system microprocessor. This alternate method supports operating systems requiring faster operation than was provided on the IBM Personal Computer AT*. Resetting the system microprocessor is used to switch the microprocessor from the protected mode to the real address mode. The alternate reset takes 13.4 microseconds.

This bit is set to 0 either by a system reset or a write operation. When a write operation changes this bit from 0 to 1, the alternate reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is 0, POST assumes the system was just powered on. If the bit is 1, POST assumes a switch from the protected mode to the real mode has taken place.

* Trademark of the IBM Corporation.

Power-On Password

RT/CMOS RAM has 8 bytes reserved for the power-on password and its check character. The 8 bytes are initialized to hex 00. The microprocessor can only access these bytes during power-on self-test (POST). After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by any program. A power-on password can be from 1 to 7 characters.

During power-on password installation, the password (1 to 7 keyboard scan codes) is stored in the security space.

Power-on password installation is a function of a program contained on the Reference Diskette. Once the power-on password has been installed, the password can be changed only during the POST. If a power-on password is changed, or removed during POST, the password is not visible on the display.

The system-unit cover can be physically locked to prevent unauthorized access to the battery. This helps prevent unauthorized battery removal and loss of power-on password and configuration information.

For information about the keyboard password, see the Keyboard and Auxiliary Device Controller section in the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces.*

Selectable Boot Sequence

With selectable boot you can specify the order in which bootable devices are searched when looking for the boot startup record of an operating system. Diskette drives, fixed disk drives, and remote initial program load (RIPL) can be part of the search sequence. Changing the sequence for selectable boot affects the drive-letter assignment each time the system is booted (started).

You can select the boot sequence by using the Select startup sequence menu on the Reference Diskette, and selecting from a list of possible devices. After the sequence is selected, it is stored in nonvolatile RAM (NVRAM). When the system is booted, it searches for a device that contains a bootable record, using the specified sequence.

After the operating system is booted, the drive lettering is determined by the sequence and by which device contained the bootable source.

Note: Selectable boot affects adapters that use initialization programs. See the Setup section in the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures* for more details.

Hardware Compatibility

The Model 90 XP 486 maintains many of the interfaces used by previous IBM PS/2 products. In most cases command and status organization of these interfaces is maintained.

The functional interfaces for the Model 90 XP 486 are compatible with the following interfaces:

- The Intel** 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller address/transfer counters, page registers, and status fields only. The Command and Request registers are not supported. The rotate and mask functions are not supported. The Mode register is partially supported.
- The NS16450 serial port.
- The Intel 8088, 8086, 80286, and 80386 microprocessors.
- The Intel 8272 diskette drive controller.
- The Motorola** MC146818A Time of Day Clock command and status (CMOS reorganized).
- The keyboard interface at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.

** Intel is a trademark of Intel Corporation, and Motorola is a trademark of Motorola, Incorporated.

Error Codes

POST returns a message in the form of a multiple-character code to indicate the type of test that failed. Two formats are used for these error messages:

- A 12-character code for all errors related to SCSI devices:
  - The first four characters identify the device type.
  - The next eight characters identify specifics of the error.
- An 8-character error code for all errors not related to SCSI devices.

The 8-character error code consists of two 4-character elements: the major error code and the minor error code. The following figure gives the failure indicated with the associated error code.

Major Code	Minor Code	Description
0001		System bus error - system board or processor complex
	0100	Unexpected interrupt
	0200	Timer failure
	0300	Timer interrupt failure
	0400	Protected mode failure
	0500	Last keyboard command not accepted
	0600	Converting logic test
	0700	NMI test failed
	0800	Timer bus-test failed
	0900	Low-MB chip-select test failed
	10xx	System board memory parity error
	11xx	I/O channel check error
	1200	Watchdog timeout
	1300	Micro Channel bus timeout
	1400	Channel feature card ROM checksum error
	1500	ROM checksum error or DMA error
	1600	System board port read/write failure
	1800	System board parity or L2-cache error during previous power-on
	1900	Down-level diskette controller (2.88MB diskette drive not supported)
	2000	Microprocessor test error
	6000	System board ID not recognized
	6100	Dead battery
	6300	Clock not updating
	6400	Memory configuration error
	6500	Adapter ID mismatch
	6600	Adapter busy error
	6700	Clock not updating
	6900	Processor complex configuration error
	7000	ASCII setup conflict error
	7100	Rolling bit test failure on CMOS Shutdown Address byte
	7200	Rolling bit test failure on NVRAM Diagnostic byte
	7300	Bad CMOS/NVRAM checksum
	7400	Bad configuration
	7900	NVRAM error log full
0002		Memory errors
	0xxx	Memory error
	1xxx	Unrecoverable error in first 1MB
	2100	ROM to RAM remapping error
	25xx	Unsupported memory-type installed or memory mismatch
	3500	Stuck data line on memory module, processor complex, or system board

Figure 3-25 (Part 1 of 2). POST Error Messages

Major Code	Minor Code	Description
0003		Keyboard
	0100	Keyboard error
	0200	Keyboard locked
	0300	Keyboard to system board interface error
	0400	Keyboard clock high
	0500	No keyboard +5 V
0006		Diskette
	0100	Diskette drive or controller error
	0200	Diskette IPL boot record not valid
	0400	Nonmedia sense
0011	0100	Async chip error
0017		Fixed disk error
	8000	Fixed disk 0 failed
	8100	Fixed disk 1 failed
	8200	Disk controller error
	9000	Fixed disk 0 error
	9100	Fixed disk 1 error
0024	0100	System board video error
0086		Mouse
	0100	System bus error - keyboard/pointing device interface
	0200	Pointing device error
	0300	Pointing device or system bus error
0096	*xxxx*	SCSI adapter (with cache) failure
0112	*xxxx*	SCSI adapter (without cache) failure
0129		Processor complex
	005*x*	DMA error
	0x00	Cache error
	12*xx*	Hardware failure
	13*xx*	Micro Channel bus timeout
	14*xx*	Software failure
	15*xx*	Processor complex error
	16*xx*	Processor complex error
	17*xx*	Processor complex error
	18*xx*	Processor complex error
	19*xx*	Processor complex error
	40*xx*	Processor complex failure
	50*xx*	Processor complex failure
	9000	Processor complex serial-number mismatch
0208 to 0241	*xxxx*	SCSI device test failure
1999		Special instruction codes
	00*xx*	Initial microcode load (IML) error
	03*xx*	No bootable device
	04*xx*	IML to system mismatch
	06*xx*	IML error

Figure 3-25 (Part 2 of 2). POST Error Messages

Section 4. Type 1 Processor Complexes

| Description 4-3
| Type 1A 4-4
| Type 1B 4-7
| Type 1C 4-10
| Type 1D 4-13
Type 1 Processor Complexes—I/O Address Map 4-15
| Type 1 Processor Complexes—Level 2 Cache 4-15
Type 1 Processor Complexes—Memory Subsystem 4-15
| Type 1 Processor Complexes—Memory Presence Detect . . . 4-16
| Type 1 Processor Complexes—Cache Address Map 4-17
Type 1 Processor Complexes—Read-Only Memory Subsystem 4-19

© Copyright IBM Corp. 1990, 1992

Notes:

Description

The processor complex provides certain devices and features that work in conjunction with devices and features provided by the system board. In addition, the processor complex determines system performance and certain channel timings. This section describes those aspects of the processor complex.

Type 1 has four different processor complexes. The major difference between each processor complex is speed. Programs can identify the processor complex by reading the model and submodel bytes. Interrupt 15H, Return System Configuration Parameters function ((AH)=C0H), returns the model byte, submodel byte, BIOS revision code, and other configuration information. The following figure shows the model bytes, submodel bytes, and speed of the processor complexes.

Model Byte	Submodel Byte	Speed	Processor Complex
F8	11	25 MHz	Type 1A
F8	13	33 MHz	Type 1B
F8	2D	20 MHz	Type 1C (see note)
F8	2F	20 MHz	Type 1C with 487 SX math coprocessor (see note)
F8	2B	50 MHz	Type 1D

Note: The type 1C processor complex features the Intel486** SX microprocessor and supports the Intel487** SX math coprocessor. When the 487 SX math coprocessor is used, a jumper must be moved to adjust for pinout differences. See "Type 1C Jumper" on page 4-10 for jumper information.

Figure 4-1. Type 1 Processor Complexes—Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems.

** Intel486 and Intel487 are trademarks of Intel Corporation.

Type 1A

The following figure shows the devices and features for the type 1A processor complex.

Device	Type	Features
Microprocessor	—	80486DX—25 MHz, 32-bit address and 32-bit data interface
Cache	—	8KB, 4-way, write-through, internal cache, optional 256KB L2 cache interface
ROM Subsystem	—	128KB physical ROM
RAM Subsystem	—	Eight-connector support, 2MB to 64MB interleaved, parity expandable on the system board only
DMA Controller	1	Eight independent DMA channels, single or burst transfers and read verification
Math Coprocessor	—	Math coprocessor functions included in 80486DX

Figure 4-2. Type 1A Processor Complex—Features and Devices

The following figure shows the performance and other timing information for the type 1A processor complex. These timings affect the channel performance for operations involving the processor complex or system board memory.

Note: All of the timings in Figure 4-3 and in Figure 4-4 on page 4-6 are typical values. Timings can vary depending on microprocessor workload, bus master workload, and cycle mix.

Device	Cycle Time (ns)
Microprocessor (25 MHz—40 ns Clock)	
Access to channel	
Default transfer cycle	240
Extended transfer cycle	320
Refresh Rate	
(Typically performed every 15.1 μs)	500 (min)
DMA Controller (10 MHz—100 ns Clock)	
Single transfer: 300 + I/O access + memory access	
Burst transfers: 300 + (I/O access + memory access)*n*†	
System board memory access	300
Default transfer cycle	200
Synchronous extended transfer cycle	300
† *n* is the number of transfers in the burst transfer.	

Figure 4-3. Type 1A Processor Complex—System Performance Specifications

Device	Cycle Time (ns) per Memory Type		
	70 ns	80 ns	85 ns
Microprocessor (25 MHz—40 ns Clock)			
Memory read (cache hit)	40	40	40
Memory read (cache miss, page hit, burst)	320	320	400
Memory read (cache miss, page miss, burst)	440	480	560
Memory write (page hit)	160	160	200
Memory write (page miss)	280	320	360
Microprocessor—with Optional L2 Cache			
Memory read (cache hit, optional cache hit)	40	40	40
Memory read (cache miss, optional cache hit, burst)	200	200	200
Memory read (cache miss, optional cache miss, page hit, burst)	320	320	400
Memory read (cache miss, optional cache miss, page miss, burst)	440	480	560
Memory write (page hit)	160	160	200
Memory write (page miss)	280	320	360
Bus Master Access to System Board RAM			
Page hit (typical†)	440	440	440
Page miss (typical†)	580	580	580

† Variations exist because of differences in timings of masters and system master accesses to system board memory that are interleaved with master accesses.

Figure 4-4. Type 1A Processor Complex—Memory Performance Specifications,

Type 1B

The following figure shows the devices and features for the type 1B processor complex.

Device	Type	Features
Microprocessor	—	80486DX—33 MHz, 32-bit address and 32-bit data interface
Cache	—	8KB, 4-way, write-through, internal cache, optional 256KB L2 cache interface
ROM Subsystem	—	128KB physical ROM
RAM Subsystem	—	Eight-connector support, 2MB to 64MB interleaved, parity expandable on the system board only
DMA Controller	1	Eight independent DMA channels, single or burst transfers and read verification
Math Coprocessor	—	Math coprocessor functions included in 80486DX

Figure 4-5. Type 1B Processor Complex—Features and Devices

The following figure shows the performance and other timing information for the type 1B processor complex. These timings affect the channel performance for operations involving the processor complex or system board memory.

Note: All of the timings in Figure 4-6 and in Figure 4-7 on page 4-9 are typical values. Timings can vary depending on microprocessor workload, bus master workload, and cycle mix.

Device	Cycle Time (ns)
Microprocessor (33 MHz—30 ns Clock)	
Access to channel	
Default transfer cycle	240
Extended transfer cycle	320
Refresh Rate	
(Typically performed every 15.1 μs)	500 (min)
DMA Controller (10 MHz—100 ns Clock)	
Single transfer: 300 + I/O access + memory access	
Burst transfers: 300 + (I/O access + memory access)*n*†	
System board memory access	300
Default transfer cycle	200
Synchronous extended transfer cycle	300
† *n* is the number of transfers in the burst transfer.	

Figure 4-6. Type 1B Processor Complex—System Performance Specifications

Device	Cycle Time (ns) per Memory Type		
	70 ns	80 ns	85 ns
Microprocessor (33 MHz—30 ns Clock)			
Memory read (cache hit)	30	30	30
Memory read (cache miss, page hit, burst)	240	300	300
Memory read (cache Miss, page miss, burst)	360	420	420
Memory write (page hit)	120	150	150
Memory write (page miss)	240	270	270
Microprocessor—with Optional L2 Cache			
Memory read (cache hit, optional cache hit)	30	30	30
Memory read (cache miss, optional cache hit, burst)	150	150	150
Memory read (cache miss, optional cache miss, page hit, burst)	240	300	300
Memory read (cache miss, optional cache miss, page miss, burst)	360	420	420
Memory write (page hit)	120	150	150
Memory write (page miss)	240	270	270
Bus Master Access to System Board RAM			
Page hit (typical†)	400	400	400
Page miss (typical†)	550	550	550

† Variations exist because of differences in timings of masters and system master accesses to system board memory that are interleaved with master accesses.

Figure 4-7. Type 1B Processor Complex—Memory Performance Specifications

Type 1C

The following figure shows the devices and features for the type 1C processor complex.

Device	Type	Features
Microprocessor	—	80486SX—20 MHz, 32-bit address and 32-bit data interface
Cache	—	8KB, 4-way, write-through, internal cache only
ROM Subsystem	—	128KB physical ROM
RAM Subsystem	—	Eight-connector support, 2MB to 64MB interleaved, parity expandable on the system board only
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Math Coprocessor	—	Optional using the 487 SX math coprocessor

Figure 4-8. Type 1C Processor Complex—Features and Devices

Type 1C Jumper: A jumper is moved to adjust for the pinout differences between the 486 SX microprocessor and the 487 SX math coprocessor. The jumper is located next to the microprocessor socket. For the 486 SX microprocessor, the jumper is connected across pins 2 and 3. For the 487 SX math coprocessor, the jumper is connected across pins 1 and 2.

The following figure shows the performance and other timing information for the type 1C processor complex. These timings affect the channel performance for operations involving the processor complex or system board memory.

Note: All of the timings in Figure 4-9 and in Figure 4-10 on page 4-12 are typical values. Timings can vary depending on microprocessor workload, bus master workload, and cycle mix.

Device	Cycle Time (ns)
Microprocessor (20 MHz—50 ns Clock)	
Access to channel	
Default transfer cycle	250
Extended transfer cycle	350
Refresh Rate	
(Typically performed every 15.1 μs)	600 (min)
DMA Controller (10 MHz—100 ns Clock)	
Single transfer: 300 + I/O access + memory access	
Burst transfers: 300 + (I/O access + memory access)*n*†	
System board memory access	400
Default transfer cycle	200
Synchronous extended transfer cycle	300

† *n* is the number of transfers in the burst transfer.

Figure 4-9. Type 1C Processor Complex—System Performance Specifications

Device	Cycle Time (ns) per Memory Type		
	70 ns	80 ns	85 ns
Microprocessor (20 MHz—50 ns Clock):			
Memory read (cache hit)	50	50	50
Memory read (cache miss, page hit, burst)	350	350	350
Memory read (cache miss, page miss, burst)	500	500	500
Memory write (page hit)	150	150	150
Memory write (page miss)	300	300	300
Bus Master Access to System Board RAM			
Page hit (typical†)	350	350	350
Page miss (typical†)	500	500	500

† Variations exist because of differences in timings of masters and system master accesses to system board memory that are interleaved with master accesses.

Figure 4-10. Type 1C Processor Complex—Memory Performance Specifications

Type 1D

The following figure shows the devices and features for the type 1D processor complex.

Device	Type	Features
Microprocessor	—	80486DX—50 MHz, 32-bit address and 32-bit data interface
Cache	—	8KB, 4-way, write-through, internal cache, 256KB L2 cache
ROM Subsystem	—	128KB physical ROM
RAM Subsystem	—	Eight-connector support, 2MB to 64MB interleaved, parity expandable on the system board only
DMA Controller	1	Eight independent DMA channels, single or burst transfers and read verification
Math Coprocessor	—	Math coprocessor functions included in 80486DX

Figure 4-11. Type 1D Processor Complex—Features and Devices

The following figure shows the performance and other timing information for the type 1D processor complex. These timings affect the channel performance for operations involving the processor complex or system board memory.

Note: All of the timings in Figure 4-12 on page 4-14 and in Figure 4-13 on page 4-14 are typical values. Timings can vary depending on microprocessor workload, bus master workload, and cycle mix.

Device	Cycle Time (ns)
Microprocessor (50 MHz—20 ns Clock)	
Access to channel	
Default transfer cycle	240
Extended transfer cycle	320
Refresh Rate	
(Typically performed every 15.1 μs)	500 (min)
DMA Controller (10 MHz—100 ns Clock)	
Single transfer: 300 + I/O access + memory access	
Burst transfers: 300 + (I/O access + memory access)*n*†	
System board memory access	300
Default transfer cycle	200
Synchronous extended transfer cycle	300

† *n* is the number of transfers in the burst transfer.

Figure 4-12. Type 1D Processor Complex—System Performance Specifications

Device	Cycle Time (ns) per Memory Type		
	70 ns	80 ns	85 ns
Microprocessor (50 MHz—20 ns Clock with L2 Cache)			
Memory read (cache hit, L2 cache hit)	20	20	20
Memory read (cache miss, L2 cache hit, burst)	100	100	100
Memory read (cache miss, L2 cache miss, page hit, burst)	360	360	440
Memory read (cache miss, L2 cache miss, page miss, burst)	480	520	600
Memory write (page hit)	200	200	240
Memory write (page miss)	320	360	400
Bus Master Access to System Board RAM			
Page hit (typical†)	300	300	300
Page miss (typical†)	300	300	300

† Variations exist because of differences in timings of masters and system master accesses to system board memory that are interleaved with master accesses.

Figure 4-13. Type 1D Processor Complex—Memory Performance Specifications

Type 1 Processor Complexes—I/O Address Map

The following shows the I/O address for devices located on the processor complex.

Hex Addresses	Device
0000–001F	DMA controller (0–3)
0081–0083, 0087	DMA Page registers (0–3)
0089–008B, 008F	DMA Page registers (4–7)
0090	Central arbitration control point
00C0–00DF	DMA controller (4–7)

Figure 4-14. Type 1 Processor Complexes—I/O Address Map

Type 1 Processor Complexes—Level 2 Cache

The type 1A and type 1B processor complexes have a 160-pin connector for an optional 256KB cache (L2 cache). The optional cache provides a secondary cache and cache controller for the system microprocessor. The type 1C processor complex does not support an optional cache. The type 1D processor complex has a standard 256KB L2 cache.

The L2 cache on type 1A, type 1B, and type 1D processor complexes provides the system microprocessor with an additional 256KB cache. It operates as a two-way, set-associative, write-through cache with parity. The primary cache in both the 80486DX and 80486DX2 must be enabled to operate the secondary cache.

Type 1 Processor Complexes—Memory Subsystem

Memory on the system board is parity-checked, interleaved, random-access memory and must be installed in matched pairs: one in an A connector and one in the matching B connector (for memory connector information, see "System Board Memory Connectors" on page 3-8). The memory in each pair must be the same speed and size. System memory on adapters in the channel is not mapped into the cacheable address space of the system microprocessor.

System board memory is designed so that the system microprocessor can access memory while a bus master has control of the channel.

The memory controller manages this dual access by interleaving the microprocessor and bus master accesses. In addition, system board memory is organized into pairs of banks so that the microprocessor can perform burst cycles with two-way interleaved accesses. Because of this organization, the microprocessor can perform zero-wait-state transfers for every other 32-bit transfer in the burst cycle.

Type 1 Processor Complexes—Memory Presence Detect

The presence-detect signals are used by the system to determine the size and speed of memory on the single inline memory module (also called *memory module*). The pins are either not connected (1) or connected to ground (0).

A set of 4 bits shows the state of all presence-detect signals for a specific memory connector; the bit is 0 when the signal is connected to ground. The following figure shows the information indicated by these bits, as well as the bank size of the memory module. Combinations that are not shown are reserved.

Presence Detect 3 2 1 0	Single Inline Memory Module Definition	Bank Size	Type
1 0 1 1	8MB 70-ns memory	4MB	Parity
1 0 0 0	8MB 80-ns memory	4MB	Parity
0 1 0 0	4MB 70-ns memory	4MB	Parity
0 0 0 0	4MB 80-ns memory	4MB	Parity
1 1 0 0	2MB 70-ns memory	1MB	Parity
1 0 0 1	2MB 80-ns memory	1MB	Parity
0 1 0 1	2MB 85-ns memory	1MB	Parity
0 1 1 0	1MB 85-ns memory	1MB	Parity
1 1 1 1	Connector is empty		

Figure 4-15. Type 1 Processor Complexes—Presence-Detect Bits

Type 1 Processor Complexes—Cache Address Map

The following map is a summary of those addresses within the memory address space that can be cached. Only system board memory is mapped into the microprocessor level 1 cache and level 2 cache. The level 2 (L2) cache is optional for type 1A and type 1B processor complexes. The type 1C processor complex does not support an optional cache. The type 1D processor complex has a standard 256KB L2 cache.

The system memory address space contains three cacheable regions:

- Region 1—Memory addresses from 0 up to 1MB
- Region 2—Memory addresses from 1MB up to 16MB
- Region 3—Memory addresses from 16MB up to 64MB.

All system board memory in region 2 and region 3 is cacheable. Programmable boundary registers for region 2 and region 3 control the upper boundaries of the memory space to be cached. The Set Configuration utility assigns memory to these cached regions, depending on the system configuration. POST establishes these cached regions, and they must not be altered.

Nonsystem memory can be located as follows:

- Region 1—In the area between memory addresses 0C0000 and 0DFFFF
- Region 2—Memory addresses from 16MB down to system memory
- Region 3—Memory addresses from 4GB (minus 1MB) down to system memory.

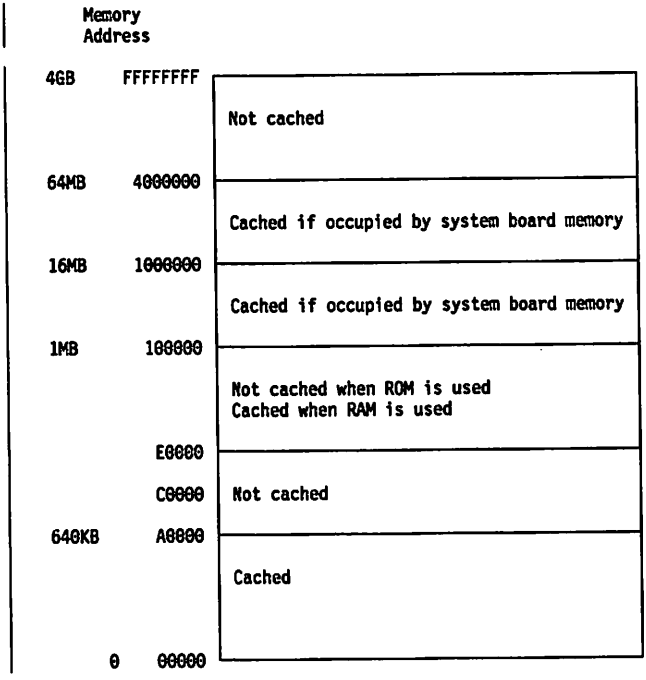


Figure 4-16. Type 1 Processor Complexes—Cache Address Map Summary

Type 1 Processor Complexes—Read-Only Memory Subsystem

The ROM subsystem is located on the processor complex and consists of 128KB in a 128K by 8-bit arrangement. The ROM is active at power-on at memory address space hex 000E0000 to 000FFFFF. The ROM contains the code that initializes the system to load and execute POST and BIOS code from a DASD device. ROM is also assigned at the top of the 4GB memory address space from hex FFFE0000 to FFFFFFFF.

Notes:

Section 5. Type 2 Processor Complexes

| Description 5-3
| Type 2A 5-4
| Type 2B 5-7
Type 2 Processor Complexes—I/O Address Map 5-10
| Type 2 Processor Complexes—Level 2 Cache 5-10
| Type 2 Processor Complexes—Memory Subsystem 5-10
| Type 2 Processor Complexes—Memory Presence Detect . . . 5-11
| Type 2 Processor Complexes—Cache Address Map 5-12
Type 2 Processor Complexes—Read-Only Memory Subsystem 5-14

© Copyright IBM Corp. 1990, 1992

Notes:

Description

The processor complex provides certain devices and features that work in conjunction with devices and features provided by the system board. In addition, the processor complex determines system performance and certain channel timings. This section describes those aspects of the processor complex.

Type 2 has two different processor complexes. The major difference between each processor complex is speed. Programs can identify the processor complex by reading the model and submodel bytes. Interrupt 15H, Return System Configuration Parameters function ((AH)=C0H), returns the model byte, submodel byte, BIOS revision code, and other configuration information. The following figure shows the model bytes, submodel bytes, and speed of the processor complexes.

Model Byte	Submodel Byte	Speed	Processor Complex
F8	57	25 MHz	Type 2A
F8	59	25 MHz	Type 2A with 487SX math coprocessor
F8	5B	50 MHz	Type 2A with 486DX2 module plugged on the type 2A processor complex†
F8	3F	50 MHz	Type 2B

† For performance information, see Figure 5-6 on page 5-8 and Figure 5-7 on page 5-9.

Figure 5-1. Type 2 Processor Complexes—Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems.

Type 2A

The following figure shows the devices and features for the type 2A processor complex.

Device	Type	Features
Microprocessor	—	80486SX—25 MHz, 32-bit address and 32-bit data interface
Cache	—	8KB, 4-way, write-through, internal cache
ROM Subsystem	—	128KB physical ROM
RAM Subsystem	—	Eight-connector support, 2MB to 64MB interleaved or noninterleaved, parity expandable on the system board only
DMA Controller	1	Eight independent DMA channels, single or burst transfers and read verification
Math Coprocessor	—	80487SX math coprocessor socket

Figure 5-2. Type 2A Processor Complex—Features and Devices

The following figure shows the performance and other timing information for the type 2A processor complex. These timings affect the channel performance for operations involving the processor complex or system board memory.

Device	Cycle Time (ns)
Microprocessor (25 MHz—40 ns Clock)	
Access to channel	
Default transfer cycle	320
Extended transfer cycle	440
Refresh Rate	
(Typically performed every 15.1 μs)	320 (min)
DMA Controller (25 MHz—40 ns Clock)	
Single transfer: 300 + I/O access + memory access	
Burst transfers: 300 + (I/O access + memory access)*n*†	
Memory access	
Page hit read	160
Page miss read	280
Page hit write	120
Page miss write	240
I/O access	
Default transfer cycle	320
Synchronous extended transfer cycle	440

† *n* is the number of transfers in the burst transfer.

Figure 5-3. Type 2A Processor Complex—System Performance Specifications

Device	Cycle Time (ns) per Memory Type		
	70 ns	80 ns	85 ns
Microprocessor (25 MHz—40 ns Clock)			
Memory read (cache hit)	40	40	NA
Memory read (cache miss, page hit, burst)	280	280	NA
Memory read (cache miss, page miss, burst)	400	400	NA
Memory write (page hit)	120	120	NA
Memory write (page miss)	240	240	NA
Bus Master Access to System Board RAM			
Always page miss (minimum)	300	300	NA

Note: NA means not applicable.

Figure 5-4. Type 2A Processor Complex—Memory Performance Specifications

Type 2B

The following figure shows the devices and features for the type 2B processor complex.

Device	Type	Features
Microprocessor	—	80486DX2—50 MHz, 32-bit address and 32-bit data interface
Cache	—	8KB, 4-way, write-through, internal cache
ROM Subsystem	—	128KB physical ROM
RAM Subsystem	—	Eight-connector support, 2MB to 64MB interleaved or noninterleaved, expandable on the system board only
DMA Controller	1	Eight independent DMA channels, single or burst transfers and read verification
Math Coprocessor	—	Math coprocessor functions included in 80486DX2

Figure 5-5. Type 2B Processor Complex—Features and Devices

The following figure shows the performance and other timing information for the type 2B processor complex. These timings affect the channel performance for operations involving the processor complex or system board memory.

Device	Cycle Time (ns)
Microprocessor (50 MHz—40 ns Clock)	
Access to channel	
Default transfer cycle	320
Extended transfer cycle	440
Refresh Rate	
(Typically performed every 15.1 μs)	320 (min)
DMA Controller (25 MHz—40 ns Clock)	
Single transfer: 300 + I/O access + memory access	
Burst transfers: 300 + (I/O access + memory access)*n*†	
Memory access	
Page hit read	160
Page miss read	280
Page hit write	120
Page miss write	240
I/O access	
Default transfer cycle	320
Synchronous extended transfer cycle	440

† *n* is the number of transfers in the burst transfer.

Figure 5-6. Type 2B Processor Complex—System Performance Specifications

Device	Cycle Time (ns) per Memory Type		
	70 ns	80 ns	85 ns
Microprocessor (50 MHz—40 ns Clock)			
Memory read (cache hit)	20	20	NA
Memory read (cache miss, page hit, burst)	280	280	NA
Memory read (cache miss, page miss, burst)	400	400	NA
Memory write (page hit)	120	120	NA
Memory write (page miss)	240	240	NA
Bus Master Access to System Board RAM			
Always page miss (minimum)	300	300	NA
Note: NA means not applicable.			

Figure 5-7. Type 2B Processor Complex—Memory Performance Specifications

Type 2 Processor Complexes—I/O Address Map

The following shows the I/O address for devices located on the processor complex.

Hex Addresses	Device
0000–001F	DMA controller (0–3)
0081–0083, 0087	DMA Page registers (0–3)
0089–008B, 008F	DMA Page registers (4–7)
0090	Central arbitration control point
00C0–00DF	DMA controller (4–7)

Figure 5-8. Type 2 Processor Complexes—I/O Address Map

Type 2 Processor Complexes—Level 2 Cache

The type 2A and type 2B processor complexes do not support a level 2 (L2) cache.

Type 2 Processor Complexes—Memory Subsystem

Memory on the system board is parity-checked, random-access memory that can be interleaved or noninterleaved. To operate in interleaved mode, the memory must be in both A connectors and B connectors (for memory connector information, see "System Board Memory Connectors" on page 3-8). The processor complex will automatically interleave memory between the A and B connectors (even and odd banks). If more memory is installed in either bank, then that difference will be used as noninterleaved memory. For example, if 2MB are installed in an A connector (even bank) and 4MB are installed in B connectors (odd bank), then the 2MB in the even bank will be interleaved with 2MB of the 4MB in the odd bank. The remaining 2MB in the odd bank will be noninterleaved. When operating in interleaved mode, the microprocessor can perform burst cycles with two-way interleaved accesses. This allows the microprocessor to perform zero-wait-state transfers for alternating 32-bit transfers in the burst cycle.

The type 2A and type 2B processor complexes do not support system microprocessor and bus master interleaving of system memory accesses.

Type 2 Processor Complexes—Memory Presence Detect

The presence-detect signals are used by the system to determine the size and speed of memory on the single inline memory module (also called *memory module*). The pins are either not connected (1) or connected to ground (0).

A set of 4 bits shows the state of all presence-detect signals for a specific memory connector; the bit is 0 when the signal is connected to ground. The following figure shows the information indicated by these bits, as well as the bank size of the memory module. Combinations that are not shown are reserved.

Presence Detect 3 2 1 0	Single Inline Memory Module Definition	Bank Size	Type
1 0 1 1	8MB 70-ns memory	4MB	Parity
1 0 0 0	8MB 80-ns memory	4MB	Parity
0 1 0 0	4MB 70-ns memory	4MB	Parity
0 0 0 0	4MB 80-ns memory	4MB	Parity
1 1 0 0	2MB 70-ns memory	1MB	Parity
1 0 0 1	2MB 80-ns memory	1MB	Parity
1 1 1 1	Connector is empty		

Figure 5-9. Type 2 Processor Complexes—Presence-Detect Bits

Type 2 Processor Complexes—Cache Address Map

The following map is a summary of those addresses within the memory address space that can be cached. Only system board memory is mapped into the microprocessor level 1 cache and level 2 cache. The type 2A and type 2B processor complexes do not support a level 2 cache.

The system memory address space contains three cacheable regions:

- Region 1—Memory addresses from 0 up to 1MB
- Region 2—Memory addresses from 1MB up to 16MB
- Region 3—Memory addresses from 16MB up to 64MB.

All system board memory in region 2 and region 3 is cacheable. Programmable boundary registers for region 2 and region 3 control the upper boundaries of the memory space to be cached. The Set Configuration utility assigns memory to these cached regions, depending on the system configuration. POST establishes these cached regions, and they must not be altered.

Nonsystem memory can be located as follows:

- Region 1—In the area between memory addresses 0C0000 and 0DFFFF
- Region 2—Memory addresses from 16MB down to system memory
- Region 3—Memory addresses from 4GB down to 2GB.

Note: If you have a type 2 processor complex, and have nonsystem memory located between 16MB and 2GB, the system will disable the processor cache during POST. If nonsystem memory is used in the 16MB to 2GB range, performance is reduced.

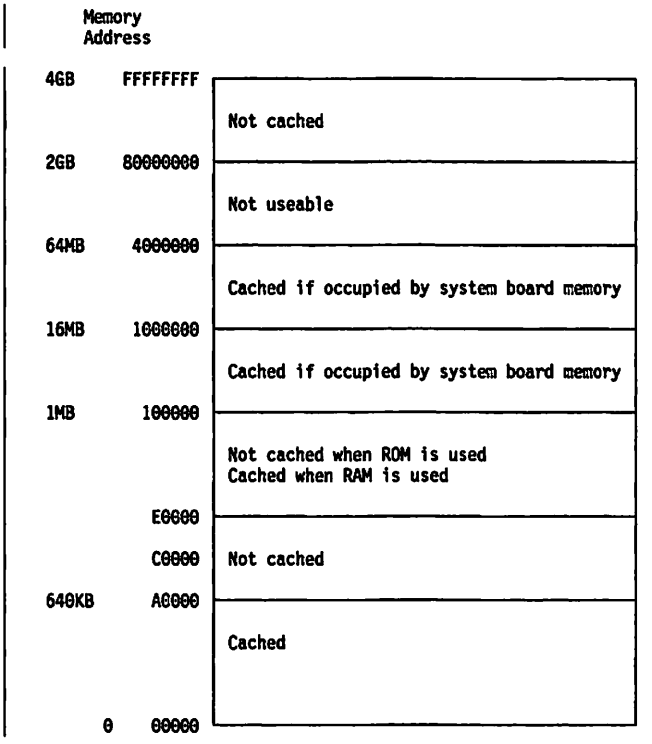


Figure 5-10. Type 2 Processor Complexes—Cache Address Map Summary

Type 2 Processor Complexes—Read-Only Memory Subsystem

The ROM subsystem is located on the processor complex and consists of 128KB in a 128K by 8-bit arrangement. The ROM is active at power-on at memory address space hex 000E0000 to 000FFFFF. The ROM contains the code that initializes the system to load and execute POST and BIOS code from a DASD device. ROM is also assigned at the top of the 4GB memory address space from hex FFFE0000 to FFFFFFFF.

Section 6. Type 3 Processor Complexes

Description 6-3
Type 3A 6-4
Type 3 Processor Complexes—I/O Address Map 6-7
Type 3 Processor Complexes—Level 2 Cache 6-7
Type 3 Processor Complexes—Memory Subsystem 6-8
Type 3 Processor Complexes—Memory Presence Detect 6-9
Type 3 Processor Complexes—Cache Address Map 6-10
Type 3 Processor Complexes—Read-Only Memory Subsystem 6-12

© Copyright IBM Corp. 1990, 1992

Notes:

Description

The processor complex provides certain devices and features that work in conjunction with devices and features provided by the system board. In addition, the processor complex determines system performance and certain channel timings. This section describes those aspects of the processor complex.

Type 3 has one processor complex. Programs can identify the processor complex by reading the model and submodel bytes. Interrupt 15H, Return System Configuration Parameters function ((AH)=C0H), returns the model byte, submodel byte, BIOS revision code, and other configuration information. The following figure shows the model byte, submodel byte, and speed of the processor complex.

Model Byte	Submodel Byte	Speed	Processor Complex
F8	29	50 MHz	Type 3A

Figure 6-1. Type 3 Processor Complexes—Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems.

Type 3A

The following figure shows the devices and features for the type 3A processor complex.

Device	Type	Features
Microprocessor	—	80486DX—50 MHz, 32-bit address and 32-bit data interface
Cache	—	8KB, 4-way, write-through, internal cache, 256KB external L2 cache
ROM Subsystem	—	128KB physical ROM
RAM Subsystem	—	Eight-connector support, 2MB to 64MB interleaved, parity/ECC expandable on the system board only
DMA Controller	2	Eight independent DMA channels, 32-bit DMA single or burst transfers and read verification
Math Coprocessor	—	Math coprocessor functions included in 80486DX

Figure 6-2. Type 3A Processor Complex—Features and Devices

The following figure shows the performance and other timing information for the type 3A processor complex. These timings affect the channel performance for operations involving the processor complex or system board memory.

Note: All of the timings in Figure 6-3, Figure 6-4 on page 6-6, and Figure 6-5 on page 6-7 are typical values. Timings can vary depending on microprocessor workload, cycle mix, bus master workload, and asynchronous clocks.

Device	Cycle Time (ns)
Microprocessor (50 MHz—20 ns Clock)	
I/O access	
Default transfer cycle	430
Extended transfer cycle	505
Refresh Rate (Typically performed every 15.1 μs)	500 (min)
DMA Controller (20 MHz—50 ns Clock)	
Accesses to system board memory: 70 ns/80 ns/85 ns (Parity/ECC)	
Single transfer read	
Page hit	325
Page miss	225
Burst transfer read	
Page hit	475 (16 bytes)
Page miss	575 (16 bytes)
Single transfer write	
Page hit	200
Page miss	300
Single transfer write (partial)	
Page hit	375
Page miss	475
Burst transfer write	
Page hit	475 (16 bytes)
Page miss	575 (16 bytes)
Accesses to Micro Channel	
Default cycle	300
Extended cycle	375

Note: A transfer can be a byte (8 bits), word (16 bits), or doubleword (32 bits).

Figure 6-3. Type 3A Processor Complex—System Performance Specifications

Device	Cycle Time (ns) Parity			Cycle Time (ns) ECC
	70 ns	80 ns	85 ns	70 ns
Microprocessor (50 MHz—20 ns Clock with L2 Cache)				
Memory read (cache hit)				
Burst†	100	100	100	100
Non-burst	40	40	40	40
Memory read (cache miss, page hit)				
Burst†	440	465	465	440
Non-burst	280	305	305	280
Memory read (cache miss, page miss)				
Burst†	540	565	565	540
Non-burst	380	405	405	380
Memory write (partial write, cache hit)				
Posted/non-posted	100	100	100	100
Page hit	155	180	180	155
Page miss	255	280	280	255
Memory write (partial write, cache miss)				
Posted/non-posted	100	100	100	100
Page hit	330	355	355	330
Page miss	430	455	455	430
Memory write (full write, cache hit/miss)				
Posted/non-posted	60	60	60	60
Page hit	155	180	180	155
Page miss	255	280	280	255

† Burst refers to 16 bytes.

Figure 6-4. Type 3A Processor Complex—Memory Performance Specifications

Device	Cycle Time (ns)
Channel Bus Master	
Basic transfer	
Single transfer read	500
First transfer of block read	500
Subsequent transfer of block reads	200
Single transfer write	200
First transfer of block write	200
Subsequent transfer of block writes	200
Streaming data transfer	
First access read	500
Subsequent access read	40 Mbps (max)
Write	40 Mbps (max)

Note: A transfer can be a byte (8 bits), word (16 bits), or doubleword (32 bits).

Figure 6-5. Type 3A Processor Complex—Channel Bus Master Performance Specifications

Type 3 Processor Complexes—I/O Address Map

The following shows the I/O address for devices located on the processor complex.

Hex Addresses	Device
0000–001F	DMA controller (0–3)
0081–0083, 0087	DMA Page registers (0–3)
0089–008B, 008F	DMA Page registers (4–7)
0090	Central arbitration control point
00C0–00DF	DMA controller (4–7)

Figure 6-6. Type 3 Processor Complexes—I/O Address Map

Type 3 Processor Complexes—Level 2 Cache

The level 2 (L2) cache provides the system microprocessor with an additional 256KB cache. It operates as a two-way, set-associative, write-through cache with parity. The primary cache in the 80486DX must be enabled to operate the secondary cache.

Type 3 Processor Complexes—Memory Subsystem

Memory on the system board is ECC or parity-checked, interleaved random-access memory and must be installed in matched pairs: one in an A connector and one in the matching B connector (for memory connector information, see "System Board Memory Connectors" on page 3-8). The memory in each pair must be the same speed and size. All memory must be of the same type, either all ECC or all parity checked. System memory on adapters in the channel is not supported.

System board memory is designed so that the system microprocessor can access memory while a bus master has control of the channel. The memory controller manages this dual access by interleaving the microprocessor and bus master accesses. In addition, system board memory is organized into pairs of banks so that the microprocessor can perform burst cycles with two-way interleaved accesses.

Type 3 Processor Complexes—Memory Presence Detect

The presence-detect signals are used by the system to determine the size and speed of memory on the single inline memory module (also called *memory module*). The pins are either not connected (1) or connected to ground (0).

A set of 4 bits shows the state of all presence-detect signals for a specific memory connector; the bit is 0 when the signal is connected to ground. The following figure shows the information indicated by these bits, as well as the bank size of the memory module. Combinations that are not shown are reserved.

The presence-detect information indicates the speed, size, and organization of a memory module. The type information, indicating either ECC or parity error detection of each memory module, also must be used to determine the type of memory module installed.

Note: Some of the presence-detect bits are the same. They are differentiated by the type of memory (parity or ECC). You must first read the System Board POS Register 3 to determine the type, then the presence-detect bits.

See "System Board POS Register 3 (Hex 0103)" on page 2-9, Figure 2-6 on page 2-9, and Figure 2-8 on page 2-10 for more information.

Presence Detect 3 2 1 0	Single Inline Memory Module Definition	Bank Size	Type
1 0 1 1	8MB 70-ns memory	4MB	ECC
1 0 1 1	8MB 70-ns memory	4MB	Parity
1 0 0 1	4MB 70-ns memory	4MB	ECC
0 1 0 0	4MB 70-ns memory	4MB	Parity
0 0 0 0	4MB 80-ns memory	4MB	Parity
1 1 0 0	2MB 70-ns memory	1MB	Parity
1 0 0 1	2MB 80-ns memory	1MB	Parity
0 1 0 1	2MB 85-ns memory	1MB	Parity
0 1 1 0	1MB 85-ns memory	1MB	Parity
1 1 1 1	Connector is empty		

Figure 6-7. Type 3 Processor Complexes—Presence-Detect Bits

Type 3 Processor Complexes—Cache Address Map

The following map is a summary of those addresses within the memory address space that can be cached. Only system board memory is mapped into the microprocessor level 1 cache and level 2 cache. The type 3A processor complex has a standard external 256KB L2 cache.

The system memory address space contains three cacheable regions:

- Region 1—Memory addresses from 0 up to 1MB
- Region 2—Memory addresses from 1MB up to 16MB
- Region 3—Memory addresses from 16MB up to 64MB.

All system board memory in region 2 and region 3 is cacheable. Programmable boundary registers for region 2 and region 3 control the upper boundaries of the memory space to be cached. The Set Configuration utility assigns memory to these cached regions, depending on the system configuration. POST establishes these cached regions, and they must not be altered.

Nonsystem memory can be located as follows:

- Region 1—In the area between memory addresses 0C0000 and 0DFFFF
- Region 2—Memory addresses from 16MB down to system memory
- Region 3—Memory addresses from 4GB (minus 1MB) down to system memory.

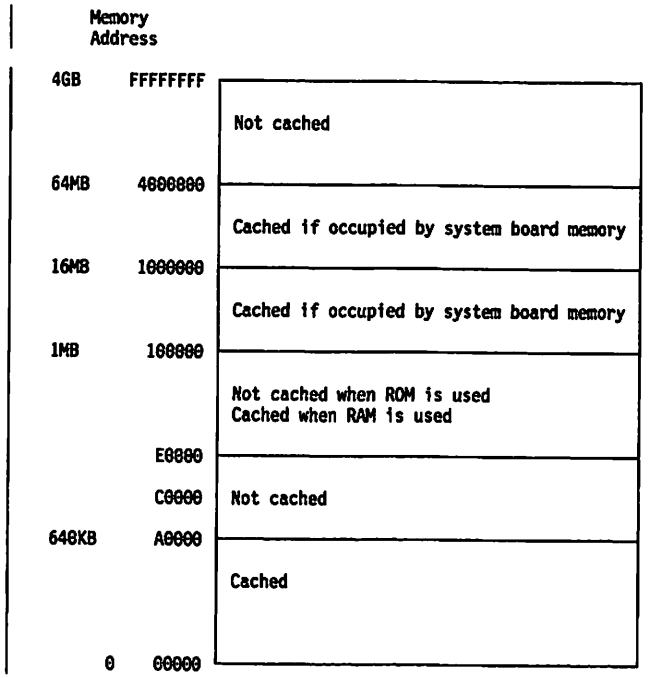


Figure 6-8. Type 3 Processor Complexes—Cache Address Map Summary

Type 3 Processor Complexes—Read-Only Memory Subsystem

The ROM subsystem is located on the processor complex and consists of 128KB in a 128K by 8-bit arrangement. The ROM is active at power-on at memory address space hex 000E0000 to 000FFFFF. The ROM contains the code that initializes the system to load and execute POST and BIOS code from a DASD device. ROM is also assigned at the top of the 4GB memory address space from hex FFFE0000 to FFFFFFFF.

Index

Numerics

80486DX performance 4-5, 4-8, 4-13, 6-5
80486DX2 performance 5-8
80486SX performance 4-11, 5-5

A

acoustic readings 1-10
activity light 1-10, 3-23
adapter setup register 2-13
address 20 gate 3-23
address maps
  POS 2-5
  system 1-6
alternate reset 3-24
arbiter programming 3-4
arbitration control point 3-3
arbitration level 3-3
arbitration register 3-4
arbitration, central control point 3-4

B

base memory bytes 3-20
battery 3-10
boot sequence 3-26
bus contention 2-3
bus priority assignments 3-3

C

cache connector 4-15
cache map 4-17, 5-12, 6-10
card selected feedback 2-6
-CD SFDBK 2-6
central arbitration control point 3-3
channel 1-3, 3-3
channel check 3-22
channel-check latch 3-22
CMOS RAM 3-10
codes, POST error 3-28
configuration CRC bytes 3-20
configuration, RT/CMOS 3-17
connector numbering, memory 3-8
connector, optional cache 4-15

D

date-century byte 3-20
description
  NMI 3-21
  password 3-25
  programmable option select 2-3
  real-time clock 3-10
  system 1-3
  system board 1-3
description, power supply 1-10
diagnostic status byte (RT/CMOS) 3-17
diskette drive connector 3-7
diskette drive information, POS 2-11, 2-12
diskette drive type byte 3-18
diskette overruns 3-4
DMA channels 3-4

E

enable NMI 3-11
equipment byte 3-19
error codes, POST 3-28
extended arbitration 3-6

F

failures and messages, POST 3-28
fault, overvoltage 1-12
features
  processor complex 1-5, 4-3, 5-3, 6-3
feedback, card selected 2-6
fixed disk drive activity light 1-10, 3-23

© Copyright IBM Corp. 1990, 1992

fixed disk drive initialization 3-17

G

gate A20 3-23

H

hardware compatibility 3-27

I

I/O address map 1-6
identifier, model 4-3, 5-3, 6-3
interrupts
  IRQ0 reset 3-22
  NMI reset 3-21

L

L2 cache 4-15, 6-7
light, fixed disk drive activity 1-10, 3-23
light, power 1-10

M

maximum current 1-9
measurements 1-9
memory
  connectors 3-8
  performance 4-5, 4-8, 4-11, 4-13, 5-5, 5-8, 6-5
  refresh 3-4
memory information, POS 2-9
memory numbering 3-8
memory presence detect 4-16, 5-11, 6-9
memory size miscompare 3-17
messages, POST error 3-28
Micro Channel 1-3, 3-3
microprocessor
  alternate reset 3-24
  gate A20 3-23
  mode switch compatibility 3-24
  performance 4-5, 4-8, 4-11, 4-13, 5-5, 5-8, 6-5
mode switching 3-24
model/submodel bytes 4-3, 5-3, 6-3

N

NMI mask 3-11
NMI service 3-4
NMI signal 3-4
noise readings 1-10
nonmaskable interrupt (NMI) 3-21
numbering, memory connector 3-8

O

operating system boot sequence 3-26
optional cache 4-15
output voltage sequencing 1-12
outputs, power supply 1-11
overvoltage fault 1-12

P

parallel port select 2-8
parity check 3-22
password, power-on 3-25
performance 4-5, 4-8, 4-11, 4-13, 5-5, 5-8, 6-5
ports, system 3-22
POS address map 2-5
POS register 2 2-7
POS register 3 2-9
POS register, diskette drive 2-11, 2-12
POST error codes 3-28
power specifications 1-9
power supply 1-3
power supply description 1-10
power supply LED 1-10
power supply output protection 1-12
power supply outputs 1-11
power-on password 3-25
processor cache map 4-17, 5-12, 6-10
processor complex 1-5
processor performance 4-5, 4-8, 4-11, 4-13, 5-5, 5-8, 6-5

programmable option select (POS) 2-3
address decode 2-6
address map 2-5
registers 2-5
setup procedures 2-4
setup register 2-6
system board 2-6
system board I/O 2-8
system configuration utilities 2-3
video 2-7
warning 2-3
programming, arbiter 3-4
protected mode switch 3-24
protection, power supply 1-12

R

real mode switch 3-24
real-time clock bytes 3-13
refresh 3-4
refresh request 3-22
registers
adapter setup 2-13
card feedback 2-6
miscellaneous system 3-22
RT/CMOS and NMI mask 3-11
RT/CMOS status registers 3-14
serial port 2 2-14
system board POS 2-6
system control 3-22
restore channel check 3-22
RT/CMOS address register 3-11
RT/CMOS RAM 3-10
password 3-25
secured area 3-23

S

second serial setup 2-14
selectable boot 3-26
sequencing, output voltage 1-12
serial port address select 2-11
set configuration 3-26
setup
bus contention 2-3
setup *(continued)*
registers 2-6
system board 2-6
system board I/O 2-8
video 2-7
shutdown status byte 3-17
size 1-9
sound specifications 1-10
speaker data enable 3-23
specifications 1-9, 4-5, 4-8, 4-11, 4-13, 5-5, 5-8, 6-5
performance 4-5, 4-8, 4-11, 4-13, 5-5, 5-8, 6-5
physical 1-9
system unit 1-9
startup sequence 3-26
status registers (RT/CMOS) 3-14
switch to real 3-24
system address map 1-6
system board 1-3
features 1-3
I/O register 2-7
memory connector 3-8
model identifier 4-3, 5-3, 6-3
POS registers 2-6
setup 2-6
system configuration utilities 2-3
system control port A 3-23
system control ports 3-22
system description 1-3
system overview 1-1
system ports, miscellaneous 3-22
system reset 3-21
system unit specifications 1-9

T

time status indicator 3-17

V

valid RAM bit 3-16
video setup 2-7

W

warnings
  arbitration 3-4
  central arbiter 3-5
  NMI mask 3-21
  POS 2-3
  real-time clock 3-11
  reserved areas xiii
watchdog status 3-23

Personal System/2
Model 95 XP 486
Technical Reference

Note

Before using this information and the product it supports, be sure to read the general information under "Notices" on page xi.

Fourth Edition (June 1992)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer of express or implied warranties in certain transactions, therefore, this statement may not apply to you.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Requests for technical information about IBM products should be made to your IBM Authorized Dealer or your IBM Marketing Representative.

© Copyright International Business Machines Corporation 1990, 1992. All rights reserved.
Note to U.S. Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Contents

Figures vii

Notices xi
Trademarks and Service Marks xi

Preface xiii

Section 1. System Overview 1-1
| Description 1-3
| System Board Devices and Features 1-4
| Processor Complex 1-5
System Board I/O Address Map 1-6
| Micro Channel Compatibility 1-7
| Specifications 1-9
Power Supply 1-10
Outputs 1-11
Output Protection 1-12
Voltage Sequencing 1-12
Power Supply Connectors 1-12

Section 2. Programmable Option Select 2-1
Description 2-3
POS Address Map 2-4
Card Selected Feedback Register (Hex 0091) 2-5
System Board Setup 2-5
System Board Enable/Setup Register (Hex 0094) 2-5
System Board POS Register 2 (Hex 0102) 2-6
| System Board POS Register 3 (Hex 0103) 2-7
System Board POS Registers 4 (Hex 0104) 2-9
System Board POS Register 5 (Hex 0105) 2-10
Diskette Drive POS Register 4 (Hex 0104) 2-11
Adapter Enable/Setup Register (Hex 0096) 2-12

Section 3. System Board 3-1
| Description 3-3
Micro Channel Implementation 3-3
| Central Arbiter 3-3
Diskette Drive Connector 3-7
| System Board Memory Connectors 3-8
| Real-Time Clock/Complementary Metal-Oxide Semiconductor
| (RT/CMOS) RAM 3-10
RT/CMOS Address Register and NMI Mask (Hex 0070) 3-11

© Copyright IBM Corp. 1990, 1992

RT/CMOS Data Register (Hex 0071) 3-11
RT/CMOS RAM I/O Operations 3-12
Real-Time Clock Bytes (Hex 000 – 00D) 3-13
| CMOS RAM Configuration 3-17
Miscellaneous System Functions and Ports 3-21
Nonmaskable Interrupt 3-21
| System Control Port B (Hex 0061) 3-22
System Control Port A (Hex 0092) 3-23
Power-On Password 3-25
Selectable Boot Sequence 3-26
Hardware Compatibility 3-27
| Error Codes 3-28

Section 4. Type 1 Processor Complexes 4-1
| Description 4-3
| Type 1A 4-4
| Type 1B 4-7
| Type 1C 4-10
| Type 1D 4-13
Type 1 Processor Complexes—I/O Address Map 4-15
| Type 1 Processor Complexes—Level 2 Cache 4-15
Type 1 Processor Complexes—Memory Subsystem 4-15
| Type 1 Processor Complexes—Memory Presence Detect . . . 4-16
| Type 1 Processor Complexes—Cache Address Map 4-17
Type 1 Processor Complexes—Read-Only Memory Subsystem 4-19

Section 5. Type 2 Processor Complexes 5-1
| Description 5-3
| Type 2A 5-4
| Type 2B 5-7
Type 2 Processor Complexes—I/O Address Map 5-10
| Type 2 Processor Complexes—Level 2 Cache 5-10
| Type 2 Processor Complexes—Memory Subsystem 5-10
| Type 2 Processor Complexes—Memory Presence Detect . . . 5-11
| Type 2 Processor Complexes—Cache Address Map 5-12
Type 2 Processor Complexes—Read-Only Memory Subsystem 5-14

| **Section 6. Type 3 Processor Complexes** 6-1
| Description 6-3
| Type 3A 6-4
| Type 3 Processor Complexes—I/O Address Map 6-7
| Type 3 Processor Complexes—Level 2 Cache 6-7
| Type 3 Processor Complexes—Memory Subsystem 6-8
| Type 3 Processor Complexes—Memory Presence Detect 6-9
| Type 3 Processor Complexes—Cache Address Map 6-10
| Type 3 Processor Complexes—Read-Only Memory Subsystem 6-12

Index X-1

Notes:

Figures

1-1. System Board Devices and Features 1-4
1-2. Processor Complexes 1-5
1-3. System Board I/O Address Map 1-6
1-4. Physical Specifications 1-9
1-5. Acoustical Readings 1-10
1-6. System-Provided Power 1-11
1-7. Load Current for Micro Channel Adapter Connector . . 1-11
1-8. Voltage Assignments for the Internal Drive Power-Supply Connectors 1-12
2-1. POS I/O Address Map 2-4
2-2. Card Selected Feedback Register (Hex 0091) 2-5
2-3. System Board Enable/Setup Register (Hex 0094) 2-6
2-4. System Board POS Register 2 (Hex 0102) 2-6
2-5. Parallel Port Select Bits 2-7
2-6. System Board POS Register 3 (Hex 0103)—Write 2-8
2-7. System Board POS Register 3 (Hex 0103)—Read 2-8
2-8. Error-Checking Information 2-8
2-9. System Board POS Register 4 (Hex 0104) 2-9
2-10. System Board POS Register 5 (Hex 0105) 2-10
2-11. Serial Port Address Select Bits 2-10
2-12. Diskette Drive POS Register 4 (Hex 0104) 2-11
2-13. Adapter Enable/Setup Register (Hex 0096) 2-12
3-1. Arbitration Bus Priority Assignments 3-4
3-2. Arbitration Register (Hex 0090)—Write 3-5
3-3. Arbitration Register (Hex 0090)—Read 3-5
3-4. Diskette Drive Connector 3-7
3-5. Memory Connector Numbering 3-8
3-6. System Board Memory Connector 3-9
3-7. RT/CMOS RAM Address Map 3-10
3-8. RT/CMOS Address Register and NMI Mask (Hex 0070) 3-11
3-9. RT/CMOS Data Register (Hex 0071) 3-11
3-10. Real-Time Clock Bytes (Hex 000 – 00D) 3-13
3-11. Status Register A (Hex 00A) 3-14
3-12. Status Register B (Hex 00B) 3-14
3-13. Status Register C (Hex 00C) 3-16
3-14. Status Register D (Hex 00D) 3-16
3-15. Diagnostic Status Byte (Hex 00E) 3-17
3-16. Diskette Drive Type Byte (Hex 010) 3-18
3-17. First Diskette Drive Type Byte (Bits 7 – 4) 3-18
3-18. Second Diskette Drive Type Byte (Bits 3 – 0) 3-18
3-19. Equipment Byte (Hex 014) 3-19
3-20. Equipment Byte (Bits 7, 6) 3-19

© Copyright IBM Corp. 1990, 1992

3-21. Equipment Byte (Bits 5, 4) 3-19
3-22. System Control Port B (Hex 0061)—Write 3-22
3-23. System Control Port B (Hex 0061)—Read 3-22
3-24. System Control Port A (Hex 0092) 3-23
3-25. POST Error Messages 3-29
4-1. Type 1 Processor Complexes—Model and Submodel Bytes 4-3
4-2. Type 1A Processor Complex—Features and Devices . . 4-4
4-3. Type 1A Processor Complex—System Performance Specifications 4-5
4-4. Type 1A Processor Complex—Memory Performance Specifications 4-6
4-5. Type 1B Processor Complex—Features and Devices . . 4-7
4-6. Type 1B Processor Complex—System Performance Specifications 4-8
4-7. Type 1B Processor Complex—Memory Performance Specifications 4-9
4-8. Type 1C Processor Complex—Features and Devices . 4-10
4-9. Type 1C Processor Complex—System Performance Specifications 4-11
4-10. Type 1C Processor Complex—Memory Performance Specifications 4-12
4-11. Type 1D Processor Complex—Features and Devices . 4-13
4-12. Type 1D Processor Complex—System Performance Specifications 4-14
4-13. Type 1D Processor Complex—Memory Performance Specifications 4-14
4-14. Type 1 Processor Complexes—I/O Address Map 4-15
4-15. Type 1 Processor Complexes—Presence-Detect Bits . 4-16
4-16. Type 1 Processor Complexes—Cache Address Map Summary 4-18
5-1. Type 2 Processor Complexes—Model and Submodel Bytes 5-3
5-2. Type 2A Processor Complex—Features and Devices . . 5-4
5-3. Type 2A Processor Complex—System Performance Specifications 5-5
5-4. Type 2A Processor Complex—Memory Performance Specifications 5-6
5-5. Type 2B Processor Complex—Features and Devices . . 5-7
5-6. Type 2B Processor Complex—System Performance Specifications 5-8
5-7. Type 2B Processor Complex—Memory Performance Specifications 5-9
5-8. Type 2 Processor Complexes—I/O Address Map 5-10
5-9. Type 2 Processor Complexes—Presence-Detect Bits . 5-11

5-10. Type 2 Processor Complexes—Cache Address Map Summary 5-13
6-1. Type 3 Processor Complexes—Model and Submodel Bytes 6-3
6-2. Type 3A Processor Complex—Features and Devices . . 6-4
6-3. Type 3A Processor Complex—System Performance Specifications 6-5
6-4. Type 3A Processor Complex—Memory Performance Specifications 6-6
6-5. Type 3A Processor Complex—Channel Bus Master Performance Specifications 6-7
6-6. Type 3 Processor Complexes—I/O Address Map 6-7
6-7. Type 3 Processor Complexes—Presence-Detect Bits . . 6-9
6-8. Type 3 Processor Complexes—Cache Address Map Summary 6-11

Notes:

Notices

References in this publication to IBM products, programs, or services do not imply that IBM intends to make these available in all countries in which IBM operates. Any reference to an IBM product, program or service is not intended to state or imply that only IBM's product, program, or service may be used. Any functionally equivalent product, program, or service that does not infringe any of IBM's intellectual property rights or other legally protectible rights may be used instead of the IBM product, program, or service. Evaluation and verification of operation in conjunction with other products, programs, or services, except those expressly designated by IBM, are the user's responsibility.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

Trademarks and Service Marks

The following terms, denoted by an asterisk (*) used in this publication, are trademarks of the IBM Corporation in the United States or other countries:

IBM
Micro Channel
Personal Computer AT
Personal System/2
PS/2

The following terms, denoted by a double asterisk (**) used in this publication, are trademarks of other companies as follows:

Intel	Intel Corporation
Intel486	Intel Corporation
Intel487	Intel Corporation
Motorola	Motorola, Incorporated
National Semiconductor	National Semiconductor Corporation

© Copyright IBM Corp. 1990, 1992

Notes:

Preface

The Technical Reference library is intended for those who develop hardware and software products for IBM Personal Computers and IBM Personal System/2 products. Users should understand computer architecture and programming concepts.

| Additions and changes have been made since the third edition of this
| manual. New or changed information is marked in the text with the
| same mark that is in the margin of this text.

This manual consists of the following sections:

Section 1, "System Overview," describes the system, features, and specifications.

Section 2, "Programmable Option Select," describes the registers used for configuration.

Section 3, "System Board," describes the system-specific hardware implementations of the Micro Channel architecture.

| Section 4, "Type 1 Processor Complexes," describes the
| components and features of the type 1 processor complexes.

| Section 5, "Type 2 Processor Complexes," describes the
| components and features of the type 2 processor complexes.

| Section 6, "Type 3 Processor Complexes," describes the
| components and features of the type 3 processor complexes.

Warning: The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

© Copyright IBM Corp. 1990, 1992

This technical reference should be used with the following publications. These publications contain additional information on many of the subjects discussed in this technical reference.

IBM Personal System/2 Hardware Interface Technical Reference—Architectures

IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference

Information about diskette drives, fixed disk drives, adapters, and external options are in separate option technical references.

Section 1. System Overview

| Description 1-3
| System Board Devices and Features 1-4
| Processor Complex 1-5
System Board I/O Address Map 1-6
| Micro Channel Compatibility 1-7
| Specifications 1-9
Power Supply 1-10
Outputs 1-11
Output Protection 1-12
Voltage Sequencing 1-12
Power Supply Connectors 1-12

© Copyright IBM Corp. 1990, 1992

Notes:

Description

The IBM* Personal System/2* (PS/2*) Model 95 XP 486 is a floor-standing computer system with a keyboard. The system can support up to four removable-media direct access storage devices (DASD) (diskette, tape, or optical) and three nonremovable-media DASD devices.

All Model 95 XP 486 systems use the same system board. The system board has:

- Eight Micro Channel* connectors
- Eight connectors for memory
- Parallel port, serial port, and diskette drive controllers
- Keyboard connector
- Pointing-device connector
- Processor complex connector
- 64-byte complementary metal-oxide semiconductor (CMOS) random access memory (RAM)
- Real-time clock.

* Trademark of the IBM Corporation.

System Board Devices and Features

The following figure lists the system board devices and features. The *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* describes devices common to PS/2 products by type number.

Device	Type	Features
Microprocessor	—	Connector for processor complex (see Figure 1-2 on page 1-5)
System Timers	1	Channel 0—System timer Channel 2—Tone generation for speaker Channel 3—Watchdog timer
RAM Subsystem	—	Eight connectors on system board Refer to the processor complex for more information
CMOS RAM Subsystem	—	64-byte CMOS RAM with real-time clock/calendar 8KB CMOS RAM extension (KB equals 1024 bytes) Battery backup
Audio Subsystem	1	Driven by —System-timer channel 2 —The 'audio sum node' signal
Interrupt Controller	1	16 levels of system interrupts Interrupts are level sensitive
Keyboard/Auxiliary Device Controller	2	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	2	Supports —3.5-in. diskette drive (1.44MB) —5.25-in. diskette drive (360KB and 1.2MB) —3.5-in. diskette drive (2.88MB)†
Serial Port Controller	3	RS-232C interface Programmable as serial ports 1–8 DMA, FIFO, and character modes Supports DMA operation
Parallel Port Controller	3	Programmable as parallel ports 1–4 Supports bidirectional input and output Supports DMA operation
Micro Channel	—	Eight connectors for Type 3 adapters —One 32-bit connector with auxiliary video extension —One 32-bit connector with base video extension —Six 32-bit connectors with matched memory extension One connector contains a fixed-disk adapter One connector contains a video adapter

† Not supported in all Model 95 XP 486 systems.

Figure 1-1. System Board Devices and Features

Processor Complex

The functions of the system can be changed depending on which processor complex is installed. The processor complex determines the model/submodel byte information. The major components on the processor complex are:

- System microprocessor
- System clock
- Direct memory access (DMA) controller
- Memory controller.

The processor complexes fall into one of three types (type 1, 2, or 3) depending on the following:

- Type of DMA controller installed (16- or 32-bit)
- Type of memory error detection supported (parity or ECC)
- Type of memory configuration supported (interleaved or noninterleaved).

The following figure lists the different processor complexes.

Processor Complex	Processor—Speed	Memory (Interleaved, Noninterleaved, or Both)	Error Detection (Parity, ECC, or Both)	Page
Type 1A	80486DX—25 MHz	Interleaved	Parity	4-4
Type 1B	80486DX—33 MHz	Interleaved	Parity	4-7
Type 1C	80486SX—20 MHz	Interleaved	Parity	4-10
Type 1D	80486DX—50 MHz	Interleaved	Parity	4-13
Type 2A	80486SX—25 MHz	Both	Parity	5-4
Type 2B	80486DX2—50 MHz	Both	Parity	5-7
Type 3A	80486DX—50 MHz	Interleaved	Both†	6-4

† The systems use *either* parity or ECC to detect memory errors *(but not a combination of both)*.

Figure 1-2. Processor Complexes

System Board I/O Address Map

Address (Hex)	Device
0020, 0021	Interrupt controller
0040, 0042–0044, 0047	System timers
0060	Keyboard, auxiliary device
0061	System Control Port B
0064	Keyboard, auxiliary device
0070, 0071	RT/CMOS and NMI mask
0091	Card Selected Feedback register
0092	System Control Port A
0094	System Board Enable/Setup register
0096	Adapter Enable/Setup register
00A0–00A1	Interrupt controller
0100–0107	Programmable option select
0108–010F	Information panel
0278–027D	Parallel port 3
02F8–02FF	Serial port 2
0378–037D	Parallel port 2
03BC–03BF	Parallel port 1
03F0–03F7	Diskette drive controller
03F8–03FF	Serial port 1
1278–127D	Parallel port 1 (DMA mode)
1378–137D	Parallel port 4
3220–3227	Serial port 3
3228–322F	Serial port 4
4220–4227	Serial port 5
4228–422F	Serial port 6
5220–5227	Serial port 7
5228–522F	Serial port 8
83F8–83FF	Serial port 1 (DMA mode)
82F8–82FF	Serial port 2 (DMA mode)
B220–B227	Serial port 3 (DMA mode)
B228–B22F	Serial port 4 (DMA mode)
C220–C227	Serial port 5 (DMA mode)
C228–C22F	Serial port 6 (DMA mode)
D220–D227	Serial port 7 (DMA mode)
D228–D22F	Serial port 8 (DMA mode)

Figure 1-3. System Board I/O Address Map

Micro Channel Compatibility

The following describes the system limitations in the support of Micro Channel procedures.

Streaming Data

The system board supports 10-MHz streaming-data procedures involving transfers between adapters.

Devices on the system board and the processor complex work with streaming-data adapters; however, they do not use the streaming-data procedure. Transfers default to the basic transfer procedure.

The exception is systems with the type 3A processor complex, which support the 16- and 32-bit, 100 nanoseconds streaming-data procedure. Masters accessing system board memory will receive a request to use the streaming-data procedure.

Data Parity

The system board supports data-parity procedures involving transfers between adapters.

Devices on the system board and the processor complex work with adapters that support data parity; however, they do not use the data-parity option. Transfers default to the basic transfer procedure.

The exception is systems with the type 3A processor complex, which support the data-parity option. Masters accessing system board memory, and slaves being addressed by the system master, will exchange data with parity included only if the given adapter supports the data-parity procedure.

Address Parity

The system board supports address-parity procedures involving transfers between adapters.

Devices on the system board and the processor complex work with adapters that support address parity; however, they do not use the address-parity option. Transfers default to the basic transfer procedure.

Selected Feedback Return Signal

Most system boards and processor complexes support the 'selected feedback return' signal, except for I/O devices at addresses below hex 0110. These devices are controlled

by the system master only and should not be accessed by bus masters.

The exception is systems with type 2 processor complexes, which do not support the 'selected feedback return' signal.

Synchronous Channel Check

Synchronous channel checks for exceptions other than Micro Channel data-parity exceptions, Micro Channel address-parity exceptions, and slave dependent exceptions generally are not supported in this system. The channel check exception reporting field in adapter POS will be set to disable synchronous channel checks and enable asynchronous channel checks.

The exception is systems with the type 3A processor complex. In these systems, all synchronous channel checks can be enabled.

Synchronous channel checks for slave dependent exceptions, Micro Channel data-parity exceptions, or Micro Channel address-parity exceptions, typically issued by slaves, are the responsibility of the master that owned the channel and issued the access to the slave. However, in this system, these channel checks can also be detected by logic on the system board, resulting in a nonmaskable interrupt (NMI).

DMA

In most systems, the DMA controller supports DMA slaves with 8-bit or 16-bit data widths. Transfers are limited to the memory address space below 16MB.

The exception is systems with the type 3A processor complex. In these systems, the DMA controller supports 8-bit, 16-bit, and 32-bit data widths. It can address memory space above 16MB. See the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* for more information.

Specifications

Size	
Width	203 mm (8.0 in.)
Depth	508 mm (20.0 in.)
Height	501 mm (19.75 in.)
Weight	
Minimum configuration	22 kg (50 lb)
Maximum configuration	30 kg (67 lb)
Cables	
Power cable	1.8 m (6 ft)
Keyboard cable	3.05 m (10 ft)
Air Temperature	
System on	
0 – 3000 ft	10.0 to 35.0°C (50 to 95°F)
3000 – 7000 ft	10.0 to 32.2°C (50 to 90°F)
System off	10.0 to 43.0°C (50 to 110°F)
Humidity	8% to 80%
Maximum Altitude	2134 m (7000 ft)
Heat Output	515 W (1757 BTU per hour)
Acoustical Readings	See Figure 1-5 on page 1-10
Electrical	
Input voltage	Range is switch selected Sinewave input required
Low range	90 (min) to 137 (max) V ac
High range	180 (min) to 265 (max) V ac
Input frequency	50 Hz ± 3 Hz or 60 Hz ± 3 Hz
Maximum current draw	
Low range	9.2 A
High range	4.6 A
Input in kilovolt-ampere (kVA)	
Minimum configuration (as shipped)	0.18 kVa
Maximum configuration	0.78 kVa
Electromagnetic Compatibility	FCC Class B

Figure 1-4. Physical Specifications

Description	L_{WAd} in bels Operate	Idle	L_{pAm} in dB Operate	Idle	$<L_{pA}>_m$ in dB Operate	Idle
Model 95 XP 486	5.3	5.3	35	35	36	36

Notes:

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

All measurements are made in accordance with ANSI standard 12.10 and are reported in conformance with ISO DIS 9296.

The measurements are preliminary data and are subject to change.

Figure 1-5. Acoustical Readings

Power Supply

The power supply requires a sinewave input and converts the ac input voltage to three dc output voltages. The switch near the power cord is used to select the input-voltage range. The power supply provides power for the following:

- System board
- Processor complex
- Micro Channel adapters
- Internal diskette drives
- Internal fixed disk drives
- Auxiliary device
- Keyboard.

The power switch and one light-emitting diode (LED) are on the front of the system unit. The power supply is operating properly when the LED is lit.

Outputs

The power supply provides separate voltage sources for the system board and the drives. The system board voltages are +5 V dc, +12 V dc, and −12 V dc. The voltages for the internal drives are +5 V dc and +12 V dc. The following is a list of the power provided for system components.

System Component	Maximum Current	
	+12 V dc	+5 V dc
Internal fixed disk drives†	2.5 A	1.5 A
Total of fixed disk drives	7.5 A	4.6 A
Auxiliary device		300 mA
Keyboard		275 mA
† Per power supply connector		

Figure 1-6. System-Provided Power

The following are the load currents allowed for the connectors for the Type 3 Micro Channel adapters. The formulas used to determine the power requirements and the definition of adapter types can be found in the section of the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures* that describes the Micro Channel architecture.

Supply Voltage	Maximum Current
+ 5.0 V dc	2.0 A
+12.0 V dc	0.175 A
−12.0 V dc	0.040 A

Figure 1-7. Load Current for Micro Channel Adapter Connector

Output Protection

A short circuit placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state with no damage to the power supply.

If an overvoltage fault occurs (internal to the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of the nominal value of the power supply.

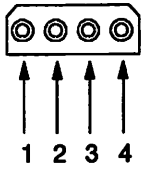
If either of these shutdown states occurs, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least one second.

Voltage Sequencing

At power-on, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Power Supply Connectors

The power supply provides three 4-pin connectors for internal devices. The connectors can be extended to provide power to more than one internal drive as long as the total power for all connectors does not exceed the connector specifications shown in Figure 1-6 on page 1-11.



Pin	Signal	Pin	Signal
1	+12 V dc	3	dc return
2	dc return	4	+5 V dc

Figure 1-8. Voltage Assignments for the Internal Drive Power-Supply Connectors

Section 2. Programmable Option Select

Description 2-3
POS Address Map 2-4
Card Selected Feedback Register (Hex 0091) 2-5
System Board Setup 2-5
System Board Enable/Setup Register (Hex 0094) 2-5
System Board POS Register 2 (Hex 0102) 2-6
System Board POS Register 3 (Hex 0103) 2-7
System Board POS Registers 4 (Hex 0104) 2-9
System Board POS Register 5 (Hex 0105) 2-10
Diskette Drive POS Register 4 (Hex 0104) 2-11
Adapter Enable/Setup Register (Hex 0096) 2-12

© Copyright IBM Corp. 1990, 1992

Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used on the Model 95 XP 486 system board. For additional POS information, refer to the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures.*

Warning:

- IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignment of the same system resource, improper operation of the feature, loss of data, or possible damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention will occur, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- Bit 7 (channel reset) in the Adapter Enable/Setup register must be set to 0 to program the adapters.
- Only 8-bit instructions are supported for setup operations. Using 32- or 16-bit I/O instructions on 8-bit POS registers will cause erroneous data to be written or read.

Setup functions respond to I/O addresses hex 0100 through 0107 only when their unique setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register must be set to 1 to allow adapter setup.
- Bits 7–0 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to a system board function.

System Board Setup:

- Bits 7 and 6 in the System Board Enable/Setup register must be set to 0 individually while other bits are set to 1 to set up corresponding system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.

POS Address Map

The following figure shows the organization of the I/O address space used by POS. Bit 0 of POS Register 2 and bits 6 and 7 of POS Register 5 are fixed. All other bits in POS Registers 2 through 5 are free form.

Address (Hex)	Function
0094	System Board Enable/Setup register
0096	Adapter Enable/Setup register
0100	POS Register 0—Adapter Identification byte (low byte)
0101	POS Register 1—Adapter Identification byte (high byte)
0102	POS Register 2—Option Select Data byte 1 Bit 0 is card enable.
0103	POS Register 3—Option Select Data byte 2
0104	POS Register 4—Option Select Data byte 3
0105	POS Register 5—Option Select Data byte 4
0106	Reserved
0107	Reserved

Figure 2-1. POS I/O Address Map

Card Selected Feedback Register (Hex 0091)

When an adapter is addressed, it responds by setting the '-card selected feedback' signal (-CD SFDBK) to active. -CD SFDBK is derived from the address decode and driven by a totem pole driver. It is latched by the system board and can be read through the Card Selected Feedback register at address hex 0091.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and thereby determine if the system board I/O or an adapter is addressed and functioning.

Bit	Function
7–1	Reserved
0	-Card selected feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7–1 These bits are reserved.

Bit 0 This bit is set to 1 when -CD SFDBK was active on a previous cycle or when the system board I/O functions (diskette drive, serial, or parallel interfaces) are accessed by an I/O or DMA cycle. Reading this register resets this bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information during setup. The diskette drive controller, serial port, and parallel port are treated as a single device. The System Board Enable/Setup register is used to place the system board into the setup mode.

System Board Enable/Setup Register (Hex 0094)

This is a read/write register; all bits in this register default to 1 (enabled). Setup functions should be accessed only one at a time.

Bit	Function
7	Enable/setup system board functions
6	Enable/setup diskette drive functions
5–0	Reserved

Figure 2-3. System Board Enable/Setup Register (Hex 0094)

Bit 7 When this bit is set to 0, various system board I/O functions are placed in the setup mode. The diskette drive controller, serial port, and parallel port are controlled through System Board POS Register 2 (hex 0102).

When this bit is set to 1, the system board function is enabled.

Bit 6 Additional setup for diskette drive. When this bit is set to 0, these setup functions are available through the Diskette Drive POS Register 4.

Bits 5–0 These bits are reserved.

System Board POS Register 2 (Hex 0102)

When the system board is in the setup mode, the diskette drive controller, serial port, and parallel port are controlled by this read/write register. Reading this register returns the current state of these system board functions.

Bit	Function
7	Disable parallel port extended mode
6, 5	Select parallel port
4	Enable parallel port
3	Select serial port IRQ
2	Enable serial port
1	Enable diskette drive interface
0	Enable system board

Figure 2-4. System Board POS Register 2 (Hex 0102)

Bit 7 When set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional (extended mode) interface. When set to 1, this bit disables the bidirectional mode. This bit is set to 0 after power-on.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Address (Hex)	Interrupt Level
0 0	Parallel 1	03BC–03BF†	7
0 1	Parallel 2	0378–037D	7
1 0	Parallel 3	0278–027D	7
1 1	Parallel 4	1378–137D	7

† The addresses are hex 1278–127D for DMA operations

Figure 2-5. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bit 3 When this bit is set to 1, the serial port uses interrupt request level 4. When this bit is set to 0, the serial port uses interrupt request level 3.

Bit 2 When this bit and bit 0 are set to 1, the system board serial port is enabled.

Bit 1 When this bit and bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When set to 1, this bit allows bits 4, 2, and 1 to enable and disable their respective devices. When set to 0, this bit disables the diskette drive interface, system board serial port, and system board parallel port, regardless of the state of bits 4, 2, and 1.

System Board POS Register 3 (Hex 0103)

The system board has connectors that provide for installation of eight single inline memory modules (also called *memory modules*) (for more information about these memory connectors, see "System Board Memory Connectors" on page 3-8). Information about each memory module is contained in four read-only data registers; each data register is selected by writing its index to the write-only index register.

POS Register 3 provides access to the read-only data registers and a write-only index register. To determine the memory information for a particular connector, write the appropriate index to POS Register 3, then read POS Register 3. The following figure shows the relationship of the index value, the memory connector, and the available data register information.

Index Value (Hex)	Description
01	Presence detect information for A1 and B1
05	Presence detect information for A2 and B2
09	Presence detect information for A3 and B3
0D	Presence detect information for A4 and B4
10	Error-checking information for all connectors

Note: Values that are not shown are reserved.

Figure 2-6. System Board POS Register 3 (Hex 0103)—Write

The following information is returned by reading POS Register 3 when the appropriate value is written to POS Register 3. For coding of the presence detect signals, see Figure 4-15 on page 4-16, Figure 5-9 on page 5-11, and Figure 6-7 on page 6-9.

Bit	Description
7	Presence detect 3, connector B
6	Presence detect 2, connector B
5	Presence detect 1, connector B
4	Presence detect 0, connector B
3	Presence detect 3, connector A
2	Presence detect 2, connector A
1	Presence detect 1, connector A
0	Presence detect 0, connector A

Figure 2-7. System Board POS Register 3 (Hex 0103)—Read

The following information is returned when index value hex 10 is selected.

Bit	Description
7	Parity/-ECC, connector B4
6	Parity/-ECC, connector A4
5	Parity/-ECC, connector B3
4	Parity/-ECC, connector A3
3	Parity/-ECC, connector B2
2	Parity/-ECC, connector A2
1	Parity/-ECC, connector B1
0	Parity/-ECC, connector A1

Figure 2-8. Error-Checking Information

Each bit indicates the type of error-checking method used by that memory module— data-parity or error-checking and correction (ECC). When the bit is set to 1, the module in the specified connector uses

| the data-parity method to check for errors. When the bit is set to 0,
| the module uses the ECC method.

System Board POS Registers 4 (Hex 0104)

This register is accessed when bit 7 of the System Board Enable/Setup register is set to 0. The register is used to specify the arbitration levels used by the serial port during transmit and receive operations in the DMA mode.

Bit	Description
7–4	Receive arbitration level
3–0	Transmit arbitration level

Figure 2-9. System Board POS Register 4 (Hex 0104)

Bits 7–4 These bits select the arbitration level used for the transfer of data that is being received through the serial port.

Bits 3–0 These bits select the arbitration level used for the transfer of data that is being transmitted through the serial port.

System Board POS Register 5 (Hex 0105)

This register is used to specify the arbitration level used by the parallel port and the I/O addresses used by the serial port.

Bit	Description
7	Reserved
6–4	Select serial address
3–0	Parallel port arbitration level

Figure 2-10. System Board POS Register 5 (Hex 0105)

Bit 7 This bit is reserved.

Note: This bit might be read as 0 but does not indicate any occurrence of channel check.

Bits 6–4 These bits are used to select the I/O addresses that are used by the serial port on the system board. The I/O addresses can be the compatible addresses or the extended address (see Serial Port Controller in the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* for more information on addressing).

Bits 6 5 4	Assignment	Address (Hex)	
		Compatible	Extended
0 0 0	Serial 1	03F8–03FF	83F8–83FF
0 0 1	Serial 2	02F8–02FF	82F8–82FF
0 1 0	Serial 3	3220–3227	B220–B227
0 1 1	Serial 4	3228–322F	B228–B22F
1 0 0	Serial 5	4220–4227	C220–C227
1 0 1	Serial 6	4228–422F	C228–C22F
1 1 0	Serial 7	5220–5227	D220–D227
1 1 1	Serial 8	5228–522F	D228–D22F

Figure 2-11. Serial Port Address Select Bits

Bits 3–0 These bits select the arbitration level used by the parallel port controller.

Diskette Drive POS Register 4 (Hex 0104)

This register is accessed when bit 6 of the System Board Enable/Setup register is set to 0. The register is used to specify the arbitration level used by the diskette drive controller.

Bit	Description
7–4	Reserved
3–0	Diskette drive arbitration level

Figure 2-12. Diskette Drive POS Register 4 (Hex 0104)

Bits 7–4 These bits are reserved.

Bits 3–0 These bits select the arbitration level used by the diskette drive controller.

Adapter Enable/Setup Register (Hex 0096)

This read/write register selects the connector to be configured.

Bit	Symbol
7	Channel reset
6–4	Reserved (set to 0)
3	Enable card setup
2–0	Channel select 2–0

Figure 2-13. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6–4 These bits are reserved and must be set to 0.

Bit 3 When set to 1, this bit enables the '-card setup' signal selected by bits 2 through 0.

Bits 2–0 These bits are the address bits for the '-card setup' signal. Connectors 1 through 8 are addressed as 0 through 7. When bit 3 is set to 1, these bits select the connector for setup cycles.

Each channel connector has a unique '-card setup' signal (-CD SETUP) associated with it. This signal is used to select the adapters for setup cycles, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Note: -CD SETUP goes active only when an operation is performed in the I/O address range hex 0100 through 0107.

Section 3. System Board

| Description 3-3
Micro Channel Implementation 3-3
| Central Arbiter 3-3
Arbitration Bus Priority Assignments 3-3
Central Arbiter Programming 3-4
Diskette Drive Connector 3-7
| System Board Memory Connectors 3-8
| Real-Time Clock/Complementary Metal-Oxide Semiconductor
| (RT/CMOS) RAM 3-10
RT/CMOS Address Register and NMI Mask (Hex 0070) 3-11
RT/CMOS Data Register (Hex 0071) 3-11
RT/CMOS RAM I/O Operations 3-12
Real-Time Clock Bytes (Hex 000–00D) 3-13
| CMOS RAM Configuration 3-17
Miscellaneous System Functions and Ports 3-21
Nonmaskable Interrupt 3-21
| System Control Port B (Hex 0061) 3-22
System Control Port A (Hex 0092) 3-23
Power-On Password 3-25
Selectable Boot Sequence 3-26
Hardware Compatibility 3-27
| Error Codes 3-28

© Copyright IBM Corp. 1990, 1992

Notes:

Description

This section describes channel differences and various system ports and connectors for the Model 95 XP 486. For additional information about these and other topics, refer to the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces.*

Micro Channel Implementation

This section describes the implementation of the Micro Channel architecture on Model 95 XP 486 systems. For general Micro Channel information, refer to *IBM Personal System/2 Hardware Interface Technical Reference—Architectures.*

Note: The system does not support adapters that use the matched memory extension.

Central Arbiter

The central arbitration control point gives intelligent subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. This arbiter supports up to 16 arbitrating devices.

Arbitration Bus Priority Assignments

The following figure shows the assignment of arbitration levels. The functions with the lowest arbitration level have the highest priority.

ARB Level	Primary Assignment
-2	Memory refresh
-1	NMI
0	DMA channel 0 (programmable to any arbitration level)
1	DMA channel 1
2	DMA channel 2
3	DMA channel 3
4	DMA channel 4 (programmable to any arbitration level)
5	DMA channel 5
6	DMA channel 6
7	DMA channel 7
8–B	Available
C	SCSI adapter
D, E	Available
F	System microprocessor

Figure 3-1. Arbitration Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation, and by the previous controlling master. To prevent overrun, the diskette drive controller should not be held inactive for more than 12 microseconds.

Nonmaskable interrupt (NMI) service is executed at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal is in the arbitrate state.

When the central arbitration control point receives a level -1 request (NMI, a system board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level -1 request, and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following figures.

Bit	Definition
7	Enable system microprocessor cycle
6	Arbitration mask
5	Enable extended arbitration
4–0	Reserved

Figure 3-2. Arbitration Register (Hex 0090)—Write

Bit	Definition
7	Enable system microprocessor cycle
6	Arbitration masked by NMI
5	Bus time-out
4	Reserved
3–0	Value of arbitration bus during previous grant state

Figure 3-3. Arbitration Register (Hex 0090)—Read

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 1 by POST.

Reading this bit as a 1 indicates system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 enables extended arbitration. The minimum arbitration cycle is 300 nanoseconds; this bit extends that minimum cycle to 600 nanoseconds. This bit is set to 0 by POST.

Reading this bit as a 1 indicates that a bus time-out has occurred, and resets bit 6 in this register to 0.

Bit 4 This bit is reserved and must be 0.

Bits 3–0 These bits are undefined for a write operation and should be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Diskette Drive Connector

The system provides three 2-by-17-pin connectors for attaching internal diskette drives. Each connector passes control and data signals between the diskette drive controller on the system board and the drives, and provides the power to each drive.

The following figure shows the signal assignments and pin numbers for the diskette drive connectors.

Pin	Signal	Pin	Signal
1	Ground	2	Data rate select 1
3	+5 V dc	4	Drive type ID 1
5	Ground	6	+12 V dc
7	Ground	8	-Index
9	Drive type ID 0	10	Reserved
11	Ground	12	-Drive select
13	Ground	14	Reserved
15	Ground	16	-Motor enable
17	Media type ID 1	18	-Direction in
19	Ground	20	-Step
21	Ground	22	-Write data
23	Ground	24	-Write enable
25	Ground	26	-Track 0
27	Media type ID 0	28	-Write protect
29	Ground	30	-Read data
31	Ground	32	-Head 1 select
33	Data rate select 0	34	-Diskette change

Figure 3-4. Diskette Drive Connector

System Board Memory Connectors

The Model 95 XP 486 system board has eight 72-pin memory connectors that support a variety of single inline memory modules (also called *memory modules*). The connectors are numbered as viewed from the top of the system.

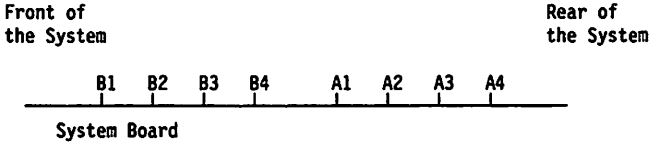


Figure 3-5. Memory Connector Numbering

The following figure shows the pin assignments for the 1- by 72-pin memory connectors. Refer to "Type 1 Processor Complexes—Memory Presence Detect" on page 4-16, "Type 2 Processor Complexes—Memory Presence Detect" on page 5-11, and "Type 3 Processor Complexes—Memory Presence Detect" on page 6-9 for decoding of the presence-detect signals.

Pin	Signal	Pin	Signal
1	Ground	37	Parity data 1/ECC check bit 1
2	Data 0	38	Parity data 3/ECC check bit 3
3	Data 16	39	Ground
4	Data 1	40	Column address strobe 0
5	Data 17	41	Column address strobe 2
6	Data 2	42	Column address strobe 3
7	Data 18	43	Column address strobe 1
8	Data 3	44	Row address strobe 0
9	Data 19	45	Row address strobe 1
10	+5 V dc	46	Block select 1/ECC check bit 5
11	-Column address strobe P	47	Write enable
12	Address 0	48	+Parity/-ECC
13	Address 1	49	Data 8
14	Address 2	50	Data 24
15	Address 3	51	Data 9
16	Address 4	52	Data 25
17	Address 5	53	Data 10
18	Address 6	54	Data 26
19	Reserved	55	Data 11
20	Data 4	56	Data 27
21	Data 20	57	Data 12
22	Data 5	58	Data 28
23	Data 21	59	+5 V dc
24	Data 6	60	Data 29
25	Data 22	61	Data 13
26	Data 7	62	Data 30
27	Data 23	63	Data 14
28	Address 7	64	Data 31
29	Block select 0/ECC check bit 4	65	Data 15
30	+5 V dc	66	Block select 2/ECC check bit 6
31	Address 8	67	Presence detect 0
32	Address 9	68	Presence detect 1
33	Row address strobe 3	69	Presence detect 2
34	Row address strobe 2	70	Presence detect 3
35	Parity data 2/ECC check bit 2	71	Block select 3
36	Parity data 0/ECC check bit 0	72	Ground

Figure 3-6. System Board Memory Connector

Real-Time Clock/Complementary Metal-Oxide Semiconductor (RT/CMOS) RAM

The real-time clock/complementary metal-oxide semiconductor (RT/CMOS) RAM module contains the real-time clock and 64 bytes of CMOS RAM. The internal clock circuitry uses 14 bytes of this memory, and the rest is allocated for configuration and system-status information.

In addition to the 64 bytes of CMOS RAM, an 8KB CMOS RAM extension is provided for configuration and other system information.

A battery maintains voltage to the RT/CMOS RAM and 8KB CMOS RAM extension when the power supply is not in operation.

The system cover can be locked to prevent battery removal and, consequently, prevents the loss of password and configuration information.

The following figure shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000–00D	Real-time clock bytes
00E	Diagnostic Status byte
00F	Shutdown Status byte
010	Diskette Drive Type byte
011	Reserved
012	Reserved
013	Reserved
014	Equipment byte
015, 016	Low and High Base-Memory bytes
017, 018	Low and High Expansion-Memory bytes
019–031	Reserved
032, 033	Configuration CRC bytes
034	Reserved
035, 036	Low and high usable memory above 1MB to 16MB
037	Date-Century byte
038–3F	Reserved

Figure 3-7. RT/CMOS RAM Address Map

RT/CMOS Address Register and NMI Mask (Hex 0070)

This read/write register is used in conjunction with the RT/CMOS Data register (hex 0071) to read and write the RT/CMOS RAM bytes.

Bit	Function
7	NMI mask
6	Reserved
5–0	RT/CMOS RAM address

Figure 3-8. RT/CMOS Address Register and NMI Mask (Hex 0070)

Warning: The operation following a write operation to hex 0070 must access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Bit 7 When this bit is set to 1, the NMI is masked (the NMI is disabled). This bit is set to 1 by a power-on reset. This is a write-only bit.

Bit 6 This bit is reserved.

Bits 5–0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This port is used in conjunction with the RT/CMOS Address and NMI Mask register (hex 0070) to read and write the RT/CMOS RAM bytes.

Bit	Function
7–0	RT/CMOS data

Figure 3-9. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts must be masked to prevent other interrupt routines from changing the CMOS Address register before data is read from or written to.

Warning: The operation following a write operation to hex 0070 must access hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Writing to RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Write the data to address hex 0071.
3. Write the address hex 0F to the RT/CMOS and NMI Mask register; this leaves address hex 0070 pointing to the Shutdown Status byte (hex 0F).
4. Read from address hex 0071 to restore the RT/CMOS (see the warning above).

Reading from RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Read the data from address hex 0071.
3. Write the address hex 0F to the RT/CMOS and NMI Mask register; this leaves address hex 0070 pointing to the Shutdown Status byte (hex 0F).
4. Read from address hex 0071 to restore the RT/CMOS.

Real-Time Clock Bytes (Hex 000 – 00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following figure.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second alarm	1
002	Minutes	2
003	Minute alarm	3
004	Hours	4
005	Hour alarm	5
006	Day of week	6
007	Date of month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-10. Real-Time Clock Bytes (Hex 000 – 00D)

Note: The Setup program initializes Status Registers A and B when the time and date are set. Interrupt 1AH is the BIOS interface to read and set the time and date. It initializes the register in the same way that the Setup program does.

Status Register A (Hex 00A)

Bit	Function
7	Update in progress
6–4	22-stage divider
3–0	Rate-selection bits

Figure 3-11. Status Register A (Hex 00A)

Bit 7 When set to 1, this bit indicates the time-update cycle is in progress. When set to 0, it indicates the current date and time can be read.

Bits 6–4 These 3 divider-selection bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768-kHz time base. This is the only value supported by the system for proper timekeeping.

Bits 3–0 These bits allow the selection of a divider output frequency. The system initializes the rate-selection bits to a binary 0110, which selects a 1.024-kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Enable periodic interrupt
5	Enable alarm interrupt
4	Enable update-ended interrupt
3	Enable square wave
2	Date mode
1	24-hour mode
0	Enable daylight savings

Figure 3-12. Status Register B (Hex 00B)

Bit 7 When set to 0, this bit updates the cycle, normally by advancing the counts at a rate of one per second. When set to 1, this bit immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This bit is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

Bit 5 When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit indicates if the time-and-date calendar updates use binary or binary-coded-decimal (BCD) formats. When set to 1, this bit indicates a binary format. The system initializes this bit to 0.

Bit 1 This bit establishes if the hours byte is in the 24-hour or 12-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When set to 1, this bit enables the daylight savings time mode. When set to 0, it disables the mode, and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt-request flag
6	Periodic-interrupt flag
5	Alarm-interrupt flag
4	Update-ended interrupt flag
3–0	Reserved

Figure 3-13. Status Register C (Hex 00C)

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 This bit is used in conjunction with bits 6, 5, and 4. When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When set to 1, this bit indicates that a periodic interrupt occurred.

Bit 5 When set to 1, this bit indicates that an alarm interrupt occurred.

Bit 4 When set to 1, this bit indicates that an update-ended interrupt occurred.

Bits 3–0 These bits are reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6–0	Reserved

Figure 3-14. Status Register D (Hex 00D)

Bit 7 This read-only bit monitors the power-sense pin. A low state of this pin indicates a loss of power to the real-time clock (dead battery). When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power.

Bits 6–0 These bits are reserved.

CMOS RAM Configuration

The following figure shows the bit definitions for the CMOS RAM Configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-time clock module power
6	Configuration record and checksum status
5	Incorrect configuration
4	Memory size miscompare
3	Fixed disk controller/drive C initialization status
2	Time-status indicator
1	Adapter-configuration miscompare
0	Adapter-ID time-out

Figure 3-15. Diagnostic Status Byte (Hex 00E)

Bit 7 When set to 1, this bit indicates the real-time clock lost power.

Bit 6 When this bit is set to 1, the checksum is incorrect.

Bit 5 This is a check, at power-on, of the Equipment byte. When set to 1, the configuration information is incorrect. Power-on checks require that at least one diskette drive be installed (bit 0 of the Equipment byte, hex 014, is set to 1).

Bit 4 When set to 1, this bit indicates the power-on check determined that the memory size is not the same as in the configuration record.

Bit 3 When set to 1, this bit indicates that the controller or drive C failed initialization, which prevents the system from attempting a power-on reset.

Bit 2 When set to 0, this bit indicates the time is valid. When set to 1, this bit indicates the time is invalid.

Bit 1 This bit indicates if the installed adapters match the configuration information. When this bit is set to 1, the adapters do not match the configuration information.

Bit 0 When set to 1, this bit indicates a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7–4	First diskette drive type
3–0	Second diskette drive type

Figure 3-16. Diskette Drive Type Byte (Hex 010)

Bits 7–4 These bits indicate the first diskette drive type, as shown in the following figure.

Bits 7 6 5 4	Function
0 0 0 0	No drive present
0 0 0 1	5.25-inch, 360KB diskette drive
0 0 1 0	5.25-inch, 1.2MB diskette drive
0 0 1 1	3.5-inch, 720KB diskette drive
0 1 0 0	3.5-inch, 1.44MB diskette drive
0 1 1 0	3.5-inch, 2.88MB diskette drive
Note: Combinations that are not shown are reserved.	

Figure 3-17. First Diskette Drive Type Byte (Bits 7–4)

Bits 3–0 These bits indicate the second diskette drive type, as shown in the following figure.

Bits 3 2 1 0	Function
0 0 0 0	No drive present
0 0 0 1	5.25-inch, 360KB diskette drive
0 0 1 0	5.25-inch, 1.2MB diskette drive
0 0 1 1	3.5-inch, 720KB diskette drive
0 1 0 0	3.5-inch, 1.44MB diskette drive
0 1 1 0	3.5-inch, 2.88MB diskette drive
Note: Combinations that are not shown are reserved.	

Figure 3-18. Second Diskette Drive Type Byte (Bits 3–0)

Reserved Byte (Hex 011): This byte is reserved.

Reserved Byte (Hex 012): This byte is reserved.

Reserved Byte (Hex 013): This byte is reserved.

Equipment Byte (Hex 014): The Equipment byte, for the power-on diagnostic tests, defines the basic equipment in the system.

Bit	Function
7, 6	Number of diskette drives
5, 4	Display operating mode
3, 2	Reserved
1	Math coprocessor presence
0	Diskette drive presence

Figure 3-19. Equipment Byte (Hex 014)

Bits 7, 6 These bits indicate the number of diskette drives installed, as shown in the following figure.

Bits 7 6	Number of Diskette Drives
0 0	One drive
0 1	Two drives
1 0	Three drives
1 1	Reserved

Figure 3-20. Equipment Byte (Bits 7, 6)

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port, as shown in the following figure.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-column mode
1 0	80-column mode
1 1	Monochrome mode

Figure 3-21. Equipment Byte (Bits 5, 4)

Bits 3, 2 These bits are reserved.

Bit 1 When set to 1, this bit indicates that a math coprocessor is installed.

Bit 0 When set to 1, this bit indicates that a diskette drive is installed.

Low and High Base-Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 indicates 640KB. The low byte is hex 015; the high byte is hex 016.

Low and High Expansion-Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The value from these bytes represents the number of 1KB blocks of expansion memory. For example, hex 0800 indicates 2048KB. The low byte is hex 017; the high byte is hex 018.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check (CRC) data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 033; the high byte is hex 032.

Reserved Byte (Hex 034): This byte is reserved.

Low and High Usable Memory Bytes (Hex 035 and 036): These bytes define the total amount of contiguous usable memory from 1MB to 16MB.

The hexadecimal values in these bytes represent the number of 1KB blocks of usable memory. For example, hex 0800 indicates 2048KB. The low byte is hex 035; the high byte is hex 036.

Date-Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 through 03F): These bytes are reserved.

Miscellaneous System Functions and Ports

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system watchdog time-out has occurred. The NMI stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts and the IRET instruction restores the interrupt flag to the state it was in before the interrupt. A system reset causes a reset of the NMI.

The NMI requests that are caused by channel checks and system board memory-parity errors are subject to mask control with the NMI mask bit in the RT/CMOS Address register. The Watchdog Timer and system channel time-out are not masked by this bit. (See "RT/CMOS Address Register and NMI Mask (Hex 0070)" on page 3-11). The power-on default of the NMI mask is 1 (NMI disabled). Prior to enabling the NMI after a power-on reset, the parity-check and channel-check state are initialized by the POST.

Warning: The operation following a write operation to hex 0070 must access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the read and write functions of this port are shown in the following figures.

Bit	Function
7	Reset timer 0 output latch (IRQ0)
6–4	Reserved
3	Enable channel check
2	Enable parity check
1	Enable speaker data
0	Timer 2 gate to speaker

Figure 3-22. System Control Port B (Hex 0061)—Write

Bit	Function
7	Memory parity check
6	Channel check
5	Timer 2 output
4	Toggles with each refresh request
3	Enable channel check
2	Enable parity check
1	Enable speaker data
0	Timer 2 gate to speaker

Figure 3-23. System Control Port B (Hex 0061)—Read

Bit 7 Setting this bit to 1 resets IRQ0. Reading this bit as a 1 indicates a memory parity check has occurred.

Bit 6 Reading this bit as a 1 indicates a channel check has occurred.

Bit 5 This bit indicates the condition of the timer/counter 2 'output' signal.

Bit 4 This bit toggles for each refresh request.

Bit 3 Setting this bit to 0 enables channel check. Setting this bit to 1 disables channel check and clears the channel-check latch.

Bit 2 Setting this bit to 0 enables system board memory parity check. This bit is set to 1 during a power-on reset. To clear the indication of a parity error, set this bit to 1 and then to 0.

Note: This does not clear the source of a parity error.

Bit 1 Setting this bit to 1 enables speaker data.

Bit 0 Setting this bit to 1 enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7–5	Reserved
4	Watchdog timer status
3	Security lock latch
2	Reserved (set to 0)
1	Alternate gate A20
0	Alternate hot reset

Figure 3-24. System Control Port A (Hex 0092)

Bits 7–5 These bits are reserved.

Bit 4 This read-only bit indicates the watchdog-timer status. When this bit is set to 1, a watchdog time-out has occurred. For more information about the watchdog timer, refer to System Timers in *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces.*

Bit 3 This bit provides the security lock for the secured area of RT/CMOS. Setting this bit to 1 electronically locks the 8-byte, power-on password. Once this bit is set by POST, it can only be cleared by turning the system off.

Bit 2 This bit is reserved.

Bit 1 This bit is ORed with bit 1 in the Keyboard Output port to enable the 'address 20' signal (A20). When both bits are set to 0, A20 is disabled and set to 0. This bit is set to 0 during POST. (See the Keyboard and Auxiliary Device Controller section in the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces.*)

Bit 0 This bit provides an alternate method of resetting the system microprocessor. This alternate method supports operating systems requiring faster operation than was provided on the IBM Personal Computer AT*. Resetting the system microprocessor is used to switch the microprocessor from the protected mode to the real address mode. The alternate reset takes 13.4 microseconds.

This bit is set to 0 either by a system reset or a write operation. When a write operation changes this bit from 0 to 1, the alternate reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is 0, POST assumes the system was just powered on. If the bit is 1, POST assumes a switch from the protected mode to the real mode has taken place.

* Trademark of the IBM Corporation.

Power-On Password

RT/CMOS RAM has 8 bytes reserved for the power-on password and its check character. The 8 bytes are initialized to hex 00. The microprocessor can only access these bytes during power-on self-test (POST). After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by any program. A power-on password can be from 1 to 7 characters.

During power-on password installation, the password (1 to 7 keyboard scan codes) is stored in the security space.

Power-on password installation is a function of a program contained on the Reference Diskette. Once the power-on password has been installed, the password can be changed only during the POST. If a power-on password is changed, or removed during POST, the password is not visible on the display.

The system-unit cover can be physically locked to prevent unauthorized access to the battery. This helps prevent unauthorized battery removal and loss of power-on password and configuration information.

For information about the keyboard password, see the Keyboard and Auxiliary Device Controller section in the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces.*

Selectable Boot Sequence

With selectable boot you can specify the order in which bootable devices are searched when looking for the boot startup record of an operating system. Diskette drives, fixed disk drives, and remote initial program load (RIPL) can be part of the search sequence. Changing the sequence for selectable boot affects the drive-letter assignment each time the system is booted (started).

You can select the boot sequence by using the Select startup sequence menu on the Reference Diskette, and selecting from a list of possible devices. After the sequence is selected, it is stored in nonvolatile RAM (NVRAM). When the system is booted, it searches for a device that contains a bootable record, using the specified sequence.

After the operating system is booted, the drive lettering is determined by the sequence and by which device contained the bootable source.

Note: Selectable boot affects adapters that use initialization programs. See the Setup section in the *IBM Personal System/2 Hardware Interface Technical Reference—Architectures* for more details.

Hardware Compatibility

The Model 95 XP 486 maintains many of the interfaces used by previous IBM PS/2 products. In most cases command and status organization of these interfaces is maintained.

The functional interfaces for the Model 95 XP 486 are compatible with the following interfaces:

- The Intel** 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller address/transfer counters, page registers, and status fields only. The Command and Request registers are not supported. The rotate and mask functions are not supported. The Mode register is partially supported.
- The NS16450 serial port.
- The Intel 8088, 8086, 80286, and 80386 microprocessors.
- The Intel 8272 diskette drive controller.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The keyboard interface at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.

** Intel is a trademark of Intel Corporation, and Motorola is a trademark of Motorola, Incorporated.

Error Codes

POST returns a message in the form of a multiple-character code to indicate the type of test that failed. Two formats are used for these error messages:

- A 12-character code for all errors related to SCSI devices:
  - The first four characters identify the device type.
  - The next eight characters identify specifics of the error.
- An 8-character error code for all errors *not* related to SCSI devices.

An information panel is used to display the first eight characters of an error message in case the system is operating without a video display. Only the code for the first error found during POST is displayed on the information panel; subsequent errors are indicated only on the video display (the information panel will continue to display the first error).

The 8-character error code consists of two 4-character elements: the major error code and the minor error code. The following figure gives the failure indicated with the associated error code.

Major Code	Minor Code	Description
0001		System bus error - system board or processor complex
	0100	Unexpected interrupt
	0200	Timer failure
	0300	Timer interrupt failure
	0400	Protected mode failure
	0500	Last keyboard command not accepted
	0600	Converting logic test
	0700	NMI test failed
	0800	Timer bus-test failed
	0900	Low-MB chip-select test failed
	10*xx*	System board memory parity error
	11*xx*	I/O channel check error
	1200	Watchdog timeout
	1300	Micro Channel bus timeout
	1400	Channel feature card ROM checksum error
	1500	ROM checksum error or DMA error
	1600	System board port read/write failure
	1800	System board parity or L2-cache error during previous power-on
	1900	Down-level diskette controller (2.88MB diskette drive not supported)
	2000	Microprocessor test error
	6000	System board ID not recognized
	6100	Dead battery
	6300	Clock not updating
	6400	Memory configuration error
	6500	Adapter ID mismatch
	6600	Adapter busy error
	6700	Clock not updating
	6900	Processor complex configuration error
	7000	ASCII setup conflict error
	7100	Rolling bit test failure on CMOS Shutdown Address byte
	7200	Rolling bit test failure on NVRAM Diagnostic byte
	7300	Bad CMOS/NVRAM checksum
	7400	Bad configuration
	7900	NVRAM error log full
0002		Memory errors
	0*xxx*	Memory error
	1*xxx*	Unrecoverable error in first 1MB
	2100	ROM to RAM remapping error
	25*xx*	Unsupported memory-type installed or memory pair mismatch
	3500	Stuck data line on memory module, processor complex, or system board

Figure 3-25 (Part 1 of 2). POST Error Messages

Major Code	Minor Code	Description
0003		Keyboard
	0100	Keyboard error
	0200	Keyboard locked
	0300	Keyboard to system board interface error
	0400	Keyboard clock high
	0500	No keyboard +5 V
0006		Diskette
	0100	Diskette drive or controller error
	0200	Diskette IPL boot record not valid
	0400	Nonmedia sense
0011	0100	Async chip error
0017		Fixed disk error
	8000	Fixed disk 0 failed
	8100	Fixed disk 1 failed
	8200	Disk controller error
	9000	Fixed disk 0 error
	9100	Fixed disk 1 error
0024	0100	System board video error
0086		Mouse
	0100	System bus error - keyboard/pointing device interface
	0200	Pointing device error
	0300	Pointing device or system bus error
0096	*xxxx*	SCSI adapter (with cache) failure
0112	*xxxx*	SCSI adapter (without cache) failure
0129		Processor complex
	005*x*	DMA error
	0x00	Cache error
	12*xx*	Hardware failure
	13*xx*	Micro Channel bus timeout
	14*xx*	Software failure
	15*xx*	Processor complex error
	16*xx*	Processor complex error
	17*xx*	Processor complex error
	18*xx*	Processor complex error
	19*xx*	Processor complex error
	40*xx*	Processor complex failure
	50*xx*	Processor complex failure
	9000	Processor complex serial-number mismatch
0208 to 0241	*xxxx*	SCSI device test failure
1999		Special instruction codes
	00*xx*	Initial microcode load (IML) error
	03*xx*	No bootable device
	04*xx*	IML to system mismatch
	06*xx*	IML error

Figure 3-25 (Part 2 of 2). POST Error Messages

Section 4. Type 1 Processor Complexes

| Description 4-3
| Type 1A 4-4
| Type 1B 4-7
| Type 1C 4-10
| Type 1D 4-13
Type 1 Processor Complexes—I/O Address Map 4-15
| Type 1 Processor Complexes—Level 2 Cache 4-15
Type 1 Processor Complexes—Memory Subsystem 4-15
| Type 1 Processor Complexes—Memory Presence Detect . . . 4-16
| Type 1 Processor Complexes—Cache Address Map 4-17
Type 1 Processor Complexes—Read-Only Memory Subsystem 4-19

© Copyright IBM Corp. 1990, 1992

Notes:

Description

The processor complex provides certain devices and features that work in conjunction with devices and features provided by the system board. In addition, the processor complex determines system performance and certain channel timings. This section describes those aspects of the processor complex.

Type 1 has four different processor complexes. The major difference between each processor complex is speed. Programs can identify the type by reading the model and submodel bytes. Interrupt 15H, Return System Configuration Parameters function ((AH) = C0H), returns the model byte, submodel byte, BIOS revision code, and other configuration information. The following figure shows the model bytes, submodel bytes, and speed of the processor complexes.

Model Byte	Submodel Byte	Speed	Processor Complex
F8	14	25 MHz	Type 1A
F8	16	33 MHz	Type 1B
F8	2C	20 MHz	Type 1C (see note)
F8	2E	20 MHz	Type 1C with 487 SX math coprocessor (see note)
F8	2A	50 MHz	Type 1D

Note: The type 1C processor complex features the Intel486** SX microprocessor and supports the Intel487** SX math coprocessor. When the 487 SX math coprocessor is used, a jumper must be moved to adjust for pinout differences. See "Type 1C Jumper" on page 4-10 for jumper information.

Figure 4-1. Type 1 Processor Complexes—Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems.

** Intel486 and Intel487 are trademarks of Intel Corporation.

Type 1A

The following figure shows the devices and features for the type 1A processor complex.

Device	Type	Features
Microprocessor	---	80486DX—25 MHz, 32-bit address and 32-bit data interface
Cache	---	8KB, 4-way, write-through, internal cache, optional 256 KB L2 cache interface
ROM Subsystem	---	128KB physical ROM
RAM Subsystem	---	Eight-connector support, 2MB to 64MB interleaved, parity expandable on the system board only
DMA Controller	1	Eight independent DMA channels, single or burst transfers and read verification
Math Coprocessor	---	Math coprocessor functions included in 80486DX

Figure 4-2. Type 1A Processor Complex—Features and Devices

The following figure shows the performance and other timing information for the type 1A processor complex. These timings affect the channel performance for operations involving the processor complex or system board memory.

Note: All of the timings in Figure 4-3, and Figure 4-4 on page 4-6 are typical values. Timings can vary depending on microprocessor workload, bus master workload, and cycle mix.

Device	Cycle Time (ns)
Microprocessor (25 MHz—40 ns Clock)	
Access to channel	
Default transfer cycle	240
Extended transfer cycle	320
Refresh Rate	
(Typically performed every 15.1 μs)	500 (min)
DMA Controller (10 MHz—100 ns Clock)	
Single transfer: 300 + I/O access + memory access	
Burst transfers: 300 + (I/O access + memory access)*n*†	
System board memory access	300
Default transfer cycle	200
Synchronous extended transfer cycle	300
† *n* is the number of transfers in the burst transfer.	

Figure 4-3. Type 1A Processor Complex—System Performance Specifications

Device	Cycle Time (ns) per Memory Type		
	70 ns	80 ns	85 ns
Microprocessor (25 MHz—40 ns Clock)			
Memory read (cache hit)	40	40	40
Memory read (cache miss, page hit, burst)	320	320	400
Memory read (cache miss, page miss, burst)	440	480	560
Memory write (page hit)	160	160	200
Memory write (page miss)	280	320	360
Microprocessor—with Optional L2 Cache			
Memory read (cache hit, optional cache hit)	40	40	40
Memory read (cache miss, optional cache hit, burst)	200	200	200
Memory read (cache miss, optional cache miss, page hit, burst)	320	320	400
Memory read (cache miss, optional cache miss, page miss, burst)	440	480	560
Memory write (page hit)	160	160	200
Memory write (page miss)	280	320	360
Bus Master Access to System Board RAM			
Page hit (typical†)	440	440	440
Page miss (typical†)	580	580	580

† Variations exist because of differences in timings of masters and system master accesses to system board memory that are interleaved with master accesses.

Figure 4-4. Type 1A Processor Complex—Memory Performance Specifications

Type 1B

The following figure shows the devices and features for the type 1B processor complex.

Device	Type	Features
Microprocessor	---	80486DX—33 MHz, 32-bit address and 32-bit data interface
Cache	---	8KB, 4-way, write-through, internal cache, optional 256KB L2 cache interface
ROM Subsystem	---	128KB physical ROM
RAM Subsystem	---	Eight-connector support, 2MB to 64MB interleaved, parity expandable on the system board only
DMA Controller	1	Eight independent DMA channels, single or burst transfers and read verification
Math Coprocessor	---	Math coprocessor functions included in 80486DX

Figure 4-5. Type 1B Processor Complex—Features and Devices

The following figure shows the performance and other timing information for the type 1B processor complex. These timings affect the channel performance for operations involving the processor complex or system board memory.

Note: All of the timings in Figure 4-6 and in Figure 4-7 on page 4-9 are typical values. Timings can vary depending on microprocessor workload, bus master workload, and cycle mix.

Device	Cycle Time (ns)
Microprocessor (33 MHz—30 ns Clock)	
Access to channel	
Default transfer cycle	240
Extended transfer cycle	320
Refresh Rate	
(Typically performed every 15.1 μs)	500 (min)
DMA Controller (10 MHz—100 ns Clock)	
Single transfer: 300 + I/O access + memory access	
Burst Transfers: 300 + (I/O access + memory access)*n*†	
System board memory access	300
Default transfer cycle	200
Synchronous extended transfer cycle	300
† *n* is the number of transfers in the burst transfer.	

Figure 4-6. Type 1B Processor Complex—System Performance Specifications

Device	Cycle Time (ns) per Memory Type		
	70 ns	80 ns	85 ns
Microprocessor (33 MHz—30 ns Clock)			
Memory read (cache hit)	30	30	30
Memory read (cache miss, page hit, burst)	240	300	300
Memory read (cache miss, page miss, burst)	360	420	420
Memory write (page hit)	120	150	150
Memory write (page miss)	240	270	270
Microprocessor—with Optional L2 Cache			
Memory read (cache hit, optional cache hit)	30	30	30
Memory read (cache miss, optional cache hit, burst)	150	150	150
Memory read (cache miss, optional cache miss, page hit, burst)	240	300	300
Memory read (cache miss, optional cache miss, page miss, burst)	360	420	420
Memory write (page hit)	120	150	150
Memory write (page miss)	240	270	270
Bus Master Access to System Board RAM			
Page hit (typical†)	400	400	400
Page miss (typical†)	550	550	550

† Variations exist because of differences in timings of masters and system master accesses to system board memory that are interleaved with master accesses.

Figure 4-7. Type 1B Processor Complex—Memory Performance Specifications

Type 1C

The following figure shows the devices and features for the type 1C processor complex.

Device	Type	Features
Microprocessor	—	80486SX—20 MHz, 32-bit address and 32-bit data interface
Cache	—	8KB, 4-way, write-through, internal cache only
ROM Subsystem	—	128KB physical ROM
RAM Subsystem	—	Eight-connector support, 2MB to 64MB interleaved, parity expandable on the system board only
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Math Coprocessor	—	Optional using the 487 SX math coprocessor

Figure 4-8. Type 1C Processor Complex—Features and Devices

Type 1C Jumper: A jumper is moved to adjust for the pinout differences between the 486 SX microprocessor and the 487 SX math coprocessor. The jumper is located next to the microprocessor socket. For the 486 SX microprocessor, the jumper is connected across pins 2 and 3. For the 487 SX math coprocessor, the jumper is connected across pins 1 and 2.

The following figure shows the performance and other timing information for the type 1C processor complex. These timings affect the channel performance for operations involving the processor complex or system board memory.

Note: All of the timings in Figure 4-9 and in Figure 4-10 on page 4-12 are typical values. Timings can vary depending on microprocessor workload, bus master workload, and cycle mix.

Device	Cycle Time (ns)
Microprocessor (20 MHz—50 ns Clock)	
Access to channel	
Default transfer cycle	250
Extended transfer cycle	350
Refresh Rate	
(Typically performed every 15.1 μs)	600 (min)
DMA Controller (10 MHz—100 ns Clock)	
Single transfer: 300 + I/O access + memory access	
Burst transfers: 300 + (I/O access + memory access)*n*†	
System board memory access	400
Default transfer cycle	200
Synchronous extended transfer cycle	300

† *n* is the number of transfers in the burst transfer.

Figure 4-9. Type 1C Processor Complex—System Performance Specifications

Device	Cycle Time (ns) per Memory Type		
	70 ns	80 ns	85 ns
Microprocessor (20 MHz—50 ns Clock)			
Memory read (cache hit)	50	50	50
Memory read (cache miss, page hit, burst)	350	350	350
Memory read (cache miss, page miss, burst)	500	500	500
Memory write (page hit)	150	150	150
Memory write (page miss)	300	300	300
Bus Master Access to System Board RAM			
Page hit (typical†)	350	350	350
Page miss (typical†)	500	500	500
† Variations exist because of differences in timings of masters and system master accesses to system board memory that are interleaved with master accesses.			

Figure 4-10. Type 1C Processor Complex—Memory Performance Specifications

Type 1D

The following figure shows the devices and features for the type 1D processor complex.

Device	Type	Features
Microprocessor	—	80486DX—50 MHz, 32-bit address and 32-bit data interface
Cache	—	8KB, 4-way, write-through, internal cache, 256KB L2 cache
ROM Subsystem	—	128KB physical ROM
RAM Subsystem	—	Eight-connector support, 2MB to 64MB interleaved, parity expandable on the system board only
DMA Controller	1	Eight independent DMA channels, single or burst transfers and read verification
Math Coprocessor	—	Math coprocessor functions included in 80486DX

Figure 4-11. Type 1D Processor Complex—Features and Devices

The following figure shows the performance and other timing information for the type 1D processor complex. These timings affect the channel performance for operations involving the processor complex or system board memory.

Note: All of the timings in Figure 4-12 on page 4-14 and in Figure 4-13 on page 4-14 are typical values. Timings can vary depending on microprocessor workload, bus master workload, and cycle mix.

Device	Cycle Time (ns)
Microprocessor (50 MHz—20 ns Clock)	
Access to channel	
Default transfer cycle	240
Extended transfer cycle	320
Refresh Rate	
(Typically performed every 15.1 μs)	500 (min)
DMA Controller (10 MHz—100 ns Clock)	
Single transfer: 300 + I/O access + memory access	
Burst transfers: 300 + (I/O access + memory access)*n*†	
System board memory access	300
Default transfer cycle	200
Synchronous extended transfer cycle	300
† *n* is the number of transfers in the burst transfer.	

Figure 4-12. Type 1D Processor Complex—System Performance Specifications

Device	Cycle Time (ns) per Memory Type		
	70 ns	80 ns	85 ns
Microprocessor (50 MHz—20 ns Clock with L2 Cache)			
Memory read (cache hit, L2 cache hit)	20	20	20
Memory read (cache miss, L2 cache hit, burst)	100	100	100
Memory read (cache miss, L2 cache miss, page hit, burst)	360	360	440
Memory read (cache miss, L2 cache miss, page miss, burst)	480	520	600
Memory write (page hit)	200	200	240
Memory write (page miss)	320	360	400
Bus Master Access to System Board RAM			
Page hit (typical†)	300	300	300
Page miss (typical†)	300	300	300
† Variations exist because of differences in timings of masters and system master accesses to system board memory that are interleaved with master accesses.			

Figure 4-13. Type 1D Processor Complex—Memory Performance Specifications

Type 1 Processor Complexes—I/O Address Map

The following shows the I/O address for devices located on the processor complex.

Hex Addresses	Device
0000–001F	DMA controller (0–3)
0081–0083, 0087	DMA Page registers (0–3)
0089–008B, 008F	DMA Page registers (4–7)
0090	Central arbitration control point
00C0–00DF	DMA controller (4–7)

Figure 4-14. Type 1 Processor Complexes—I/O Address Map

Type 1 Processor Complexes—Level 2 Cache

The type 1A and type 1B processor complexes have a 160-pin connector for an optional 256KB cache (L2 cache). The optional cache provides a secondary cache and cache controller for the system microprocessor. The type 1C processor complex does not support an optional cache. The type 1D processor complex has a standard 256KB L2 cache.

The L2 cache on type 1A, type 1B, and type 1D processor complexes provides the system microprocessor with an additional 256KB cache. It operates as 2-way set-associative, write-through cache with parity. The primary cache in both the 80486DX and 80486DX2 must be enabled to operate the secondary cache.

Type 1 Processor Complexes—Memory Subsystem

Memory on the system board is parity-checked, interleaved, random-access memory and must be installed in matched pairs: one in an A connector and one in the matching B connector (for memory connector information, see "System Board Memory Connectors" on page 3-8). The memory in each pair must be the same speed and size. System memory on adapters in the channel is not mapped into the cacheable address space of the system microprocessor.

System board memory is designed so that the system microprocessor can access memory while a bus master has control of the channel.

The memory controller manages this dual access by interleaving the microprocessor and bus master accesses. In addition, system board memory is organized into pairs of banks so that the microprocessor can perform burst cycles with two-way interleaved accesses. Because of this organization, the microprocessor can perform zero-wait-state transfers for every other 32-bit transfer in the burst cycle.

Type 1 Processor Complexes—Memory Presence Detect

The presence-detect signals are used by the system to determine the size and speed of memory on the single inline memory module (also called *memory module*). The pins are either not connected (1) or connected to ground (0).

A set of 4 bits shows the state of all presence-detect signals for a specific memory connector; the bit is 0 when the signal is connected to ground. The following figure shows the information indicated by these bits, as well as the bank size of the memory module. Combinations that are not shown are reserved.

Presence Detect 3 2 1 0	Single Inline Memory Module Definition	Bank Size	Type
1 0 1 1	8MB 70-ns memory	4MB	Parity
1 0 0 0	8MB 80-ns memory	4MB	Parity
0 1 0 0	4MB 70-ns memory	4MB	Parity
0 0 0 0	4MB 80-ns memory	4MB	Parity
1 1 0 0	2MB 70-ns memory	1MB	Parity
1 0 0 1	2MB 80-ns memory	1MB	Parity
0 1 0 1	2MB 85-ns memory	1MB	Parity
0 1 1 0	1MB 85-ns memory	1MB	Parity
1 1 1 1	Connector is empty		

Figure 4-15. Type 1 Processor Complexes—Presence-Detect Bits

Type 1 Processor Complexes—Cache Address Map

The following map is a summary of those addresses within the memory address space that can be cached. Only system board memory is mapped into the microprocessor level 1 cache and level 2 cache. The level 2 (L2) cache is optional for type 1A and type 1B processor complexes. The type 1C processor complex does not support an optional cache. The type 1D processor complex has a standard 256KB L2 cache.

The system memory address space contains three cacheable regions:

- Region 1—Memory addresses from 0 up to 1MB
- Region 2—Memory addresses from 1MB up to 16MB
- Region 3—Memory addresses from 16MB up to 64MB.

All system board memory in region 2 and region 3 is cacheable. Programmable boundary registers for region 2 and region 3 control the upper boundaries of the memory space to be cached. The Set Configuration utility assigns memory to these cached regions, depending on the system configuration. POST establishes these cached regions, and they must not be altered.

Nonsystem memory can be located as follows:

- Region 1—In the area between memory addresses 0C0000 and 0DFFFF
- Region 2—Memory addresses from 16MB down to system memory
- Region 3—Memory addresses from 4GB (minus 1MB) down to system memory.

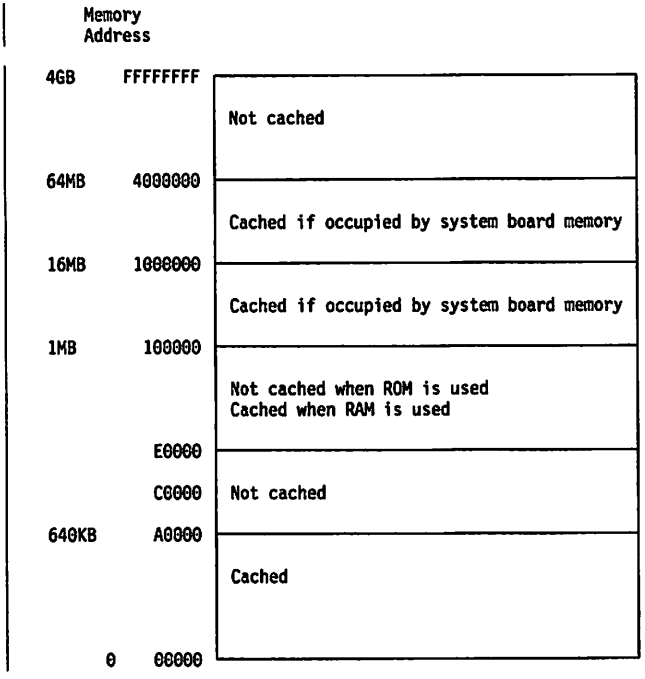


Figure 4-16. Type 1 Processor Complexes—Cache Address Map Summary

Type 1 Processor Complexes—Read-Only Memory Subsystem

The ROM subsystem is located on the processor complex and consists of 128KB in a 128K by 8-bit arrangement. The ROM is active at power-on at memory address space hex 000E0000 to 000FFFFF. The ROM contains the code that initializes the system to load and execute POST and BIOS code from a DASD device. ROM is also assigned at the top of the 4GB memory address space from hex FFFE0000 to FFFFFFFF.

Notes:

Section 5. Type 2 Processor Complexes

| Description 5-3
| Type 2A 5-4
| Type 2B 5-7
Type 2 Processor Complexes—I/O Address Map 5-10
| Type 2 Processor Complexes—Level 2 Cache 5-10
| Type 2 Processor Complexes—Memory Subsystem 5-10
| Type 2 Processor Complexes—Memory Presence Detect . . . 5-11
| Type 2 Processor Complexes—Cache Address Map 5-12
Type 2 Processor Complexes—Read-Only Memory Subsystem 5-14

© Copyright IBM Corp. 1990, 1992

Notes:

Description

The processor complex provides certain devices and features that work in conjunction with devices and features provided by the system board. In addition, the processor complex determines system performance and certain channel timings. This section describes those aspects of the processor complex.

Type 2 has two different processor complexes. The major difference between each processor complex is speed. Programs can identify the processor complex by reading the model and submodel bytes. Interrupt 15H, Return System Configuration Parameters function ((AH)=C0H), returns the model byte, submodel byte, BIOS revision code, and other configuration information. The following figure shows the model bytes, submodel bytes, and speed of the processor complexes.

Model Byte	Submodel Byte	Speed	Processor Complex
F8	58	25 MHz	Type 2A
F8	5A	25 MHz	Type 2A with 487SX math coprocessor
F8	5C	50 MHz	Type 2A with 486DX2 module plugged on the type 2A processor complex†
F8	40	50 MHz	Type 2B

† For performance information, see Figure 5-6 on page 5-8 and Figure 5-7 on page 5-9.

Figure 5-1. Type 2 Processor Complexes—Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems.

Type 2A

The following figure shows the devices and features for the type 2A processor complex.

Device	Type	Features
Microprocessor	---	80486SX—25 MHz, 32-bit address and 32-bit data interface
Cache	---	8KB, 4-way, write-through, internal cache
ROM Subsystem	---	128KB physical ROM
RAM Subsystem	---	Eight-connector support, 2MB to 64MB interleaved or noninterleaved, parity expandable on the system board only
DMA Controller	1	Eight independent DMA channels, single or burst transfers and read verification
Math Coprocessor	---	80487SX math coprocessor socket

Figure 5-2. Type 2A Processor Complex—Features and Devices

The following figure shows the performance and other timing information for the type 2A processor complex. These timings affect the channel performance for operations involving the processor complex or system board memory.

Device	Cycle Time (ns)
Microprocessor (25 MHz—40 ns Clock)	
Access to channel	
Default transfer cycle	320
Extended transfer cycle	440
Refresh Rate	
(Typically performed every 15.1 μs)	320 (min)
DMA Controller (25 MHz—40 ns Clock)	
Single transfer: 300 + I/O access + memory access	
Burst transfers: 300 + (I/O access + memory access)*n*†	
Memory access	
Page hit read	160
Page miss read	280
Page hit write	120
Page miss write	240
I/O access	
Default transfer cycle	320
Synchronous extended transfer cycle	440

† *n* is the number of transfers in the burst transfer.

Figure 5-3. Type 2A Processor Complex—System Performance Specifications

Device	Cycle Time (ns) per Memory Type		
	70 ns	80 ns	85 ns
Microprocessor (25 MHz—40 ns Clock)			
Memory read (cache hit)	40	40	NA
Memory read (cache miss, page hit, burst)	280	280	NA
Memory read (cache miss, page miss, burst)	400	400	NA
Memory write (page hit)	120	120	NA
Memory write (page miss)	240	240	NA
Bus Master Access to System Board RAM			
Always page miss (minimum)	300	300	NA
Note: NA means not applicable.			

Figure 5-4. Type 2A Processor Complex—Memory Performance Specifications

Type 2B

The following figure shows the devices and features for the type 2B processor complex.

Device	Type	Features
Microprocessor	---	80486DX2—50 MHz, 32-bit address and 32-bit data interface
Cache	---	8KB, 4-way, write-through, internal cache
ROM Subsystem	---	128KB physical ROM
RAM Subsystem	---	Eight-connector support, 2MB to 64MB interleaved or noninterleaved, expandable on the system board only
DMA Controller	1	Eight independent DMA channels, single or burst transfers and read verification
Math Coprocessor	---	Math coprocessor functions included in 80486DX2

Figure 5-5. Type 2B Processor Complex—Features and Devices

The following figure shows the performance and other timing information for the type 2B processor complex. These timings affect the channel performance for operations involving the processor complex or system board memory.

Device	Cycle Time (ns)
Microprocessor (50 MHz—40 ns Clock)	
Access to channel	
Default transfer cycle	320
Extended transfer cycle	440
Refresh Rate	
(Typically performed every 15.1 μs)	320 (min)
DMA Controller (25 MHz—40 ns Clock)	
Single transfer: 300 + I/O access + memory access	
Burst transfers: 300 + (I/O access + memory access)*n*†	
Memory access	
Page hit read	160
Page miss read	280
Page hit write	120
Page miss write	240
I/O access	
Default transfer cycle	320
Synchronous extended transfer cycle	440

† *n* is the number of transfers in the burst transfer.

Figure 5-6. Type 2B Processor Complex—System Performance Specifications

Device	Cycle Time (ns) per Memory Type		
	70 ns	80 ns	85 ns
Microprocessor (50 MHz—40 ns Clock)			
Memory read (cache hit)	20	20	NA
Memory read (cache miss, page hit, burst)	280	280	NA
Memory read (cache miss, page miss, burst)	400	400	NA
Memory write (page hit)	120	120	NA
Memory write (page miss)	240	240	NA
Bus Master Access to System Board RAM			
Always page miss (minimum)	300	300	NA

Note: NA means not applicable.

Figure 5-7. Type 2B Processor Complex—Memory Performance Specifications

Type 2 Processor Complexes—I/O Address Map

The following shows the I/O address for devices located on the processor complex.

Hex Addresses	Device
0000–001F	DMA controller (0–3)
0081–0083, 0087	DMA Page registers (0–3)
0089–008B, 008F	DMA Page registers (4–7)
0090	Central arbitration control point
00C0–00DF	DMA controller (4–7)

Figure 5-8. Type 2 Processor Complexes—I/O Address Map

Type 2 Processor Complexes—Level 2 Cache

The type 2A and type 2B processor complexes do not support a level 2 (L2) cache.

Type 2 Processor Complexes—Memory Subsystem

Memory on the system board is parity-checked, random-access memory that can be interleaved or noninterleaved. To operate in interleaved mode, the memory must be in both A connectors and B connectors (for memory connector information, see "System Board Memory Connectors" on page 3-8). The processor complex will automatically interleave memory between the A and B connectors (even and odd banks). If more memory is installed in either bank, then that difference will be used as noninterleaved memory. For example, if 2MB are installed in an A connector (even bank) and 4MB are installed in B connectors (odd bank), then the 2MB in the even bank will be interleaved with 2MB of the 4MB in the odd bank. The remaining 2MB in the odd bank will be noninterleaved. When operating in interleaved mode, the microprocessor can perform burst cycles with two-way interleaved accesses. This allows the microprocessor to perform zero-wait-state transfers for alternating 32-bit transfers in the burst cycle.

The type 2A and type 2B processor complexes do not support system microprocessor and bus master interleaving of system memory accesses.

Type 2 Processor Complexes—Memory Presence Detect

The presence-detect signals are used by the system to determine the size and speed of memory on the single inline memory module (also called *memory module*). The pins are either not connected (1) or connected to ground (0).

A set of 4 bits shows the state of all presence-detect signals for a specific memory connector; the bit is 0 when the signal is connected to ground. The following figure shows the information indicated by these bits, as well as the bank size of the memory module. Combinations that are not shown are reserved.

Presence Detect 3 2 1 0	Single Inline Memory Module Definition	Bank Size	Type
1 0 1 1	8MB 70-ns memory	4MB	Parity
1 0 0 0	8MB 80-ns memory	4MB	Parity
0 1 0 0	4MB 70-ns memory	4MB	Parity
0 0 0 0	4MB 80-ns memory	4MB	Parity
1 1 0 0	2MB 70-ns memory	1MB	Parity
1 0 0 1	2MB 80-ns memory	1MB	Parity
1 1 1 1	Connector is empty		

Figure 5-9. Type 2 Processor Complexes—Presence-Detect Bits

Type 2 Processor Complexes—Cache Address Map

The following map is a summary of those addresses within the memory address space that can be cached. Only system board memory is mapped into the microprocessor level 1 cache and level 2 cache. The type 2A and type 2B processor complexes do not support a level 2 cache.

The system memory address space contains three cacheable regions:

- Region 1—Memory addresses from 0 up to 1MB
- Region 2—Memory addresses from 1MB up to 16MB
- Region 3—Memory addresses from 16MB up to 64MB.

All system board memory in region 2 and region 3 is cacheable. Programmable boundary registers for region 2 and region 3 control the upper boundaries of the memory space to be cached. The Set Configuration utility assigns memory to these cached regions, depending on the system configuration. POST establishes these cached regions, and they must not be altered.

Nonsystem memory can be located as follows:

- Region 1—In the area between memory addresses 0C0000 and 0DFFFF
- Region 2—Memory addresses from 16MB down to system memory
- Region 3—Memory addresses from 4GB down to 2GB system memory.

Note: If you have a type 2 processor complex, and have nonsystem memory located between 16MB and 2GB, the system will disable the processor cache during POST. If nonsystem memory is used in the 16MB to 2GB range, performance is reduced.

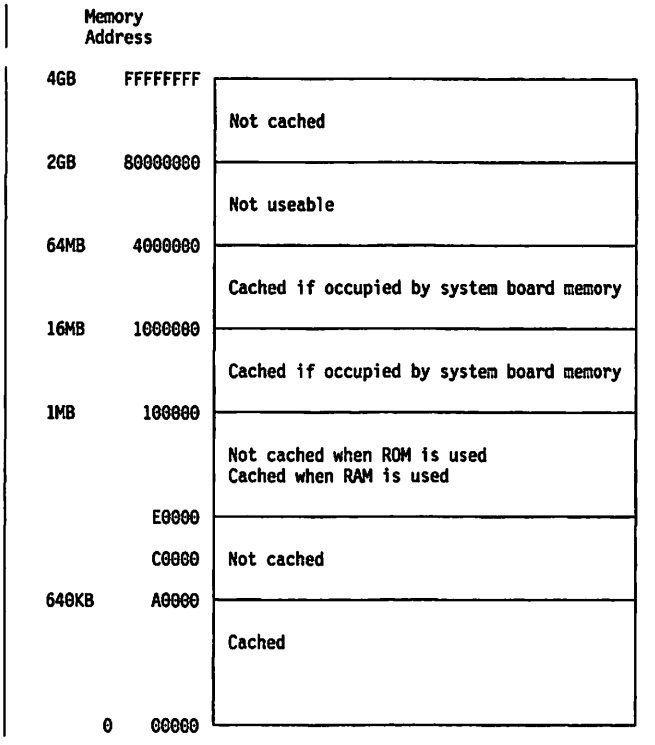


Figure 5-10. Type 2 Processor Complexes—Cache Address Map Summary

Type 2 Processor Complexes—Read-Only Memory Subsystem

The ROM subsystem is located on the processor complex and consists of 128KB in a 128K by 8-bit arrangement. The ROM is active at power-on at memory address space hex 000E0000 to 000FFFFF. The ROM contains the code that initializes the system to load and execute POST and BIOS code from a DASD device. ROM is also assigned at the top of the 4GB memory address space from hex FFFE0000 to FFFFFFFF.

Section 6. Type 3 Processor Complexes

Description 6-3
Type 3A 6-4
Type 3 Processor Complexes—I/O Address Map 6-7
Type 3 Processor Complexes—Level 2 Cache 6-7
Type 3 Processor Complexes—Memory Subsystem 6-8
Type 3 Processor Complexes—Memory Presence Detect 6-9
Type 3 Processor Complexes—Cache Address Map 6-10
Type 3 Processor Complexes—Read-Only Memory Subsystem 6-12

© Copyright IBM Corp. 1990, 1992

Notes:

Description

The processor complex provides certain devices and features that work in conjunction with devices and features provided by the system board. In addition, the processor complex determines system performance and certain channel timings. This section describes those aspects of the processor complex.

Type 3 has one processor complex. Programs can identify the processor complex by reading the model and submodel bytes. Interrupt 15H, Return System Configuration Parameters function ((AH)=C0H), returns the model byte, submodel byte, BIOS revision code, and other configuration information. The following figure shows the model byte, submodel byte, and speed of the processor complex.

Model Byte	Submodel Byte	Speed	Processor Complex
F8	28	50 MHz	Type 3A

Figure 6-1. Type 3 Processor Complexes—Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems.

Type 3A

The following figure shows the devices and features for the type 3A processor complex.

Device	Type	Features
Microprocessor	—	80486DX—50 MHz, 32-bit address and 32-bit data interface
Cache	—	8KB, 4-way, write-through, internal cache, 256KB external L2 cache
ROM Subsystem	—	128KB physical ROM
RAM Subsystem	—	Eight-connector support, 2MB to 64MB interleaved, parity/ECC expandable on the system board only
DMA Controller	2	Eight independent DMA channels, 32-bit DMA single or burst transfers and read verification
Math Coprocessor	—	Math coprocessor functions included in 80486DX

Figure 6-2. Type 3A Processor Complex—Features and Devices

The following figure shows the performance and other timing information for the type 3A processor complex. These timings affect the channel performance for operations involving the processor complex or system board memory.

Note: All of the timings in Figure 6-3, Figure 6-4 on page 6-6, and Figure 6-5 on page 6-7 are typical values. Timings can vary depending on microprocessor workload, cycle mix, bus master workload, and asynchronous clocks.

Device	Cycle Time (ns)
Microprocessor (50 MHz—20 ns Clock)	
I/O access	
Default transfer cycle	430
Extended transfer cycle	505
Refresh Rate (Typically performed every 15.1 μs)	500 (min)
DMA Controller (20 MHz—50 ns Clock)	
Accesses to system board memory: 70 ns/80 ns/85 ns (Parity/ECC)	
Single transfer read	
Page hit	325
Page miss	225
Burst transfer read	
Page hit	475 (16 bytes)
Page miss	575 (16 bytes)
Single transfer write	
Page hit	200
Page miss	300
Single transfer write (partial)	
Page hit	375
Page miss	475
Burst transfer write	
Page hit	475 (16 bytes)
Page miss	575 (16 bytes)
Accesses to Micro Channel	
Default cycle	300
Extended cycle	375

Note: A transfer can be a byte (8 bits), word (16 bits), or doubleword (32 bits).

Figure 6-3. Type 3A Processor Complex—System Performance Specifications

Device	Cycle Time (ns) Parity			Cycle Time (ns) ECC
	70 ns	80 ns	85 ns	70 ns
Microprocessor (50 MHz—20 ns Clock with L2 Cache)				
Memory read (cache hit)				
Burst†	100	100	100	100
Non-burst	40	40	40	40
Memory read (cache miss, page hit)				
Burst†	440	465	465	440
Non-burst	280	305	305	280
Memory read (cache miss, page miss)				
Burst†	540	565	565	540
Non-burst	380	405	405	380
Memory write (partial write, cache hit)				
Posted/non-posted	100	100	100	100
Page hit	155	180	180	155
Page miss	255	280	280	255
Memory write (partial write, cache miss)				
Posted/non-posted	100	100	100	100
Page hit	330	355	355	330
Page miss	430	455	455	430
Memory write (full write, cache hit/miss)				
Posted/non-posted	60	60	60	60
Page hit	155	180	180	155
Page miss	255	280	280	255

† Burst refers to 16 bytes.

Figure 6-4. Type 3A Processor Complex—Memory Performance Specifications

Device	Cycle Time (ns)
Channel Bus Master	
Basic transfer	
Single transfer read	500
First transfer of block read	500
Subsequent transfer of block reads	200
Single transfer write	200
First transfer of block write	200
Subsequent transfer of block writes	200
Streaming data transfer	
First access read	500
Subsequent access read	40 Mbps (max)
Write	40 Mbps (max)
Note: A transfer can be a byte (8 bits), word (16 bits), or doubleword (32 bits).	

Figure 6-5. Type 3A Processor Complex—Channel Bus Master Performance Specifications

Type 3 Processor Complexes—I/O Address Map

The following shows the I/O address for devices located on the processor complex.

Hex Addresses	Device
0000–001F	DMA controller (0–3)
0081–0083, 0087	DMA Page registers (0–3)
0089–008B, 008F	DMA Page registers (4–7)
0090	Central arbitration control point
00C0–00DF	DMA controller (4–7)

Figure 6-6. Type 3 Processor Complexes—I/O Address Map

Type 3 Processor Complexes—Level 2 Cache

The level 2 (L2) cache provides the system microprocessor with an additional 256KB cache. It operates as 2-way set-associative, write-through cache with parity. The primary cache in the 80486DX must be enabled to operate the secondary cache.

Type 3 Processor Complexes—Memory Subsystem

Memory on the system board is ECC or parity-checked, interleaved random-access memory and must be installed in matched pairs: one in an A connector and one in the matching B connector (for memory connector information, see "System Board Memory Connectors" on page 3-8). The memory in each pair must be the same speed and size. All memory must be of the same type, either all ECC or all parity checked. System memory on adapters in the channel is not supported.

System board memory is designed so that the system microprocessor can access memory while a bus master has control of the channel. The memory controller manages this dual access by interleaving the microprocessor and bus master accesses. In addition, system board memory is organized into pairs of banks so that the microprocessor can perform burst cycles with two-way interleaved accesses.

Type 3 Processor Complexes—Memory Presence Detect

The presence-detect signals are used by the system to determine the size and speed of memory on the single inline memory module (also called *memory module*). The pins are either not connected (1) or connected to ground (0).

A set of 4 bits shows the state of all presence-detect signals for a specific memory connector; the bit is 0 when the signal is connected to ground. The following figure shows the information indicated by these bits, as well as the bank size of the memory module. Combinations that are not shown are reserved.

The presence-detect information indicates the speed, size, and organization of a memory module. The type information, indicating either ECC or parity error detection of each memory module, also must be used to determine the type of memory module installed.

Note: Some of the presence-detect bits are the same. They are differentiated by the type of memory (parity or ECC). You must first read the System Board POS Register 3 to determine the type, then the presence-detect bits.

See "System Board POS Register 3 (Hex 0103)" on page 2-7, Figure 2-6 on page 2-8, and Figure 2-8 on page 2-8 for more information.

Presence Detect 3 2 1 0	Single Inline Memory Module Definition	Bank Size	Type
1 0 1 1	8MB 70-ns memory	4MB	ECC
1 0 1 1	8MB 70-ns memory	4MB	Parity
1 0 0 1	4MB 70-ns memory	4MB	ECC
0 1 0 0	4MB 70-ns memory	4MB	Parity
0 0 0 0	4MB 80-ns memory	4MB	Parity
1 1 0 0	2MB 70-ns memory	1MB	Parity
1 0 0 1	2MB 80-ns memory	1MB	Parity
0 1 0 1	2MB 85-ns memory	1MB	Parity
0 1 1 0	1MB 85-ns memory	1MB	Parity
1 1 1 1	Connector is empty		

Figure 6-7. Type 3 Processor Complexes—Presence-Detect Bits

Type 3 Processor Complexes—Cache Address Map

The following map is a summary of those addresses within the memory address space that can be cached. Only system board memory is mapped into the microprocessor level 1 cache and level 2 cache. The type 3A processor complex has a standard external 256KB L2 cache.

The system memory address space contains three cacheable regions:

- Region 1—Memory addresses from 0 up to 1MB
- Region 2—Memory addresses from 1MB up to 16MB
- Region 3—Memory addresses from 16MB up to 64MB.

All system board memory in region 2 and region 3 is cacheable. Programmable boundary registers for region 2 and region 3 control the upper boundaries of the memory space to be cached. The Set Configuration utility assigns memory to these cached regions, depending on the system configuration. POST establishes these cached regions, and they must not be altered.

Nonsystem memory can be located as follows:

- Region 1—In the area between memory addresses 0C0000 and 0DFFFF
- Region 2—Memory addresses from 16MB down to system memory
- Region 3—Memory addresses from 4GB (minus 1MB) down to system memory.

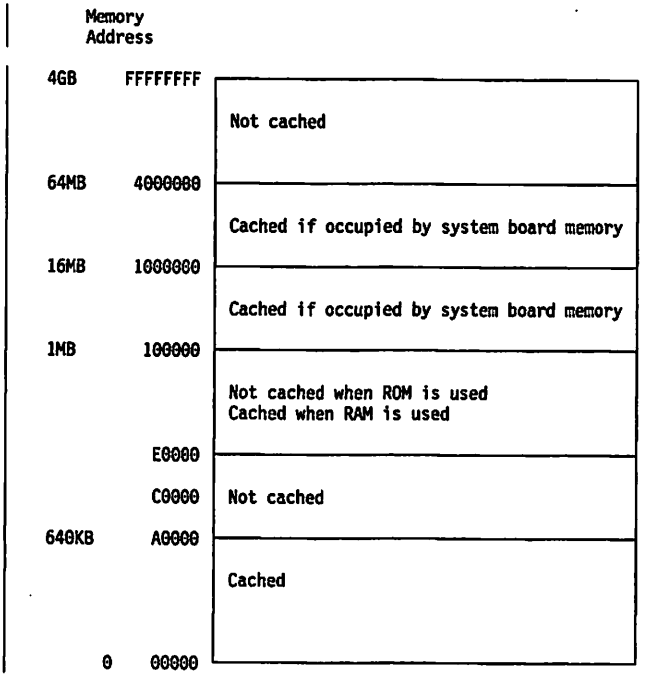


Figure 6-8. Type 3 Processor Complexes—Cache Address Map Summary

Type 3 Processor Complexes—Read-Only Memory Subsystem

The ROM subsystem is located on the processor complex and consists of 128KB in a 128K by 8-bit arrangement. The ROM is active at power-on at memory address space hex 000E0000 to 000FFFFF. The ROM contains the code that initializes the system to load and execute POST and BIOS code from a DASD device. ROM is also assigned at the top of the 4GB memory address space from hex FFFE0000 to FFFFFFFF.

Index

Numerics

80486DX performance 4-5, 4-8, 4-13, 6-5
80486DX2 performance 5-8
80486SX performance 4-11, 5-5

A

acoustic readings 1-10
adapter setup register 2-12
address 20 gate 3-23
address maps
  POS 2-4
  system 1-6
alternate reset 3-24
arbiter programming 3-4
arbitration control point 3-3
arbitration level 3-3
arbitration register 3-4
arbitration, central control point 3-4

B

base memory bytes 3-20
battery 3-10
boot sequence 3-26
bus contention 2-3
bus priority assignments 3-3

C

cache connector 4-15
cache map 4-17, 5-12, 6-10
card selected feedback 2-5
-CD SFDBK 2-5
central arbitration control point 3-3
channel 1-4, 3-3
channel check 3-22
channel-check latch 3-22
CMOS RAM 3-10
codes, POST error 3-28
configuration CRC bytes 3-20
configuration, RT/CMOS 3-17
connector numbering, memory 3-8
connector, optional cache 4-15

D

date-century byte 3-20
description
  NMI 3-21
  password 3-25
  programmable option select 2-3
  real-time clock 3-10
  system 1-3
  system board 1-4
description, power supply 1-10
diagnostic status byte (RT/CMOS) 3-17
diskette drive connector 3-7
diskette drive information, POS 2-10, 2-11
diskette drive type byte 3-18
diskette overruns 3-4
display panel, information 3-28
DMA channels 3-4

E

enable NMI 3-11
equipment byte 3-19
error codes, POST 3-28
extended arbitration 3-6

F

failures and messages, POST 3-28
fault, overvoltage 1-12
features
  processor complex 1-5, 4-3, 5-3, 6-3
feedback, card selected 2-5
fixed disk drive initialization 3-17

© Copyright IBM Corp. 1990, 1992

G

gate A20 3-23

H

hardware compatibility 3-27

I

I/O address map 1-6
identifier, model 4-3, 5-3, 6-3
information panel 3-28
interrupts
  IRQ0 reset 3-22
  NMI reset 3-21

L

L2 cache 4-15, 6-7
light, power 1-10

M

maximum current 1-9
measurements 1-9
memory
  connectors 3-8
  performance 4-5, 4-8, 4-11, 4-13, 5-5, 5-8, 6-5
  refresh 3-4
memory information, POS 2-7
memory numbering 3-8
memory presence detect 4-16, 5-11, 6-9
memory size miscompare 3-17
messages, POST error 3-28
Micro Channel 1-4, 3-3
microprocessor
  alternate reset 3-24
  gate A20 3-23
  mode switch compatibility 3-24
  performance 4-5, 4-8, 4-11, 4-13, 5-5, 5-8, 6-5
mode switching 3-24
model/submodel bytes 4-3, 5-3, 6-3

N

NMI mask 3-11
NMI service 3-4
NMI signal 3-4
noise readings 1-10
nonmaskable interrupt (NMI) 3-21
numbering, memory connector 3-8

O

operating system boot sequence 3-26
optional cache 4-15
output voltage sequencing 1-12
outputs, power supply 1-11
overvoltage fault 1-12

P

panel, information 3-28
parallel port select 2-6
parity check 3-22
password, power-on 3-25
performance 4-5, 4-8, 4-11, 4-13, 5-5, 5-8, 6-5
ports, system 3-22
POS address map 2-4
POS register 2 2-6
POS register 3 2-7
POS register, diskette drive 2-10, 2-11
POST error codes 3-28
power specifications 1-9
power supply 1-4
power supply description 1-10
power supply LED 1-10
power supply output protection 1-12
power supply outputs 1-11
power-on password 3-25
processor cache map 4-17, 5-12, 6-10
processor complex 1-5
processor performance 4-5, 4-8, 4-11, 4-13, 5-5, 5-8, 6-5
programmable option select (POS) 2-3

programmable option select (POS)
(continued)
address decode 2-5
address map 2-4
registers 2-4
setup procedures 2-4
setup register 2-5
system board 2-5
system board I/O 2-6
system configuration utilities 2-3
warning 2-3
programming, arbiter 3-4
protected mode switch 3-24
protection, power supply 1-12

R

real mode switch 3-24
real-time clock bytes 3-13
refresh 3-4
refresh request 3-22
registers
adapter setup 2-12
card feedback 2-5
miscellaneous system 3-22
RT/CMOS and NMI mask 3-11
RT/CMOS status registers 3-14
system board POS 2-5
system control 3-22
restore channel check 3-22
RT/CMOS address register 3-11
RT/CMOS RAM 3-10
password 3-25
secured area 3-23

S

selectable boot 3-26
sequencing, output voltage 1-12
serial port address select 2-10
set configuration 3-26
setup
bus contention 2-3
registers 2-5
system board 2-5
system board I/O 2-6
shutdown status byte 3-17
size 1-9
sound specifications 1-10
speaker data enable 3-23
specifications 1-9, 4-5, 4-8, 4-11, 4-13, 5-5, 5-8, 6-5
performance 4-5, 4-8, 4-11, 4-13, 5-5, 5-8, 6-5
physical 1-9
system unit 1-9
startup sequence 3-26
status registers (RT/CMOS) 3-14
switch to real 3-24
system address map 1-6
system board 1-3, 1-4
features 1-4
I/O register 2-6
memory connector 3-8
model identifier 4-3, 5-3, 6-3
POS registers 2-5
setup 2-5
system configuration utilities 2-3
system control port A 3-23
system control ports 3-22
system description 1-3
system overview 1-1
system ports, miscellaneous 3-22
system reset 3-21
system unit specifications 1-9

T

time status indicator 3-17

V

valid RAM bit 3-16

W

warnings
arbitration 3-4
central arbiter 3-5
NMI mask 3-21
POS 2-3
real-time clock 3-11
reserved areas xiii

watchdog status 3-23